

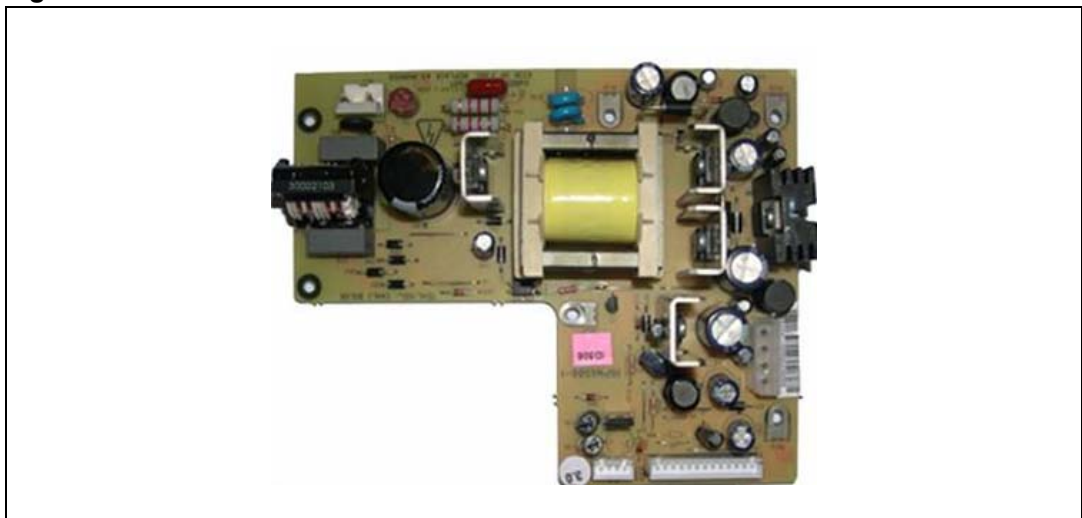
SMPS for high-end PVR based on L6668

Introduction

The set-top box (STB) market is growing very fast due to the high growth of both satellite and terrestrial/cable broadcasting. As expected, the market is always looking for solutions with high cost effectiveness and performance.

This document introduces a reference design of a 55 W switch-mode power supply dedicated to high-end set-top box applications, and in particular for PVRs (Personal Video Recorders). This kind of solution in addition to typical loads is able to supply HD and VFD front panels. The board accepts European input voltage range (from 185 to 265V_{ac}) and delivers eight outputs. It is based on the advanced current mode PWM controller L6668, working at fixed frequency. Despite high performance, standard parts are used, e.g. standard capacitors are connected on the outputs in place of low ESR components commonly used, contributing to an overall decrease of the total cost of the solution.

Figure 1. STEVAL-ISA040V1



Contents

- 1 Main characteristics 5**

- 2 Circuit description 7**
 - 2.1 Transformer specification 8
 - 2.1.1 Windings data 8
 - 2.2 BOM 9

- 3 Test description 12**
 - 3.1 Cross regulation and main waveforms 12
 - 3.2 High frequency ripple of output voltages at full load 20
 - 3.3 Measurement of RMS current of output capacitors 21
 - 3.4 Dynamic load test 21
 - 3.5 Startup behavior 23
 - 3.6 Wakeup time 26
 - 3.7 Short circuit test 27
 - 3.8 Conducted emission (EMI) measurements 28
 - 3.9 Thermal measurements 28

- 4 Conclusions 29**

- 5 Revision history 29**

List of tables

Table 1.	Output specifications	5
Table 2.	Windings parameters	8
Table 3.	Bill of material	9
Table 4.	Output voltages measurement at $V_{in}= 184$ V and full load	12
Table 5.	Output voltages measurement at $V_{in}= 230$ V and full load	12
Table 6.	Output voltages measurement at $V_{in}= 276$ V and full load	13
Table 7.	Output voltages measurement at $V_{in}= 184$ V and reduced load	14
Table 8.	Output voltages measurement at $V_{in}= 230$ V and reduced load	15
Table 9.	Output voltages measurement at $V_{in}= 276$ V and reduced load	15
Table 10.	Output voltages measurement at $V_{in}= 184$ V and reduced load (20 W)	17
Table 11.	Output voltages measurement at $V_{in}= 230$ V and reduced load (20 W)	17
Table 12.	Output voltages measurement at $V_{in}= 276$ V and reduced load (20 W)	17
Table 13.	Output voltages measurement at $V_{in}= 230$ V and light load	19
Table 14.	Measurement of high frequency ripple of output voltages at $V_{in}= 230$ V and full load	20
Table 15.	Measurement of RMS current of output capacitors at $V_{in}= 230$ V and full load	21
Table 16.	Dynamic load test on $3.3 V_{out}$	22
Table 17.	Dynamic load test on $5 V_{out}$	22
Table 18.	Overshoot	25
Table 19.	Thermal behavior of the components at primary side	28
Table 20.	Thermal behavior of the components at secondary side	29
Table 21.	Document revision history	29

List of figures

Figure 1.	STEVAL-ISA040V1.....	1
Figure 2.	Electrical schematic	6
Figure 3.	Transformer electrical and mechanical drawings	8
Figure 4.	Vds and Id of STP5NK60Z in full load at $V_{in} = 184 V_{rms} - 50 Hz$	13
Figure 5.	Vds and Id of STP5NK60Z in full load at $V_{in} = 230 V_{rms} - 50 Hz$	13
Figure 6.	Vds and Id of STP5NK60Z in full load at $V_{in} = 276 V_{rms} - 50 Hz$	14
Figure 7.	Vds and Id of STP5NK60Z at reduced load $V_{in} = 184 V_{rms} - 50 Hz$	15
Figure 8.	Vds and Id of STP5NK60Z at reduced load $V_{in} = 230 V_{rms} - 50 Hz$	16
Figure 9.	Vds and Id of STP5NK60Z at reduced load $V_{in} = 276 V_{rms} - 50 Hz$	16
Figure 10.	Vds and Id of STP5NK60Z at reduced load (20 W) $V_{in} = 184 V_{rms} - 50 Hz$	18
Figure 11.	Vds and Id of STP5NK60Z at reduced load (20 W) $V_{in} = 230 V_{rms} - 50 Hz$	18
Figure 12.	Vds and Id of STP5NK60Z at reduced load (20 W) $V_{in} = 276 V_{rms} - 50 Hz$	19
Figure 13.	Vds and Id of STP5NK60Z at light load at 230 V	20
Figure 14.	High frequency ripple of output voltages at full load at 230 V	21
Figure 15.	Outputs behavior under dynamic load on 3.3 V output at $V_{in}=230 V$	22
Figure 16.	Behavior of outputs with dynamic load applied to 5 V output at $V_{in}=230 V$	23
Figure 17.	Startup behavior of the system at $V_{in} = 184 V_{rms} - 50 Hz$	24
Figure 18.	Startup behavior of the system at $V_{in} = 230 V_{rms} - 50 Hz$	24
Figure 19.	Startup behavior of the system at $V_{in} = 276 V_{rms} - 50 Hz$	25
Figure 20.	Wakeup behavior of the system at $V_{in} = 184 V_{rms} - 50 Hz$	26
Figure 21.	Wakeup behavior of the system at $V_{in} = 230 V_{rms} - 50 Hz$	26
Figure 22.	Wakeup behavior of the system at $V_{in} = 276 V_{rms} - 50 Hz$	27
Figure 23.	Short circuit on 5 V output	27
Figure 24.	Conducted emissions of the system at full load and $V_{in}=230 V$ - phase conducted emission	28
Figure 25.	Conducted emissions of the system at full load and $V_{in}=230 V$ -neutral conducted emission	28

1 Main characteristics

The main characteristics of the SMPS are listed below:

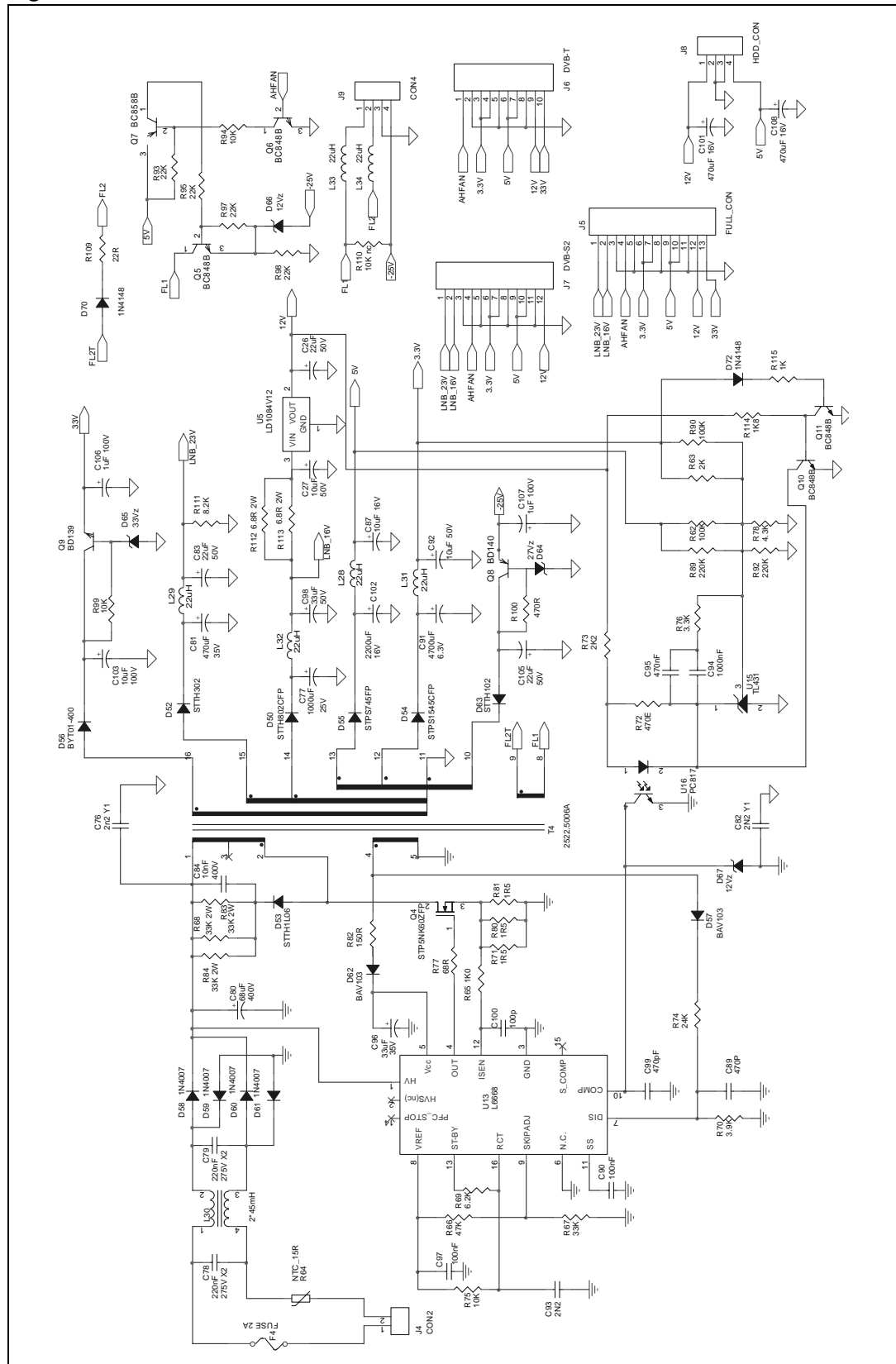
- Input voltage:
 - $V_{in} = 185 \div 265 V_{rms}$
 - $f=50 \text{ Hz}$

Table 1. Output specifications

	Vout (V):	Iout (A)	Pout (W)	Tolerance	Notes
1	3.3	3.5	11.55	+/- 5%	Dedicated to 3.3 V circuitry, 2.6 V and 1.1 V local post regulators
2	5	1.9	9.5	+/- 5%	Dedicated to HDD, display, 5V circuitry and 2.6 V local post regulators
3	12	0.8	9.6	+/- 2%	Dedicated to HDD
4	16	0.5	8	+/- 10%	Dedicated to LNB for satellite DVB
5	23	0.5	11.5	+/- 10%	Dedicated to LNB for satellite DVB
6	-25	0.15	3.75	+/- 10%	Dedicated to display
7	3.3 AC	0.08	0.25		Dedicated to the display filaments
8	33	0.01	0.33	+/- 10%	Dedicated to the tuner
		P _{OUT} (W) =		55 W	

- EMI: in accordance with EN55022 Class B
- Safety: in accordance with IEC 60065 7th ed.

Figure 2. Electrical schematic



2 Circuit description

The topology used in this power supply is a standard flyback, working in continuous conduction mode with fixed frequency. The switching frequency (65 kHz) represents a good trade-off between the transformer size and the harmonics of the switching frequency, in order to optimize the input filter size and cost. The Power MOSFET is a 600 V-1.6 Ω in SuperMESH® technology, housed in a TO-220FP (insulated package). The reflected voltage is 70 V, providing enough room for the leakage inductance voltage spike with still margin for reliability. The network D53-R68- R83-R84-C84 clamps the peak of the leakage inductance voltage spike.

The controller is the new L6668, integrating all the functionalities needed to control an SMPS with high performance and minimum component count, offering the maximum flexibility. A new functionality embedded in the device is a high voltage startup internal circuit which draws current from the DC bus and charges the IC supply capacitor (C96). As soon as the voltage on this capacitor reaches the L6668 turn-on threshold, the controller starts to drive the MOSFET, and the IC is supplied only by the auxiliary winding of the transformer via the diode D62 (After startup, the HV current source is deactivated, saving power during normal operation).

The control system is Current Mode, so the current flowing in the primary is sensed by R71, R80 and R81 then filtered by R65 and C100 and fed into pin 12 (Isen). No slope compensation is needed as the duty cycle is kept well below 50%. The circuit connected to pin 7 (DIS) provides overvoltage protection in case of feedback network failures and open loop operation. An internal comparator senses this pin voltage and in case its threshold is exceeded, the L6668 stops operating and reduces its consumption. After Disable intervention the controller operation can be resumed only by disconnecting the mains plug. The switching frequency is programmed by the RC network connected to pin 16 (RCT) and in case of reduced load operation, the controller can decrease the operating frequency via pin 13 (ST-BY) and resistor R69 proportionally to the load consumption.

The output rectifiers have been chosen according to the maximum reverse voltage and power dissipation. The 3.3 V and 5 V outputs rectifiers are Schottky type, featuring lower losses compared to standard PN diodes. The diodes D50, D54 and D55 need a small heat sink, as indicated on the BOM. The other output rectifiers are fast recovery. The 12 V output is obtained from the 16 V output by a high-current low-drop voltage regulator.

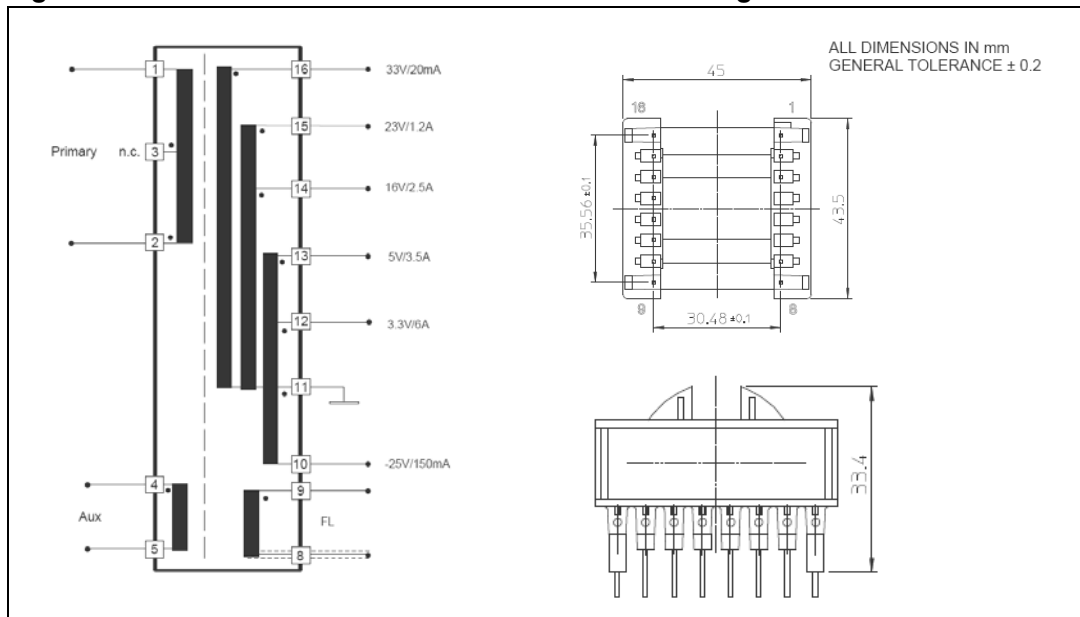
The output voltage control is performed by the secondary feedback on the 5 V and 3.3 V outputs, while for the other outputs the control is achieved by the transformer coupling. The feedback network uses a TL431 driving an opto-coupler, in this case a PC817, ensuring the required insulation between primary and secondary. The opto-transistor drives directly the COMP pin of the L6668. An LC filter has been added on all outputs in order to filter the high frequency ripple without increasing the output capacitors.

The input EMI filter consists of two X2 capacitors with a common mode choke in between. The NTC limits the inrush current charging the input capacitor at plug-in.

The transformer is layer type, manufactured by Pulse Eldor Corporation, in accordance with the safety standard IEC 60065 7th ed.

2.1 Transformer specification

Figure 3. Transformer electrical and mechanical drawings



- Primary inductance: 675 $\mu\text{H} \pm 10\%$ at 10 kHz - 1 V
- Leakage inductance: $\leq 20 \mu\text{H}$ at 100 kHz - 1 V
- Typical operating frequency: 65 kHz

2.1.1 Windings data

Table 2. Windings parameters

Terminal no.	Windings	Number of turns	Wire
2-3	W1 primary/2	26	0.45 - G
12-11	W2 - 3.3 V	3	Cu-foil - W=10 mm T=0.1 mm
13-12	W3 - 5 V	1	Cu-foil - W=10 mm T=0.1 mm
14-11	W4 - 16 V	12	2x0.45-G2
15-14	W5 - 23 V	4	0.45-G2
16-11	W6 - 33 V	26	0.25-G2
10-11	W7 - 25 V	20	0.25-G2
9-8	W8 - FL	3	0.25-G2
4-5	W9 - Aux	10	0.25-G2
3-1	W10 - primary/2	26	0.45-G2

2.2 BOM

Table 3. Bill of material

Qty	Reference	Value & part	Description
3	C26,C83,C105	22 μ F 50 V	Electrolytic cap
1	C27	10 μ F 50 V	Electrolytic cap
2	C76,C82	2.2 nF 4 Kv	Y1 cap
1	C77	1000 μ F 25 V	Electrolytic cap
2	C78,C79	220 nF 75 V	X2 cap
1	C80	68 μ F 400 V	Electrolytic cap
1	C81	470 μ F 35 V	Electrolytic cap
1	C84	10 nF 400 V	Ceramic cap
1	C87	10 μ F 16 V	Electrolytic cap
2	C89,C99	470 pF 0805 50 V	SMD ceramic cap
1	C90	100 nF 1206 50 V	SMD ceramic cap
1	C91	4700 μ F 6.3 V	Electrolytic cap
1	C92	10 μ F 50 V	Electrolytic cap
1	C93	2.2 nF 0805 50 V	SMD ceramic cap
1	C94	1000 nF 0805 50 V	SMD ceramic cap
1	C95	470 nF 1206 50 V	SMD ceramic cap
1	C96	33 μ F 35 V	Electrolytic cap
1	C97	100 nF 0805 50 V	SMD ceramic cap
1	C98	33 μ F 50 V	Electrolytic cap
2	C101, C108	470 μ F 16 V	Electrolytic cap
1	C106, C107	1 μ F 100V	Electrolytic cap
1	C100	100 pF 0805 25 V	SMD ceramic cap
1	C102	2200 μ F 16 V	Electrolytic cap
1	C103	10 μ F 100 V	Electrolytic cap
1	D50	STTH802CFP	STMicroelectronics high-efficiency, ultrafast diode
1	D52	STTH302	STMicroelectronics high-efficiency, ultrafast diode
1	D53	STTH1L06	STMicroelectronics ultrafast, high-voltage rectifier
1	D54	STPS1545CFP	STMicroelectronics power Schottky rectifier
1	D55	STPS745FP	STMicroelectronics power Schottky rectifier
1	D56	BYT01-400	STMicroelectronics high-efficiency, ultrafast diode
2	D57,D62	BAV103	General-purpose rectifier
4	D58,D59,D60,D61	1N4007	Rectifier
1	D63	STTH102	STMicroelectronics ultrafast diode

Table 3. Bill of material (continued)

Qty	Reference	Value & part	Description
1	D64	27Vz DO35 1 W	Zener diode
1	D65	33Vz D035 1 W	Zener diode
2	D66,D67	12Vz D034	0.5W Zener diode
2	D70,D72	1N4148	General-purpose rectifier
1	F4	FUSE 2 A	Radial fuse
1	J4	CON2 7.62 mm pitch	Two-pin Input connector
1	J5	Full_Con 2.54 mm pitch	13-pin output connector
1	J8	HDD_Con RS code:471-430	Hard disk connector
1	J9	CON4 2.54 mm pitch	4-pin VFD connector
4	L28,L29,L31,L32	22 μ H 5 A	Radial power inductor
1	L30	2*45 mH-HF2430-453	TDK common-mode choke coils
2	L33,L34	22 μ H 1 A	Radial inductor
1	Q4	STP5NK60ZFP	STMicroelectronics N-Channel Power MOSFET
4	Q5,Q6,Q10,Q11	BC848B	NPN general-purpose bipolar
1	Q7	BC858B	PNP general-purpose bipolar
1	Q8	BD140	STMicroelectronics PNP Transistor
1	Q9	BD139	STMicroelectronics NPN Transistor
3	R62,	100 k Ω 0805	SMD resistor
	R75,R94	10 k Ω 0805	SMD resistor
1	R63	2 k Ω 0805	SMD resistor
1	R64	NTC_16 Ω 2.9 A	Inrush current suppressor
1	R65	1 k Ω 0805	SMD resistor
1	R66	47 k Ω 0805	SMD resistor
1	R67	33 k Ω 0805	SMD resistor
2	R68,R83,R84	33 k Ω 2 W	Axial resistor
1	R69	6.2 k Ω 1206	SMD resistor
1	R70	3.9 k Ω 0805	SMD resistor
3	R71,R80,R81	1.5 Ω 1206	SMD resistor
1	R72	470 Ω 0805	SMD resistor
1	R73	2.2 k Ω 1206	SMD resistor
1	R74	24 k Ω 1206	SMD resistor
1	R76	3.3 k Ω 1206	SMD resistor
1	R77	68 Ω 1206	SMD resistor
1	R78	4.3 k Ω 0805	SMD resistor
1	R79 not mounted	1 M Ω ¼ W	Axial resistor

Table 3. Bill of material (continued)

Qty	Reference	Value & part	Description
1	R82	150 Ω 1206	SMD resistor
2	R89,R92	220 k Ω 0805	SMD resistor
1	R90	100 k Ω 0805	SMD resistor
4	R93,R95,R97,R98	22 k Ω 0805	SMD resistor
1	R99	10 k Ω 0805	SMD resistor
1	R100	470 Ω ¼ W	Axial resistor
1	R109	22 Ω ¼ W	Axial resistor
1	R110 not mounted	10 k Ω 0805	SMD resistor
1	R111	8.2 k Ω ¼ W	Axial resistor
2	R112,R113	6.8 Ω 2 W	Axial resistor
1	R114	1.8 k Ω 0805	SMD resistor
1	R115	1 k Ω 0805	SMD resistor
1	T4	2522.5006C	Pulseeng SMT
1	U5	LD1084V12	STMicroelectronics 5 A low-drop, positive voltage regulator
1	U13	L6668	STMicroelectronics smart primary controller
1	U15	TL431	STMicroelectronics voltage reference
1	U16	PC817	OptoCoupler

Note: Q4 needs 15 °C/W heatsink;
D50, D54, D55 needs 20 °C/W heatsink;
U5 needs 12 °C/W heatsink;

3 Test description

The set of tests performed on the board aim to evaluate the performance of the power supply for different load conditions, in terms of regulation, power consumption, efficiency and safe operating area of the Power MOSFET,

Moreover, in order to evaluate the behavior of the SMPS in terms of stability, the performance under dynamic load condition have been measured and several tests have been performed at startup with three different input voltage values and full load conditions.

Finally the conducted emission measurements and the thermal performances of the main critical components have been evaluated.

3.1 Cross regulation and main waveforms

In [Table 4](#), [5](#), and [6](#) the output voltage cross regulation is given with static and dynamic loads and the overall efficiency of the converter measured at different input voltages. All the output voltages have been measured after the load connector by means of a digital multimeter. The length of the connection cable is 100 mm. Moreover the primary Power MOSFET STP5NK60Z main waveforms are shown.

- Full load - Satellite2 DVB

Table 4. Output voltages measurement at $V_{in}= 184$ V and full load

V_{out} [V]	3.42	5.1	11.94	16.8	22.94	32.28	-26.9	V_{in} [V _{rms}]	184
$\Delta V_{out}\%$	+ 3.6	+ 2	-0.5	+ 5	- 0.26	-2.2	+ 7.6		
I_{out} [A]	3.5	1.9	0.8	0.5	0.5	0.01	0.15	I_{in} [A _{rms}]	0.742
P_{out} [W]	11.97	9.69	9.55	8.41	11.49	0.32	4.03	P_{in} [W]	76.3
P_{outTOT} [W]	55.46							η (%)	73
f_s [kHz]	67.8								

Note: All voltages are within tolerance.

Table 5. Output voltages measurement at $V_{in}= 230$ V and full load

V_{out} [V]	3.44	5.08	11.9	16.71	22.8	31.98	-26.67	V_{in} [V _{rms}]	230
$\Delta V_{out}\%$	4.2	+1.6	-0.8	+4.4	-0.8	-2.2	+6.68		
I_{out} [A]	3.5	1.9	0.8	0.5	0.5	0.01	0.15	I_{in} [A _{rms}]	0.623
P_{out} [W]	12.04	9.65	9.52	8.37	11.44	0.32	4	P_{in} [W]	75.2
P_{outTOT} [W]	55.34							η (%)	73.6
f_s [kHz]	67.1								

Note: All voltages are within tolerance.

Table 6. Output voltages measurement at $V_{in} = 276\text{ V}$ and full load

V_{out} [V]	3.42	5.09	11.91	16.69	22.8	32.21	-26.72	V_{in} [V_{rms}]	276
$\Delta V_{out}\%$	3.6	+1.8	-0.75	+4.3	-0.8	-2.4	+6.88		
I_{out} [A]	3.5	1.9	0.8	0.5	0.5	0.01	0.15	I_{in} [A_{rms}]	0.548
P_{out} [W]	11.97	9.67	9.53	8.36	11.41	0.32	4	P_{in} [W]	74.9
P_{outTOT} [W]	52.5							η (%)	73.8
f_s [kHz]	66.4								

Note: All voltages are within tolerance.

Figure 4. V_{ds} and I_d of STP5NK60Z in full load at $V_{in} = 184\text{ V}_{rms} - 50\text{ Hz}$

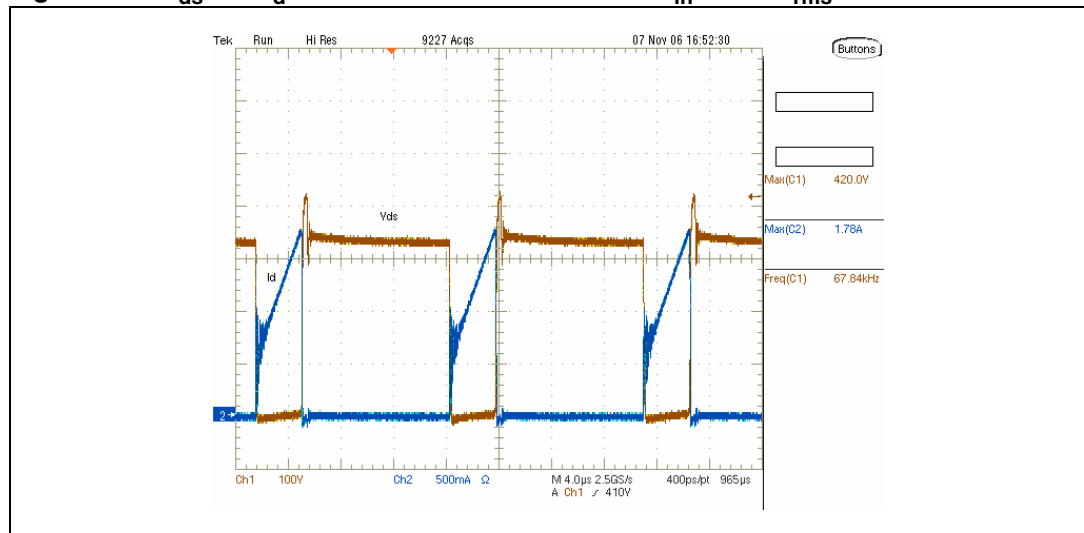


Figure 5. V_{ds} and I_d of STP5NK60Z in full load at $V_{in} = 230\text{ V}_{rms} - 50\text{ Hz}$

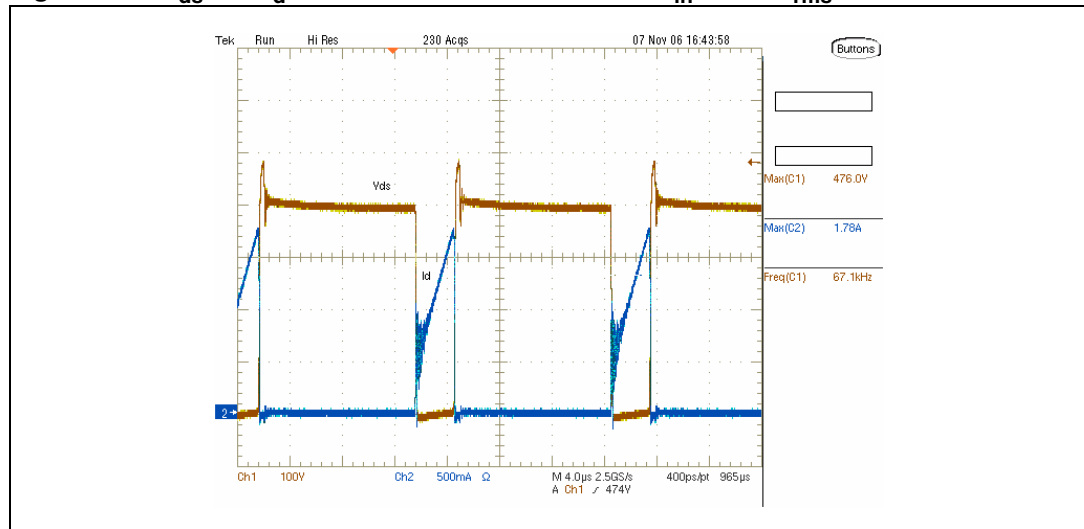
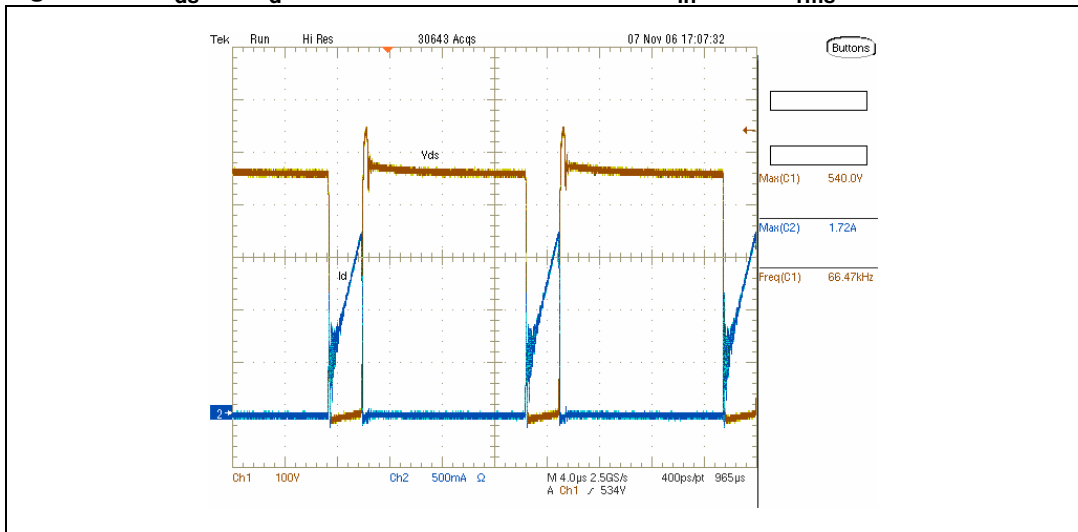


Figure 6. V_{ds} and I_d of STP5NK60Z in full load at $V_{in} = 276 V_{rms} - 50 Hz$



Note: CH1: drain voltage (brown)

CH2: drain current (blue)

- $V_{in} (V_{ac})$: 184 - 230 - 276
- $V_{dsMax} (V)$: 420 - 476 - 540
- $I_{dPk} (A)$: 1.78 - 1.78 - 1.72

The measured values are the drain peak voltage and current at minimum, nominal and maximum input mains voltage, during normal operation at full load. The voltage peak, which is 540 V, assures a reliable operation of the STP5NK60ZFP with a good margin against the maximum BV_{DSS} .

- Reduced load - terrestrial DVB (without LNB)

Table 7. Output voltages measurement at $V_{in} = 184 V$ and reduced load

$V_{out} [V]$	3.38	5.11	11.92	17.19	24.26	32.2	-26.83	$V_{in} [V_{rms}]$	184
$\Delta V_{out} \%$	+2.42	+2.2	-0.6	+7.4	+5.4	-2.4	+7.32		
$I_{out} [A]$	3.5	1.9	0.8	-	0.003 ⁽¹⁾	0.01	0.15	$I_{in} [A_{rms}]$	0.531
$P_{out} [W]$	11.83	9.7	9.54	-	0.072	0.32	4	$P_{in} [W]$	52.6
$P_{outTOT} [W]$	35.5						$\eta (\%)$	67.5	
$f_s [kHz]$	63.5								

1. With a 8.2 k Ω 1/4 W dummy load

Note: All voltages are within tolerance.

Table 8. Output voltages measurement at $V_{in}=230\text{ V}$ and reduced load

V_{out} [V]	3.39	5.09	11.92	17.15	24.21	32.2	-26.7	V_{in} [V_{rms}]	230
$\Delta V_{out}\%$	+2.72	+1.8	-0.6	+7.18	+5.26	-2.4	+6.8		
I_{out} [A]	3.5	1.9	0.8	-	0.003 ⁽¹⁾	0.01	0.15	I_{in} [A_{rms}]	0.448
P_{out} [W]	11.86	9.67	9.54	-	0.072	0.32	4	P_{in} [W]	52.3
P_{outTOT} [W]	35.47							η (%)	67.8
f_s [kHz]	62.2								

1. With a 8.2 k Ω 1/4 W dummy load

Note: All voltages are within tolerance.

Table 9. Output voltages measurement at $V_{in}=276\text{ V}$ and reduced load

V_{out} [V]	3.37	5.1	11.92	17.16	24.2	32.24	-26.82	V_{in} [V_{rms}]	276
$\Delta V_{out}\%$	+2.12	+2	-0.6	+7.2	+5.2	-2.3	+7.28		
I_{out} [A]	3.5	1.9	0.8	-	0.003 ⁽¹⁾	0.01	0.15	I_{in} [A_{rms}]	0.396
P_{out} [W]	11.79	9.69	9.54	-	0.072	0.32	4.1	P_{in} [W]	52.3
P_{outTOT} [W]	35.5							η (%)	67.9
f_s [kHz]	61								

1. With a 8.2 k Ω 1/4 W dummy load

Note: All voltages are within tolerance

Table 7, 8 and 9 show the output voltage measured applying the same loads that we could have if a different DVB type is powered (e.g. a terrestrial or cable) without the LNB. As under the load condition described before, all the output voltages are within the tolerances. To keep the 23 V LNB output within the tolerance, a negligible dummy load has to be connected on this output.

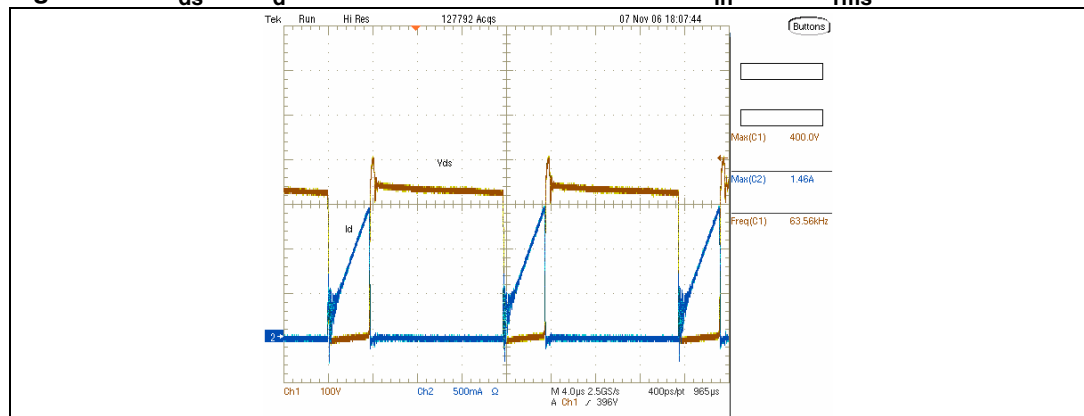
Figure 7. V_{ds} and I_d of STP5NK60Z at reduced load $V_{in} = 184\text{ V}_{rms} - 50\text{ Hz}$ 

Figure 8. V_{ds} and I_d of STP5NK60Z at reduced load $V_{in} = 230 V_{rms} - 50 Hz$

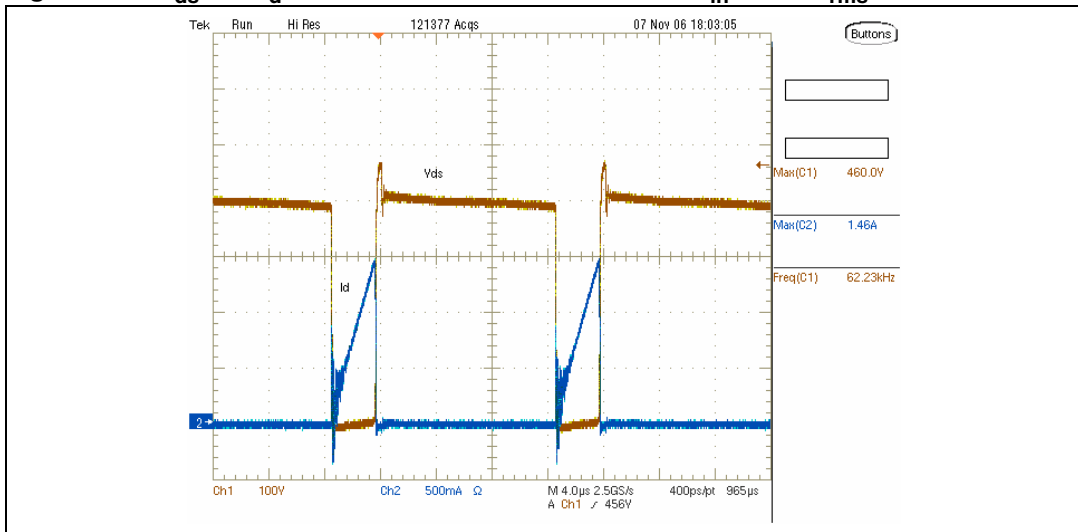
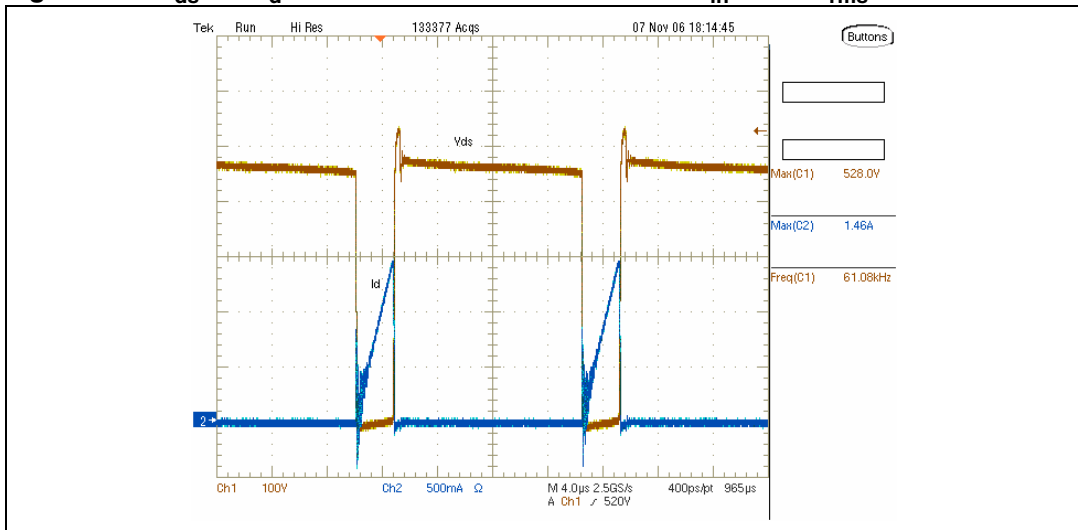


Figure 9. V_{ds} and I_d of STP5NK60Z at reduced load $V_{in} = 276 V_{rms} - 50 Hz$



Note: CH1: drain voltage (brown)

CH2: drain current (blue)

- $V_{in} (V_{ac})$: 184 - 230 - 276
- $V_{dsMax} (V)$: 400 - 460 - 528
- $I_{dpk} (A)$: 1.46 - 1.46 - 1.46

The measured values are the drain peak voltage and current at minimum, nominal and maximum input mains voltage, during normal operation at full load. The voltage peak, which is 528 V, assures a reliable operation of the STP5NK60Z with a good margin against the maximum BV_{DSS} .

- Reduced load - total power = 20 W

Table 10. Output voltages measurement at $V_{in}= 184$ V and reduced load (20 W)

V_{out} [V]	3.5	5	12	16.56	23.01	32.15	-26.2	V_{in} [V _{rms}]	184
$\Delta V_{out}\%$	+6	+0	+0	+3.5	+0	-2.5	+4.8		
I_{out} [A]	1.75	1	0.4	-	0.003 ⁽¹⁾	0.01	0.15	I_{in} [A _{rms}]	0.301
P_{out} [W]	6.125	5	4.8	-	0.07	0.32	3.93	P_{in} [W]	28.3
P_{outTOT} [W]	20.2							η (%)	71.4
f_s [kHz]	53.8								

1. With a 8.2 k Ω 1/4 W dummy load

Table 11. Output voltages measurement at $V_{in}= 230$ V and reduced load (20 W)

V_{out} [V]	3.5	5	11.98	16.57	23.03	32.1	-26.2	V_{in} [V _{rms}]	230
$\Delta V_{out}\%$	+6	+0	-0.16	+3.6	+0.1	-2.72	+4.8		
I_{out} [A]	1.75	1	0.4	-	0.003 ⁽¹⁾	0.01	0.15	I_{in} [A _{rms}]	0.256
P_{out} [W]	6.125	5	4.79	-	0.07	0.32	3.93	P_{in} [W]	28.35
P_{outTOT} [W]	20.2							η (%)	71.4
f_s [kHz]	52								

1. With a 8.2 k Ω 1/4 W dummy load

Table 12. Output voltages measurement at $V_{in}= 276$ V and reduced load (20 W)

V_{out} [V]	3.5	5.04	11.98	16.59	23.04	32.17	-26.2	V_{in} [V _{rms}]	276
$\Delta V_{out}\%$	+6	+0.8	-0.16	+3.7	+0.1	-2.5	+4.8		
I_{out} [A]	1.75	1	0.4	-	0.003 ⁽¹⁾	0.01	0.15	I_{in} [A _{rms}]	0.225
P_{out} [W]	6.125	5.04	4.79	-	0.07	0.32	3.93	P_{in} [W]	28.3
P_{outTOT} [W]	20.2							η (%)	71.4
f_s [kHz]	50								

1. With a 8.2 k Ω 1/4 W dummy load

Even still reducing the load down to 20 W, thanks to the coupling of the transformer, all the output voltages are well regulated. The tables above show that the switching frequency is decreased according to the power consumption.

Figure 10. V_{ds} and I_d of STP5NK60Z at reduced load (20 W) $V_{in} = 184 V_{rms} - 50 Hz$

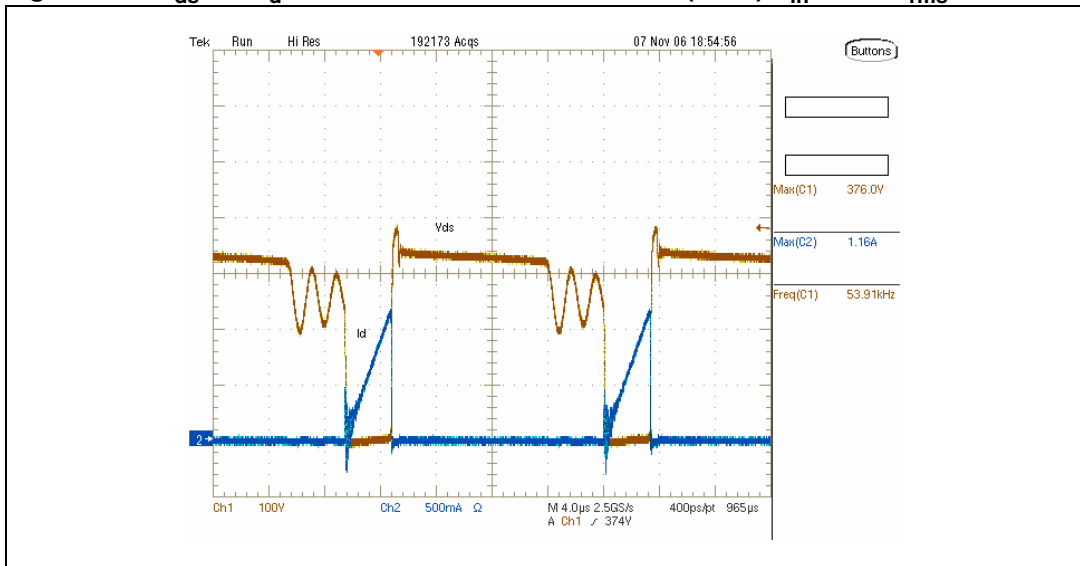


Figure 11. V_{ds} and I_d of STP5NK60Z at reduced load (20 W) $V_{in} = 230 V_{rms} - 50 Hz$

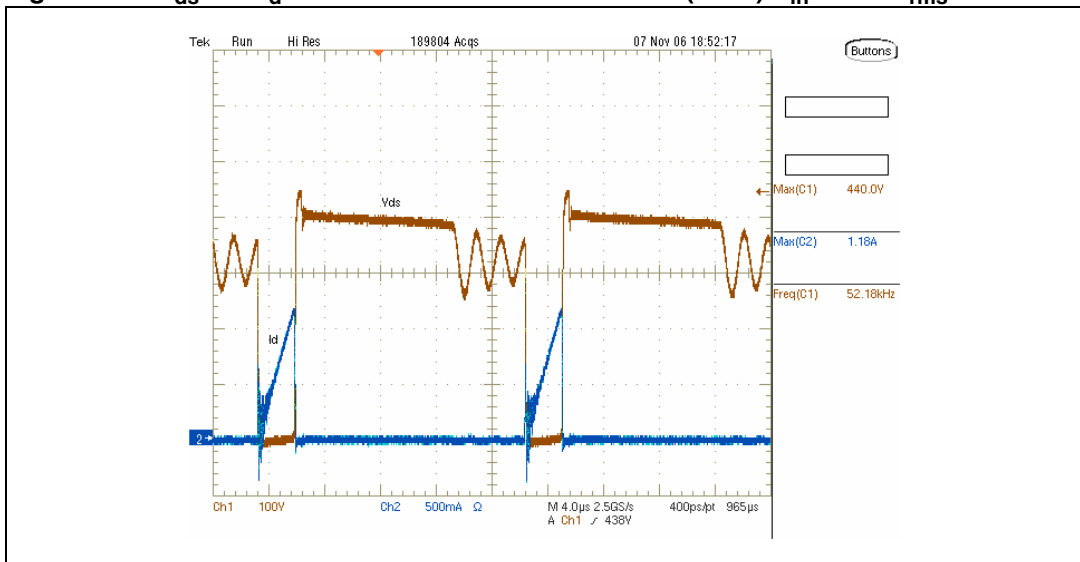
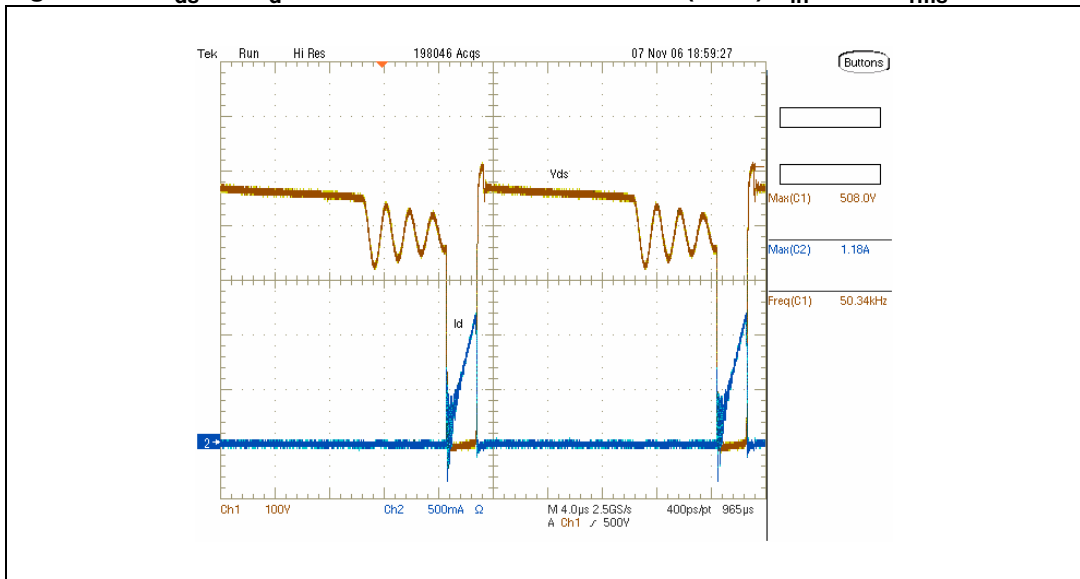


Figure 12. V_{ds} and I_d of STP5NK60Z at reduced load (20 W) $V_{in} = 276 V_{rms} - 50 Hz$



Note: CH1: drain voltage (brown)

CH2: drain current (blue)

- $V_{in} (V_{ac})$: 184 - 230 - 276
- $V_{dsMax} (V)$: 376 - 440 - 508
- $I_{dPk} (A)$: 1.16 - 1.18 - 1.18

The measured values are the drain peak voltage and current at minimum, nominal and maximum input mains voltage, during normal operation at full load. The voltage peak, which is 508 V, assures a reliable operation of the STP5NK60Z with a good margin against the maximum BV_{DSS} .

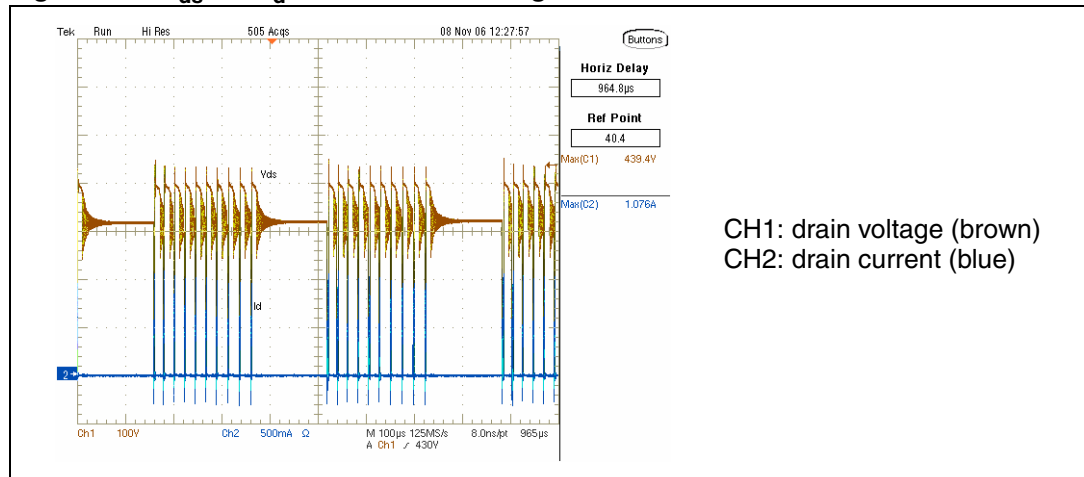
- Light load

Table 13. Output voltages measurement at $V_{in} = 230 V$ and light load

$V_{out} [V]$	3.58	5.25	12	16.52	22.65	32	-25.74	$V_{in} [V_{rms}]$	230
$I_{out} [A]$	0.8	0.08	0.08	-	0.003 ⁽¹⁾	0.01	0.15	$I_{in}[A_{rms}]$	0.114
$P_{out} [W]$	2.86	0.42	0.96	-	0.07	0.32	3.93	$P_{in} [W]$	11.3
$P_{outTOT} [W]$	8.56							$\eta(\%)$	75.7
$f_s [kHz]$	Burst mode								

1. with a 8.2 k Ω 1/4 W dummy load

Figure 13. V_{ds} and I_d of STP5NK60Z at light load at 230 V



Also in this load condition the circuit is still able to maintain all voltages under control, Hence a perfect functionality of the circuit is achieved also in this abnormal condition. During light load operation the circuit works in burst mode and, thanks to the controller functionality, the switching frequency inside the burst pulses is kept low. This allows low power consumption of the power supply under light load.

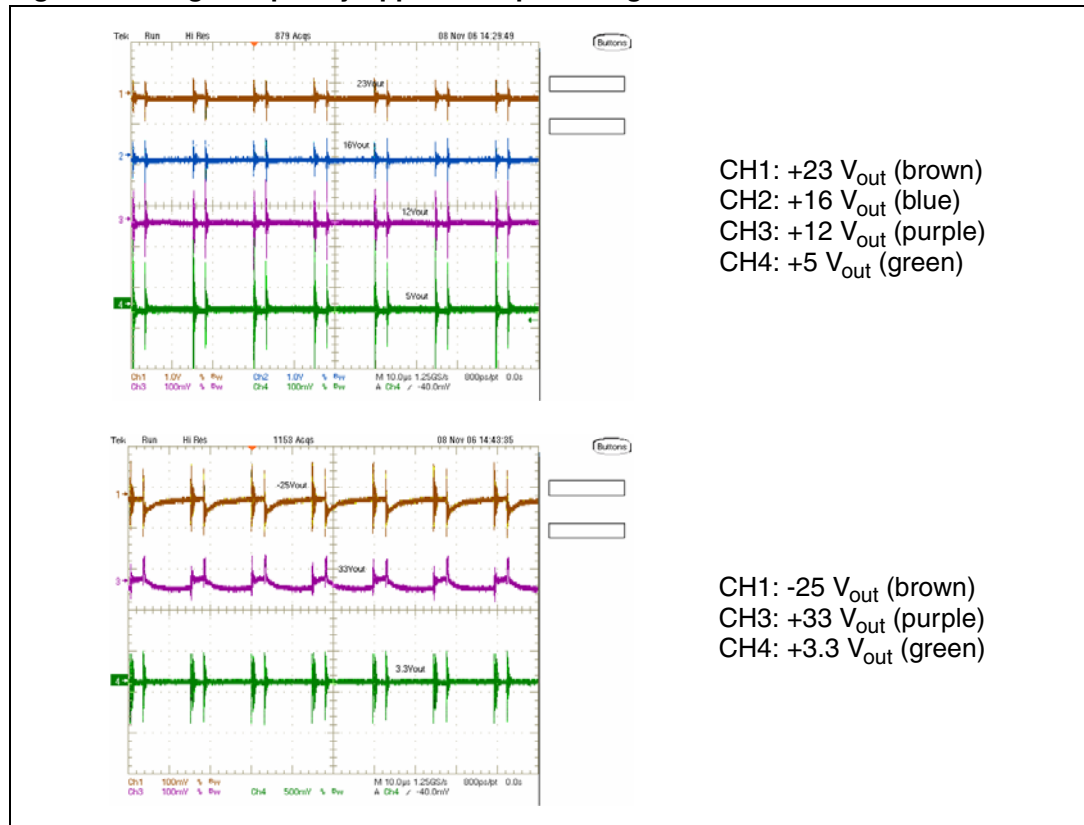
3.2 High frequency ripple of output voltages at full load

The output voltage ripple at switching frequency has been measured, as listed in [Table 14](#). In [Figure 14](#) the waveforms of the voltage ripple are shown.

Table 14. Measurement of high frequency ripple of output voltages at V_{in} = 230 V and full load

V_{out} [V]	3.3	5	12	16	23	33	-25
ΔV_{outHF} [mV]	11	6	4.8	46	36	29	43

Figure 14. High frequency ripple of output voltages at full load at 230 V



3.3 Measurement of RMS current of output capacitors

Table 15 shows the RMS current values flowing into the output capacitors at 230V_{ac}, full load. All the RMS currents are within the rating of the capacitor type indicated. This avoids any component overstress that could affect the reliability and the expected lifetime of the SMPS.

Table 15. Measurement of RMS current of output capacitors at V_{in}= 230 V and full load

I _{CapC77} (16V _{out})	I _{CapC91} (3.3V _{out})	I _{CapC81} (23V _{out})	I _{CapC102} (5V _{out})
0.850	1.9	0.550	1

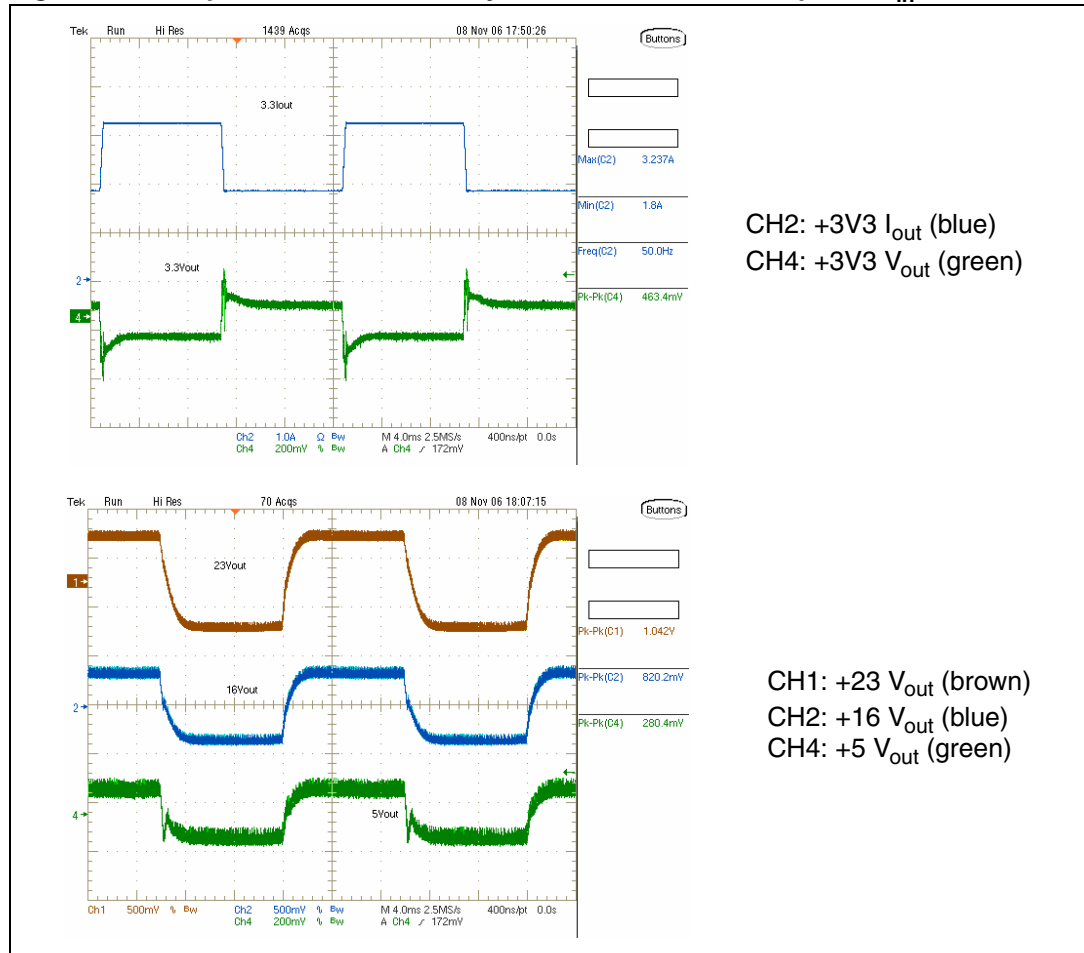
3.4 Dynamic load test

The dynamic load tests have been performed by varying the load on 3.3 V and 5 V outputs, keeping the other outputs at full load. Varying the load on 3.3 V output, the following results have been obtained:

Table 16. Dynamic load test on 3.3 V_{out}

Outputs	Load condition
+5 V, +12 V, +16 V, +23 V, +33 V, -25 V	Full load
+3.3 V	Load 50% ÷ 90%

Figure 15. Outputs behavior under dynamic load on 3.3 V output at V_{in} =230 V

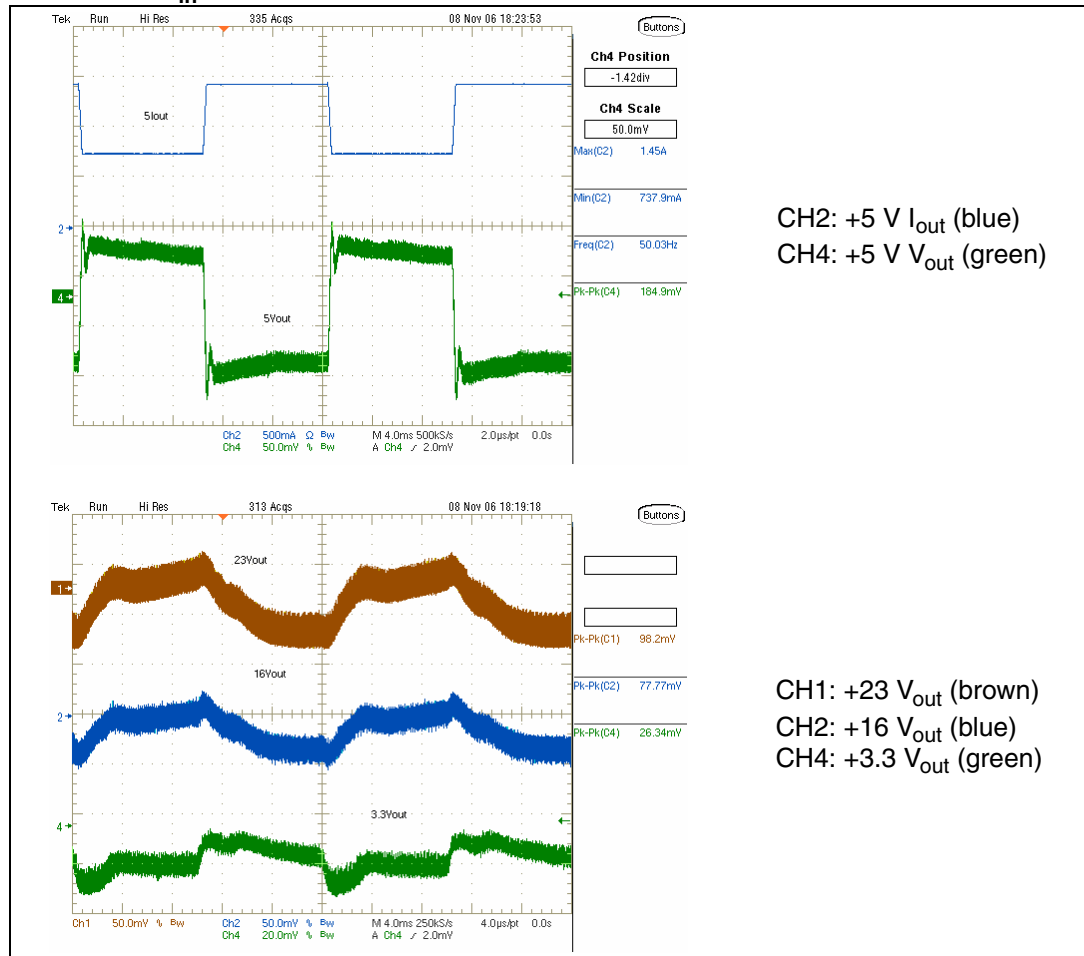


Varying the load on 5 V output, the following results have been obtained:

Table 17. Dynamic load test on 5 V_{out}

Outputs	Load condition
+3.3 V, +12 V, +16 V, +23 V, +33 V, -25 V	Full load
+5 V	Load 50% ÷ 90%

Figure 16. Behavior of outputs with dynamic load applied to 5 V output at $V_{in}=230\text{ V}$



The worst case condition happens when the 3.3 V output load is increased from 50% to 90% of full load value.

3.5 Startup behavior

Figure 17, 18, 19 show the rise slopes at full load of the output voltage at nominal, minimum and maximum input voltage. As shown in the graphs, the rise times are almost constant.

Figure 17. Startup behavior of the system at $V_{in} = 184 V_{rms} - 50 Hz$

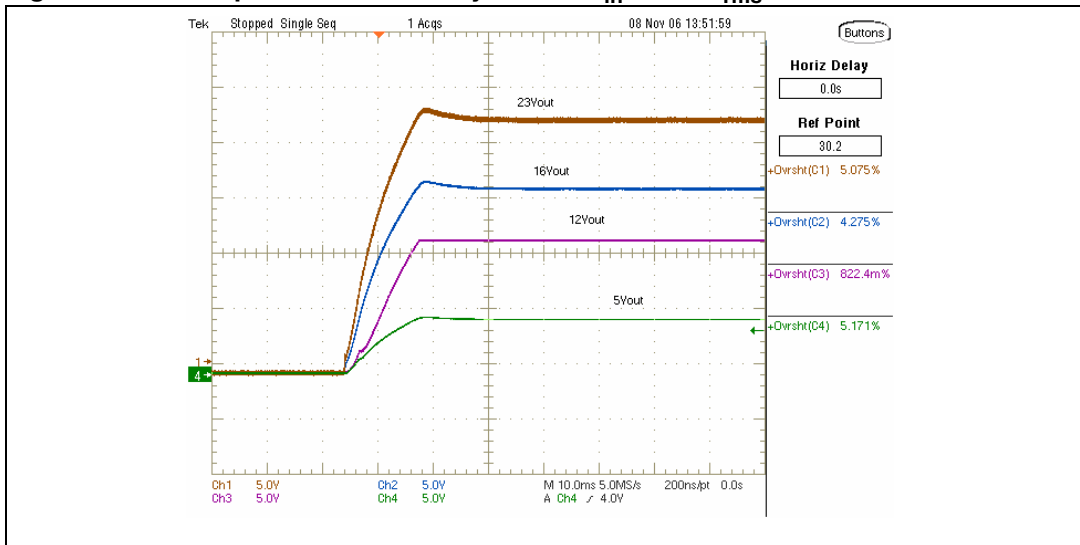


Figure 18. Startup behavior of the system at $V_{in} = 230 V_{rms} - 50 Hz$

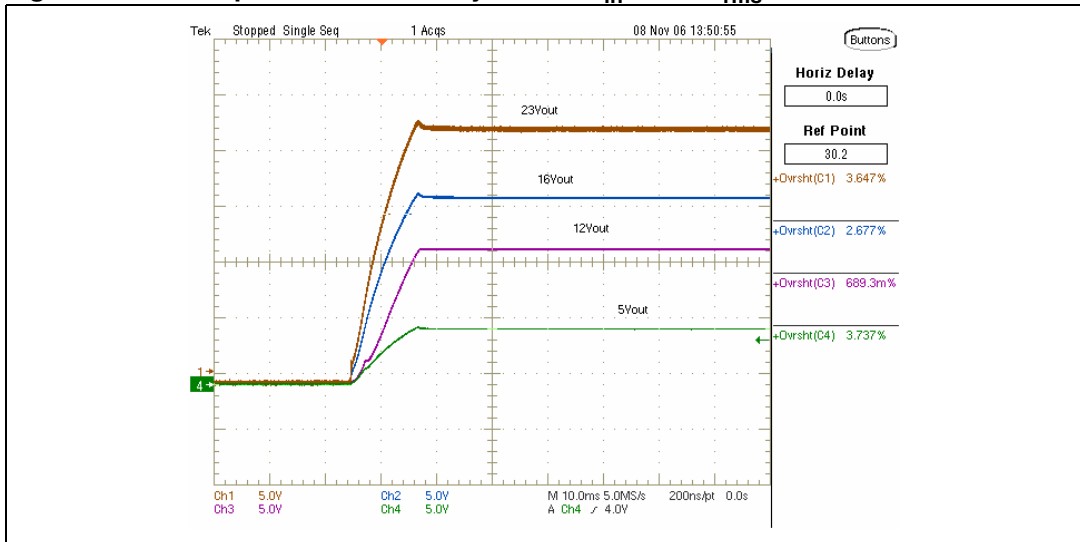
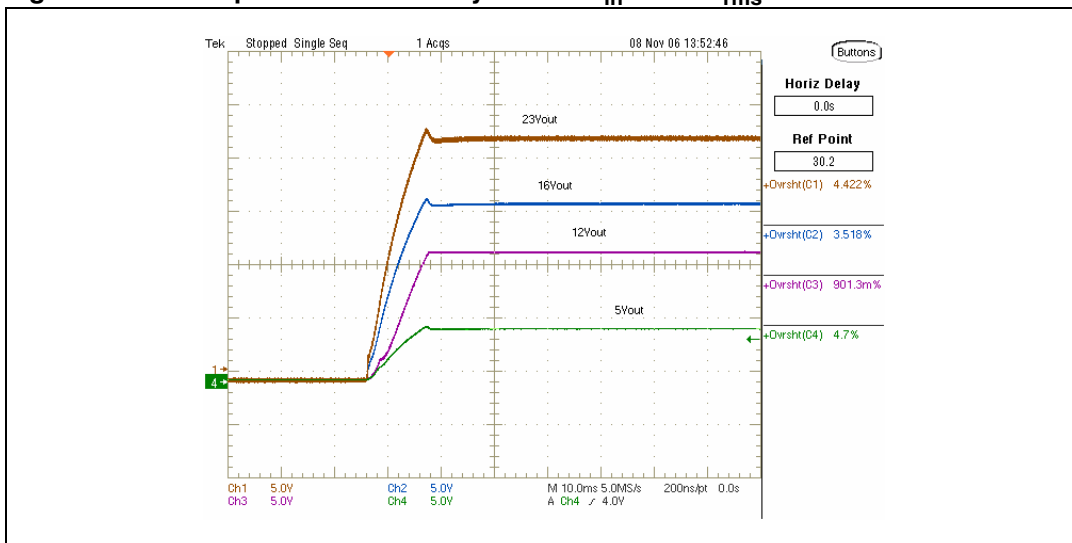


Figure 19. Startup behavior of the system at $V_{in} = 276 V_{rms} - 50 Hz$



Note:
 CH1: +23 V_{out} (brown)
 CH2: +16 V_{out} (blue)
 CH3: +12 V_{out} (purple)
 CH4: +5 V_{out} (green)

Table 18. Overshoot

$V_{in}(V_{ac})$	23 V_{out} (%)	16 V_{out} (%)	12 V_{out} (%)	5 V_{out} (%)
184	5	4.2	0.8	5.1
230	3.6	2.6	0.6	3.7
276	4.2	3.5	0.9	4.7

Table 18 lists the overshoot for the most significant outputs at startup, giving the performances of the power supply in terms of stability. All voltages are well controlled.

3.6 Wakeup time

Figure 20, 21, 22 show the waveforms at startup with the wakeup time measurement at the minimum, nominal and maximum input mains. Obviously, due to the circuitry characteristics, the wakeup time is constant and independent from the input voltage. The measured value is about 0.9 s, according to the IC startup high voltage current generator.

Figure 20. Wakeup behavior of the system at $V_{in} = 184 V_{rms} - 50 Hz$

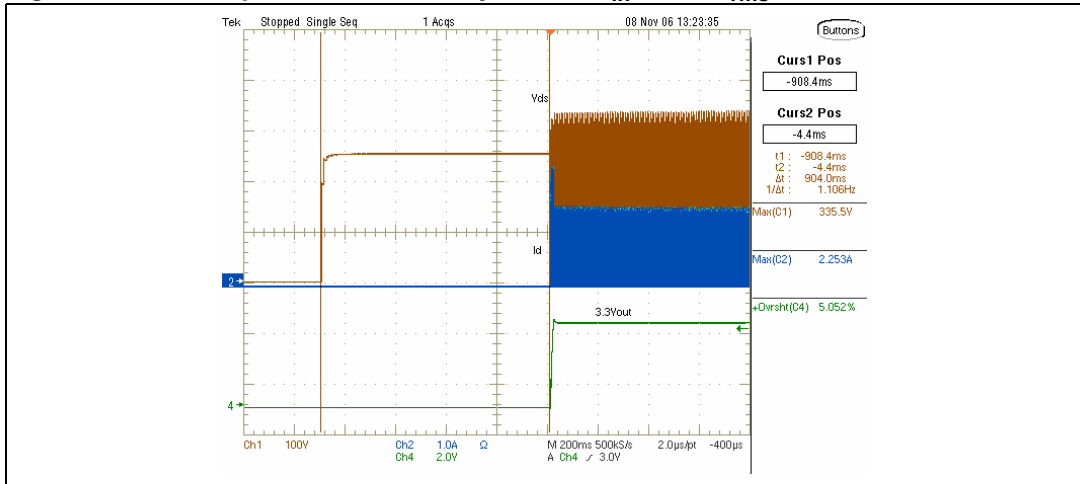


Figure 21. Wakeup behavior of the system at $V_{in} = 230 V_{rms} - 50 Hz$

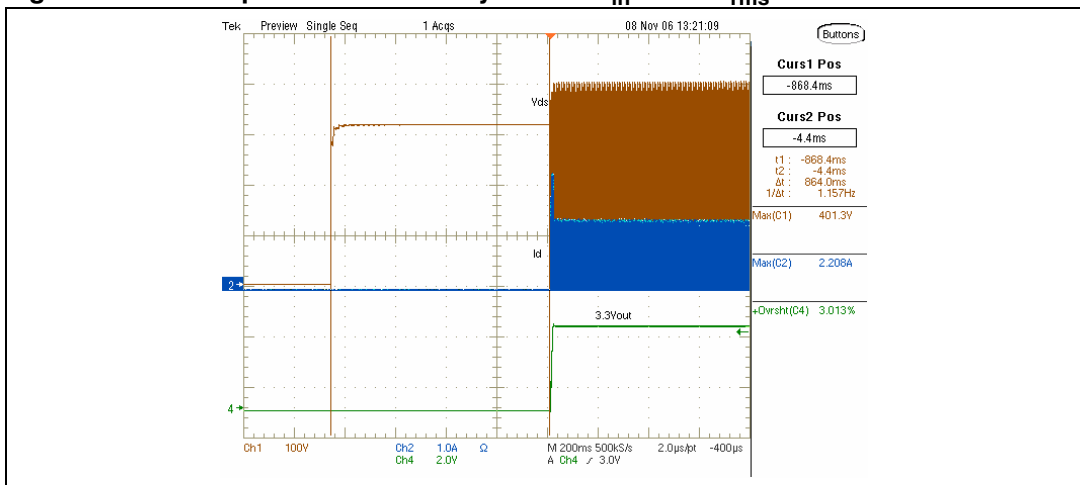
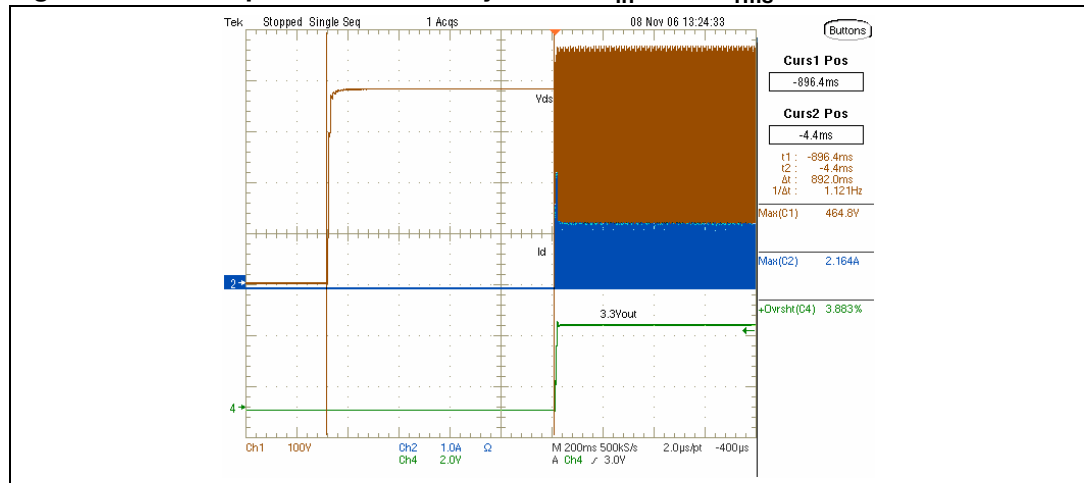


Figure 22. Wakeup behavior of the system at $V_{in} = 276 V_{rms} - 50 Hz$



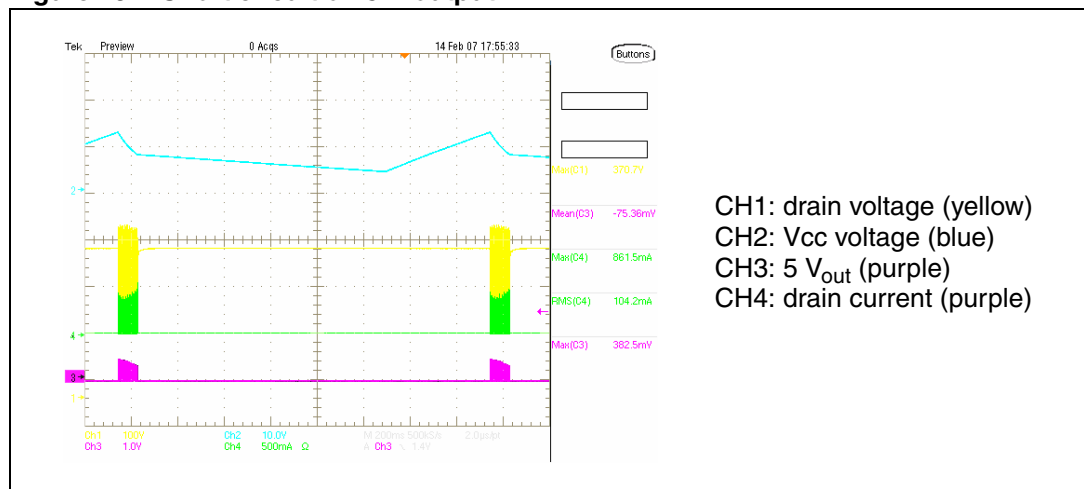
- Note:
- CH1: drain voltage (brown)
 - CH2: drain current (blue)
 - CH4: +3.3 V_{out}
 - $V_{in} (V_{ac})$: 184 - 230 - 276
 - $V_{dsmax} (V)$: 335 - 401 - 465
 - I_{dpk} : 2.25 - 2.2 - 2.16

3.7 Short circuit test

The short circuit tests have been performed on the two regulated voltages. The short circuit has been provided by means of the electronic load, which is able to emulate the "soft" short circuit that could happen on the STB main board. The tests have been done at nominal input voltage with all outputs at full load.

The protection against short circuit on the +12 V is given by the protection of the voltage regulator.

Figure 23. Short circuit on 5 V output



- CH1: drain voltage (yellow)
- CH2: Vcc voltage (blue)
- CH3: 5 V_{out} (purple)
- CH4: drain current (purple)

As the coupling between the 3.3 V and the auxiliary windings is poor, to help the SMPS to enter hiccup mode in case of 3.3 V output shorted, the circuitry based on Q10 and Q11 has been added.

3.8 Conducted emission (EMI) measurements

Conducted emissions measurements at full load and nominal mains voltage have been performed, using a 50 Ω LISN and a spectrum analyzer with peak detector as shown in [Figure 24](#) and [25](#). The emissions are below the limits given by the EN55022 standard for CLASS B equipment. As the margin between the limits and emission is acceptable, the power supply is ready for the final compliance test.

Figure 24. Conducted emissions of the system at full load and $V_{in}=230\text{ V}$ - phase conducted emission

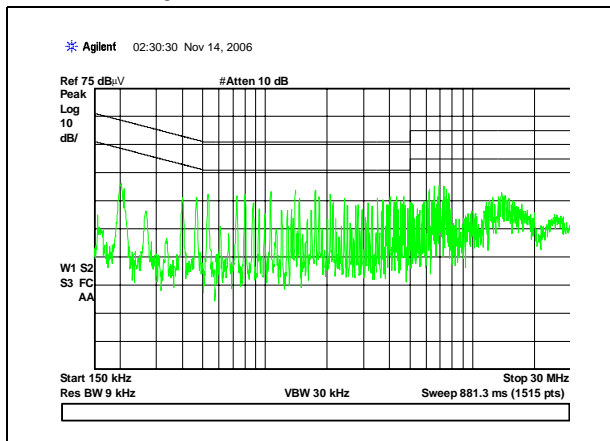
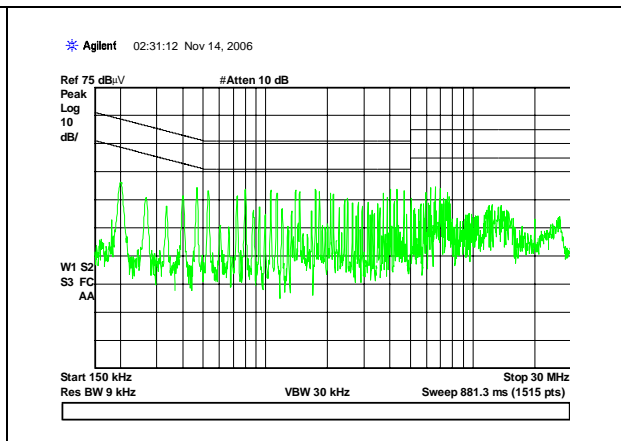


Figure 25. Conducted emissions of the system at full load and $V_{in}=230\text{ V}$ - neutral conducted emission



3.9 Thermal measurements

In order to check the reliability of the design, thermal measurements using a thermocouple have been performed. [Table 19](#) and [Table 20](#) list the thermal measurements at nominal input voltage at ambient temperature (25 °C) for the most critical components under full load.

Table 19. Thermal behavior of the components at primary side

	STP5NK60ZFP case (°C)	STP5NK60ZFP heatsink (°C)	Trafo core (°C)	Trafo windings (°C)	Snubber resistor (°C)
After 30 min	66	57	43	50	60
After 1 hour	72	63	49	50	65

Table 20. Thermal behavior of the components at secondary side

	D55 case (°C)	D54 case (°C)	U5 case (°C)	U5 heatsink (°C)	C102 (°C)
After 30 min	58	69	79	64	61
After 1 hour	63	71	81	68	65

4 Conclusions

A 55 W SMPS for terrestrial and satellite DVB based on 7100 chipset has been designed and fully validated, resulting in an efficient, reliable, and cost-effective system.

The power supply is based on the L6668 controller with integrated high voltage startup circuit, which provides high efficiency also in standby and light load conditions, thanks to its dedicated functions related to "STBY" and "SKIPADJ" pins.

5 Revision history

Table 21. Document revision history

Date	Revision	Changes
17-Jan-2008	1	Initial release

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