

NCP382

Fixed Current-Limiting Power-Distribution Switches

The NCP382 is a single input dual outputs high side power-distribution switch designed for applications where heavy capacitive loads and short-circuits are likely to be encountered. The device includes an integrated 80 mΩ, P-channel MOSFET. The device limits the output current to a desired level by switching into a constant-current mode when the output load exceeds the current-limit threshold or a short is present. The current-limit threshold is internally fixed. The power-switches rise and fall times are controlled to minimize current ringing during switching.

The $\overline{\text{FLAG}}$ logic output asserts low during overcurrent or overtemperature conditions. The switch is controlled by a logic enable input active high or low.

Features

- 2.5 V – 5.5 V Operating Range
- 80 mΩ High-Side MOSFET
- Current Limit: Fixed 500 mA, 1 A, 1.5 A and 2 A
- Undervoltage Lock-Out (UVLO)
- Soft-Start Prevents Inrush Current
- Thermal Protection
- Soft Turn-Off
- Enable Active High or Low (EN or $\overline{\text{EN}}$)
- Compliance to IEC61000-4-2 (Level 4)
 - ◆ 8.0 kV (Contact)
 - ◆ 15 kV (Air)
- UL Listed for SOIC package (NCP382xDxxxx) – File No. E343275
- IEC60950 – Edition 2 – for SOIC package (NCP382xDxxxx) – Amendments 1 & 2 Certified (CB Scheme)
- These are Pb-Free Devices

Typical Applications

- Laptops
- USB Ports/Hubs
- TVs



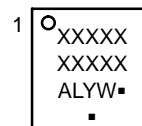
ON Semiconductor®

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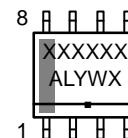
MARKING DIAGRAMS



DFN8 3x3
CASE 506BW



SOIC-8 NB
CASE 751



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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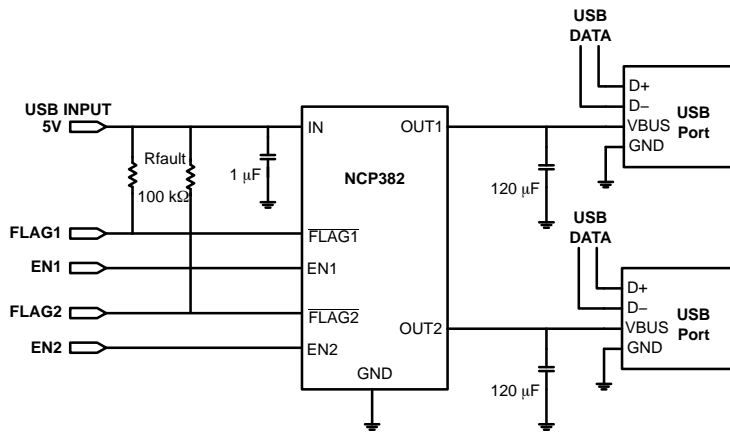


Figure 1. Typical Application Circuit

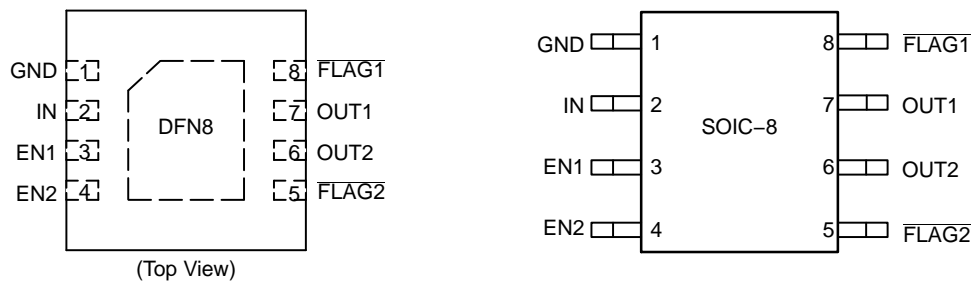


Figure 2. Pin Connections

PIN FUNCTION DESCRIPTION

| Pin Name | Type | Description |
|--------------------|------|--|
| EN1 | I | Enable 1 input, logic low/high (i.e. \overline{EN} or EN) turns on power switch. |
| EN2 | I | Enable 2 input, logic low/high (i.e. \overline{EN} or EN) turns on power switch. |
| GND | P | Ground connection. |
| IN | P | Power-switch input voltage; connect a 1 μ F or greater ceramic capacitor from IN to GND as close as possible to the IC. |
| $\overline{FLAG1}$ | O | Active-low open-drain output 1, asserted during overcurrent or overtemperature conditions. Connect a 10 k Ω or greater resistor pull-up, otherwise leave unconnected. |
| $\overline{FLAG2}$ | O | Active-low open-drain output 2, asserted during overcurrent or overtemperature conditions. Connect a 10 k Ω or greater resistor pull-up, otherwise leave unconnected. |
| OUT1 | O | Power-switch output1; connect a 1 μ F ceramic capacitor from OUT1 to GND, as close as possible to the IC. This minimum value is recommended for USB requirement in terms of load transient response and strong short circuits. |
| OUT2 | O | Power-switch output2; connect a 1 μ F ceramic capacitor from OUT2 to GND, as close as possible to the IC. This minimum value is recommended for USB requirement in terms of load transient response and strong short circuits. |

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MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|--|-------------------|--------------|
| From IN to OUT1, From IN to OUT2 Supply Voltage (Note 1) | $V_{IN}, V_{OUT1}, V_{OUT2}$ | -7.0 to +7.0 | V |
| IN, OUT1, OUT2, EN1, EN2, FLAG1, FLAG2 (Note 1) | $V_{IN}, V_{OUT1}, V_{OUT2}, V_{EN1}, V_{EN2}, V_{FLAG1}, V_{FLAG2}$ | -0.3 to +7.0 | V |
| FLAG1, FLAG2 sink current | I_{SINK} | 1.0 | mA |
| ESD Withstand Voltage (IEC 61000-4-2) (output only, when bypassed with 1.0 μ F capacitor minimum) | ESD IEC | 15 Air, 8 contact | kV |
| Human Body Model (HBM) ESD Rating are (Note 2) | ESD HBM | 2000 | V |
| Machine Model (MM) ESD Rating are (Note 2) | ESD MM | 200 | V |
| Latch-up protection (Note 3) - Pins IN, OUT1, OUT2, FLAG1, FLAG2 - EN1, EN2 | LU | 100 | mA |
| Maximum Junction Temperature (Note 4) | T_J | -40 to + TSD | $^{\circ}$ C |
| Storage Temperature Range | T_{STG} | -40 to + 150 | $^{\circ}$ C |
| Moisture Sensitivity (Note 5) | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- According to JEDEC standard JESD22-A108.
- This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) +/-2.0 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) +/-200 V per JEDEC standard: JESD22-A115 for all pins.
- Latch up Current Maximum Rating: ± 100 mA per JEDEC standard: JESD78 class II.
- A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.

OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------------------|--------------------------------|-----|-----|------|----------------|
| V_{IN} | Operational Power Supply | | 2.5 | | 5.5 | V |
| V_{ENX} | Enable Voltage | | 0 | | 5.5 | |
| T_A | Ambient Temperature Range | | -40 | 25 | +85 | $^{\circ}$ C |
| I_{SINK} | FLAG sink current | | | | 1 | mA |
| C_{IN} | Decoupling input capacitor | | 1 | | | μ F |
| C_{OUTX} | Decoupling output capacitor | USB port per Hub | 120 | | | μ F |
| $R_{\theta JA}$ | Thermal Resistance Junction-to-Air | DFN-8 package (Notes 6 and 7) | | 140 | | $^{\circ}$ C/W |
| | | SOIC-8 package (Notes 6 and 7) | | 210 | | $^{\circ}$ C/W |
| T_J | Junction Temperature Range | | -40 | 25 | +125 | $^{\circ}$ C |
| I_{OUTX} | Recommended Maximum DC current | DFN-8 package | | | 2 | A |
| | | SOIC-8 package | | | 1.5 | A |
| P_D | Power Dissipation Rating (Note 8) | $T_A \leq 25^{\circ}$ C | | | | |
| | | DFN-8 package | 850 | | | mW |
| | | SOIC-8 package | 570 | | | mW |
| | | $T_A = 85^{\circ}$ C | | | | |
| | | DFN-8 package | 428 | | | mW |
| | | SOIC-8 package | 285 | | | mW |

- A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
- The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Announced thermal resistance is the unless PCB dissipation and can be improve with final PCB layout.
- The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

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ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ and T_J up to $+125^{\circ}\text{C}$ for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

POWER SWITCH

| | | | | | | | |
|--------------|--|--|--|-----|------|-----|------------|
| $R_{DS(on)}$ | Static drain-source on-state resistance (SOIC-8 Package) | $T_J = 25^{\circ}\text{C}$, $V_{IN} = 3.6\text{ V to }5\text{ V}$ | | | 80 | 110 | m Ω |
| | | $V_{IN} = 5\text{ V}$ | $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ | | | 140 | |
| $R_{DS(on)}$ | Static drain-source on-state resistance (DFN8 Package) | $T_J = 25^{\circ}\text{C}$, $V_{IN} = 3.6\text{ V to }5\text{ V}$ | | | 80 | 95 | m Ω |
| | | $V_{IN} = 5\text{ V}$ | $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ | | | 100 | |
| T_R | Output rise time | $V_{IN} = 5\text{ V}$ | $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 100\ \Omega$ (Note 9) | 0.3 | 1.0 | 1.5 | ms |
| | | $V_{IN} = 2.5\text{ V}$ | | 0.2 | 0.65 | 1.0 | |
| T_F | Output fall time | $V_{IN} = 5\text{ V}$ | | 0.1 | | 0.5 | |
| | | $V_{IN} = 2.5\text{ V}$ | | 0.1 | | 0.5 | |

ENABLE INPUT ENx OR $\overline{\text{EN}}x$

| | | | | | | |
|-----------|--------------------------|---|------|--|-----|---------------|
| V_{IH} | High-level input voltage | | 1.2 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.4 | V |
| I_{ENx} | Input current | $V_{ENx} = 0\text{ V}$, $\overline{V_{ENx}} = 5\text{ V}$ | -0.5 | | 0.5 | μA |
| T_{ON} | Turn on time | $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 100\ \Omega$ (Note 9) | 1.0 | | 3.0 | ms |
| T_{OFF} | Turn off time | | 1.0 | | 3.0 | ms |

CURRENT LIMIT

| | | | | | | |
|-----------|--|-------------------------------------|-----|------|-----|---------------|
| I_{OCP} | Current-limit threshold (Maximum DC output current I_{OUTX} delivered to load) | $V_{IN} = 5\text{ V}$, Fixed 0.5 A | 0.5 | 0.6 | 0.7 | A |
| | | $V_{IN} = 5\text{ V}$, Fixed 1.0 A | 1.0 | 1.2 | 1.4 | |
| | | $V_{IN} = 5\text{ V}$, Fixed 1.5 A | 1.5 | 1.75 | 2.0 | |
| | | $V_{IN} = 5\text{ V}$, Fixed 2 A | 2 | 2.25 | 2.5 | |
| T_{DET} | Response time to short circuit | $V_{IN} = 5\text{ V}$ | | 2.0 | | μs |
| T_{REG} | Regulation time | | 2.0 | 3.0 | 4.0 | ms |
| T_{OCP} | Over current protection time | | 14 | 20 | 26 | ms |

UNDERVOLTAGE LOCKOUT

| | | | | | | |
|-------------|--------------------------------|----------------------------|-----|------|-----|----|
| V_{UVLO} | IN pin low-level input voltage | V_{IN} rising | 2.0 | 2.35 | 2.5 | V |
| V_{HYST} | IN pin hysteresis | $T_J = 25^{\circ}\text{C}$ | 25 | 40 | 60 | mV |
| T_{RUVLO} | Re-arming Time | V_{IN} rising | 5.0 | 10 | 15 | ms |

SUPPLY CURRENT

| | | | | | | | |
|-------------|----------------------------------|--|--|--|-----|------------|---------------|
| I_{INOFF} | Low-level output supply current | $V_{IN} = 5\text{ V}$, No load on $OUTX$, Device OFF $V_{ENx} = 0\text{ V}$ or $V_{ENx} = 5\text{ V}$ | | | 2.0 | 3.0 | μA |
| I_{INON} | High-level output supply current | 0.5 A | $T_J = 25^{\circ}\text{C}$ $T_J = 85^{\circ}\text{C}$ | | | 95 100 | μA |
| | | 1 and 1.5 A | $T_J = 25^{\circ}\text{C}$ $T_J = 85^{\circ}\text{C}$ | | | 115 125 | |
| | | 2 A | $T_J = 25^{\circ}\text{C}$ $T_J = 85^{\circ}\text{C}$ | | | 130 140 | |
| I_{REV} | Reverse leakage current | $V_{OUTX} = 5\text{ V}$, $V_{IN} = 0\text{ V}$ | $T_J = 25^{\circ}\text{C}$ | | 1.0 | 2.0 | μA |

FLAG PIN

| | | | | | | |
|------------|--|--|---|------|-----|---------------|
| V_{OL} | $\overline{\text{FLAGX}}$ output low voltage | $I_{\overline{\text{FLAGX}}} = 1\text{ mA}$ | | | 400 | mV |
| I_{LEAK} | Off-state leakage | $V_{\overline{\text{FLAGX}}} = 5\text{ V}$ | | 0.02 | 1 | μA |
| T_{FLG} | $\overline{\text{FLAGX}}$ deglitch | $\overline{\text{FLAGX}}$ de-assertion time due to overcurrent | 4 | 6 | 9 | ms |
| T_{FOCP} | $\overline{\text{FLAGX}}$ deglitch | $\overline{\text{FLAGX}}$ assertion due to overcurrent | 6 | 8 | 12 | ms |

THERMAL SHUTDOWN

| | | | | | | |
|-------------|---------------------------------------|--|--|-----|--|--------------------|
| T_{SD} | Thermal shutdown threshold | | | 140 | | $^{\circ}\text{C}$ |
| T_{SDOCP} | Thermal regulation threshold | | | 125 | | $^{\circ}\text{C}$ |
| T_{RSD} | Thermal regulation rearming threshold | | | 115 | | $^{\circ}\text{C}$ |

9. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the $OUTX$ pin with respect to the ground.

10. DFN package only.

11. Guaranteed by characterization.

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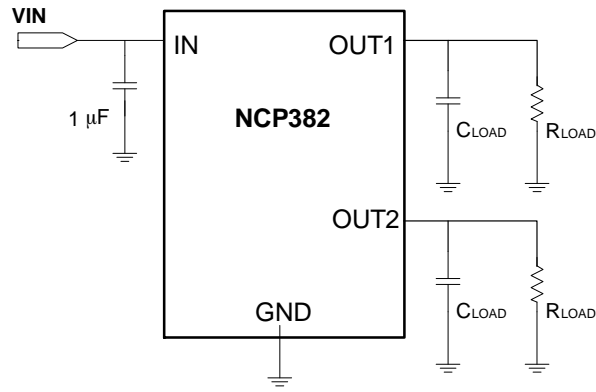


Figure 3. Test Configuration

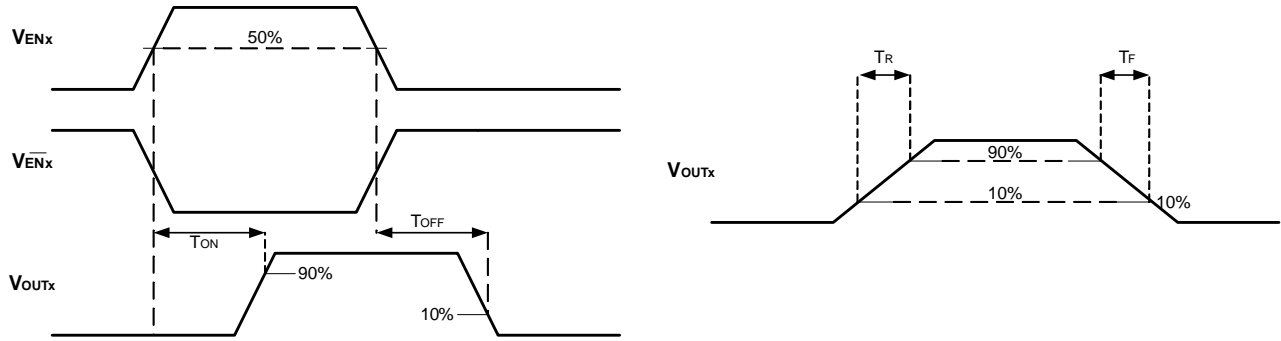


Figure 4. Voltage Waveform

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BLOCK DIAGRAM

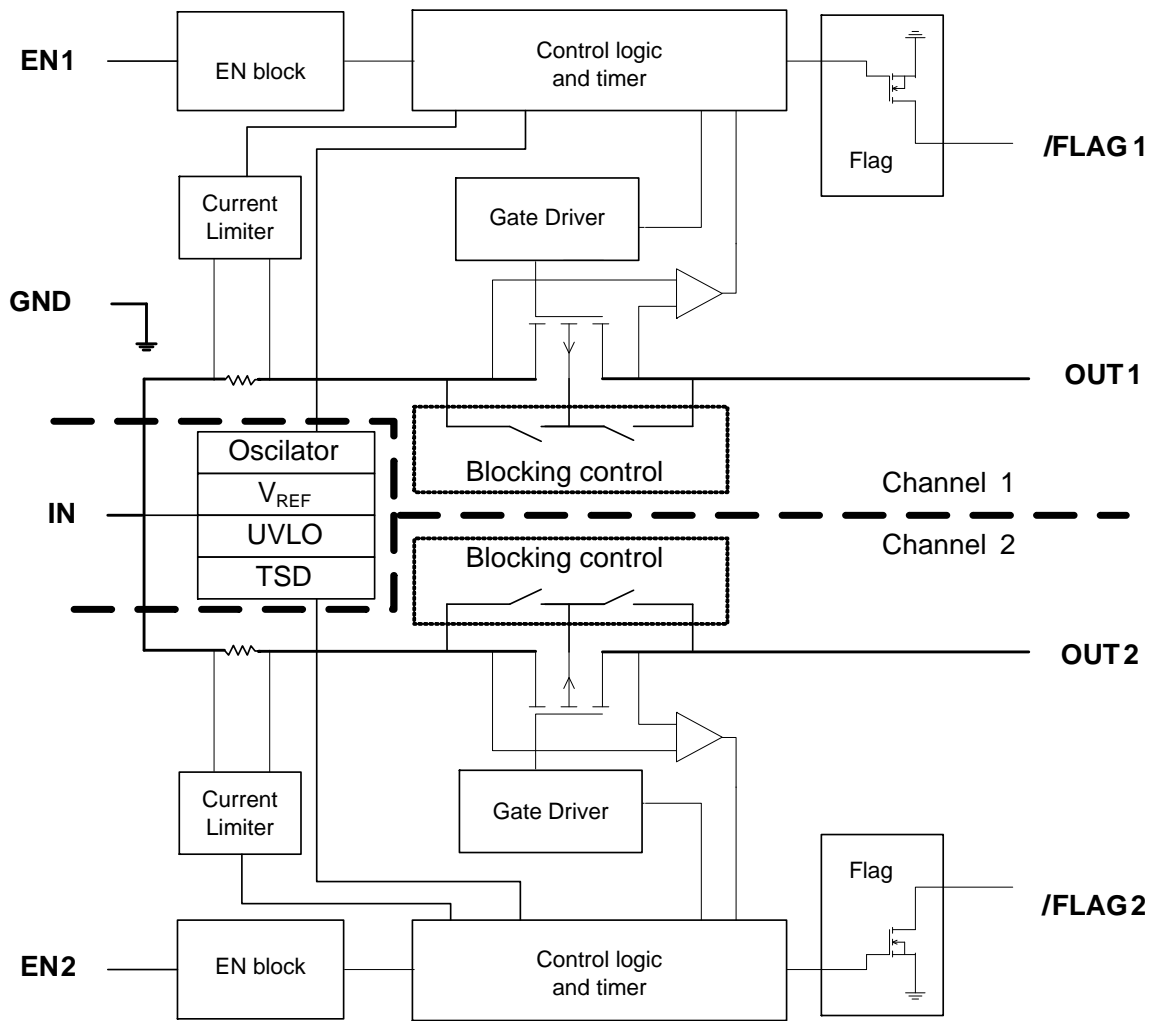


Figure 5. Block Diagram

FUNCTIONAL DESCRIPTION

Overview

The NCP382 is a dual high side power distribution switches designed to protect the input supply voltage in case of heavy capacitive loads, short circuit or over current. In addition, the high side MOSFETs are turned off during undervoltage or thermal shutdown condition. Thanks to the soft start circuitry, NCP382 is able to limit large current and voltage surges.

Overcurrent Protection

NCP382 switches into a constant current regulation mode when the output current is above the I_{OCP} threshold. Depending on the load, the output voltage is decreased accordingly.

- In case of hot plug with heavy capacitive load, the output voltage is brought down to the capacitor voltage. The NCP382 will limit the current to the I_{OCP} threshold value until the charge of the capacitor is completed.

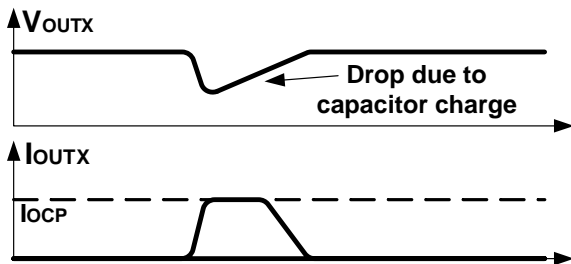


Figure 6. Heavy Capacitive Load

- In case of overload, the current is limited to the I_{OCP} value and the voltage value is reduced according to the load by the following relation:

$$V_{OUTX} = R_{LOAD2} \times I_{OCP} \quad (eq. 1)$$

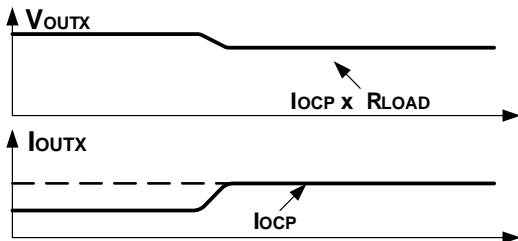


Figure 7. Overload

- In case of short circuit or huge load, the current is limited to the I_{OCP} value within T_{DET} time until the short condition is removed. If the output remains shorted or tied to a very low voltage, the junction temperature of the chip exceeds T_{SDOCP} value and the device enters in thermal shutdown (MOSFET is turned-off).

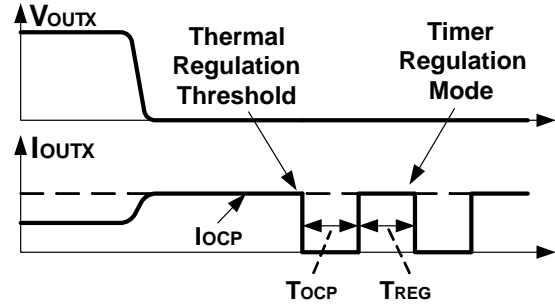


Figure 8. Short-Circuit

Then, the device enters in timer regulation mode, described in 2 phases:

- Off-phase: Power MOSFET is off during T_{OCP} to allow the die temperature to drop.
- On-phase: regulation current mode during T_{REG} . The current is regulated to the I_{OCP} level.

The timer regulation mode allows the device to handle high thermal dissipation (in case of short circuit for example) within temperature operating condition.

NCP382 stays in on-phase/off-phase loop until the over current condition is removed or enable pin is toggled.

Remark: other regulation modes can be available for different applications. Please contact our On Semiconductor representative for availability.

FLAG Indicator

The \overline{FLAG} pin is an open-drain MOSFET asserted low during overcurrent or overtemperature conditions. When an overcurrent fault is detected on the power path, \overline{FLAG} pin is asserted low at the end of the associate deglitch time (T_{FOCP}). Thanks to this feature, the \overline{FLAG} pin is not tied low during the charge of a heavy capacitive load or a voltage transient on output. The \overline{FLAG} pin remains low until the fault is removed. Then, the \overline{FLAG} pin goes high at the end of T_{FGL} .

Undervoltage Lock-out

Thanks to a built-in under voltage lockout (UVLO) circuitry, the output remains disconnected from input until V_{IN} voltage is above V_{UVLO} . This circuit has a V_{HYST} hysteresis witch provides noise immunity to transient condition.

Thermal Sense

Thermal shutdown turns off the power MOSFET if the die temperature exceeds T_{SD} . A built-in hysteresis prevents the part from turning on until the die temperature cools at $TRSD$.

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Enable Input

Enable pin must be driven by a logic signal (CMOS or TTL compatible) or connected to the GND or VIN. A logic low on $\overline{\text{ENX}}$ or high on ENX turns-on the device. A logic high on $\overline{\text{ENX}}$ or low on ENX turns off device and reduces the current consumption down to I_{INOFF} .

Blocking Control

The blocking control circuitry switches the bulk of the power MOS. When the part is off, the body diode limits the

leakage current I_{REV} from OUTX to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUTX pin. In operating condition, anode of the body diode is connected to OUTX pin and cathode is connected to IN pin preventing the discharge of the power supply.

APPLICATION INFORMATION

Power Dissipation

The junction temperature of the device depends on different contributing factors such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{\text{DS(on)}} \times \left((I_{\text{OUT1}})^2 + (I_{\text{OUT2}})^2 \right) \quad (\text{eq. 2})$$

| | |
|-----------------------|---|
| P_D | = Power dissipation (W) |
| $R_{\text{DS(on)}}$ | = Power MOSFET on resistance (Ω) |
| I_{OUTx} | = Output current in channel X (A) |
| | $T_J = P_D \times R_{\theta\text{JA}} + T_A \quad (\text{eq. 3})$ |
| T_J | = Junction temperature ($^{\circ}\text{C}$) |
| $R_{\theta\text{JA}}$ | = Package thermal resistance ($^{\circ}\text{C}/\text{W}$) |
| T_A | = Ambient temperature ($^{\circ}\text{C}$) |

Power dissipation in regulation mode can be calculated by taking into account the drop $V_{\text{IN}} - V_{\text{OUTX}}$ link to the load by the following relation:

$$P_D = \left((V_{\text{IN}} - R_{\text{LOAD1}} \times I_{\text{OCP}}) + (V_{\text{IN}} - R_{\text{LOAD2}} \times I_{\text{OCP}}) \right) \times I_{\text{OCP}} \quad (\text{eq. 4})$$

| | |
|--------------------|---|
| P_D | = Power dissipation (W) |
| V_{IN} | = Input Voltage (V) |
| R_{LOADX} | = Load Resistance on channel X (Ω) |
| I_{OCP} | = Output regulated current (A) |

PCB Recommendations

The NCP382 integrates two PMOS FET rated up to 2 A, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The DFN8 PAD1 must be connected to ground plane to increase the heat transfer if necessary. Of course, in any case, this pad must not connect to any other potential. By increasing PCB area, the $R_{\theta\text{JA}}$ of the package can be decreased, allowing higher current.

NCP382

ORDERING INFORMATION

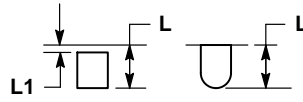
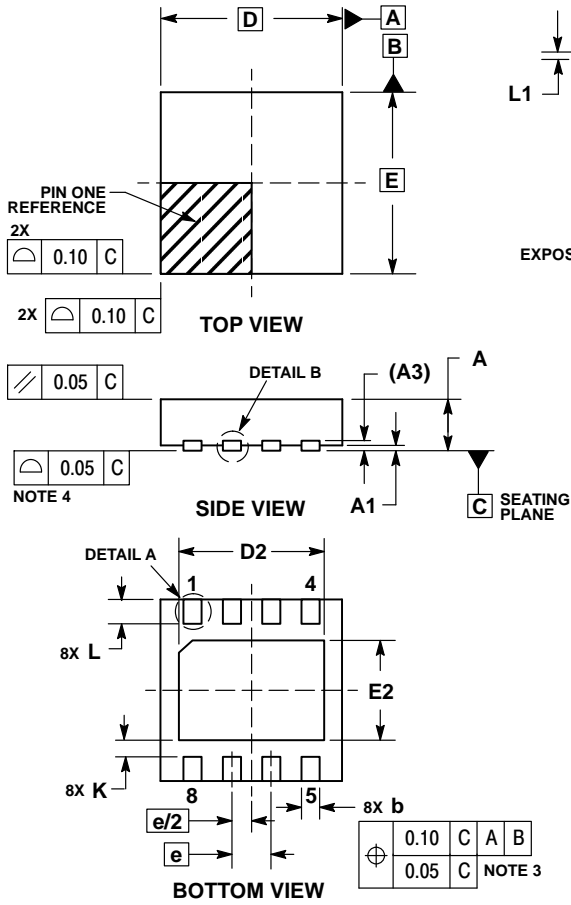
| Device | Marking | Active Enable Level | Over Current Limit | Evaluation Board | UL 236 7 | IEC60950 Ed2 (CB Scheme) | IEC60950 Ed2 Ad1, Ad2 | Package | Shipping† | | |
|-------------------|---------|---------------------|--------------------|-------------------|----------|--------------------------|-----------------------|------------------|--------------------|------------------|--------------------|
| NCP382LMN05-AATXG | 382 L05 | ENx Low | 0.5 A | NCP382LM N05AGEVB | N | N | N | DFN8 (Pb-Free) | 3000 / Tape / Reel | | |
| NCP382LMN10-AATXG | 382 L10 | | 1.0 A | NCP382LM N10AGEVB | N | N | N | | | | |
| NCP382LMN15-AATXG | 382 L15 | | 1.5 A | NCP382LM N15AGEVB | N | N | N | | | | |
| NCP382LMN20-AATXG | 382 L20 | | 2.0 A | NCP382LM N20AGEVB | N | N | N | | | | |
| NCP382HMN05-AATXG | 382 H05 | ENx High | 0.5 A | NCP382HM N05AGEVB | N | N | N | | | SOIC-8 (Pb-Free) | 2500 / Tape / Reel |
| NCP382HMN10-AATXG | 382 H10 | | 1.0 A | NCP382HM N10AGEVB | N | N | N | | | | |
| NCP382HMN15-AATXG | 382 H15 | | 1.5 A | NCP382HM N15AGEVB | N | N | N | | | | |
| NCP382HMN20-AATXG | 382 H20 | | 2.0 A | NCP382HM N20AGEVB | N | N | N | | | | |
| NCP382LD05AA-R2G | 382L05 | ENx Low | 0.5 A | NCP382LD 05AAGEVB | Y | Y | Y | SOIC-8 (Pb-Free) | 2500 / Tape / Reel | | |
| NCP382LD10AA-R2G | 382L10 | | 1.0 A | NCP382LD 10AAGEVB | Y | Y | Y | | | | |
| NCP382LD15AA-R2G | 382L15 | | 1.5 A | NCP382LD 15AAGEVB | Y | Y | Y | | | | |
| NCP382HD05A-AR2G | 382H05 | ENx High | 0.5 A | NCP382HD 05AAGEVB | Y | Y | Y | | | | |
| NCP382HD10A-AR2G | 382H10 | | 1.0 A | NCP382HD 10AAGEVB | Y | Y | Y | | | | |
| NCP382HD15A-AR2G | 382H15 | | 1.5 A | NCP382HD 15AAGEVB | Y | Y | Y | | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

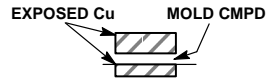
NCP382

PACKAGE DIMENSIONS

DFN8, 3x3, 0.65P
CASE 506BW
ISSUE O



DETAIL A
OPTIONAL
CONSTRUCTIONS



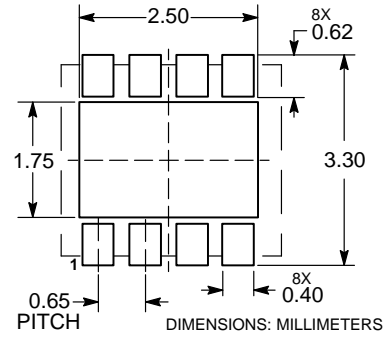
DETAIL B
OPTIONAL
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.25 | 0.35 |
| D | 3.00 BSC | |
| D2 | 2.30 | 2.50 |
| E | 3.00 BSC | |
| E2 | 1.55 | 1.75 |
| e | 0.65 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |
| L1 | 0.00 | 0.15 |

RECOMMENDED SOLDERING FOOTPRINT*

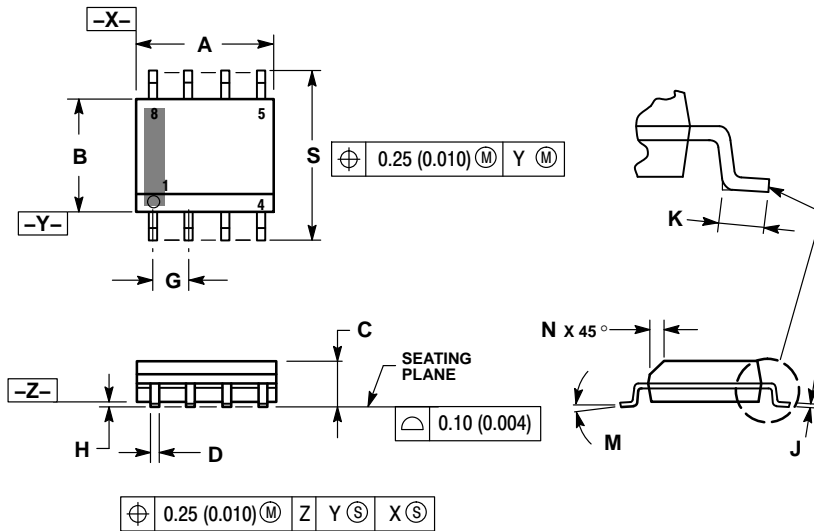


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP382

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

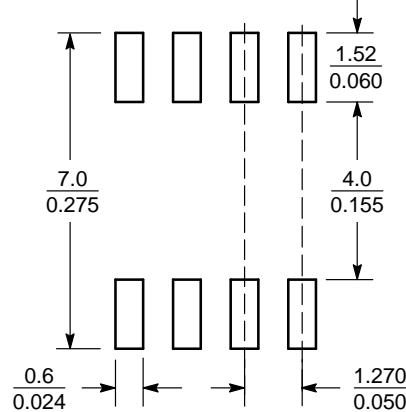


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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