PIC12(L)F1571/2

PIC12(L)F1571/2 Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC12F1571   • PIC12LF1571
- PIC12F1572   • PIC12LF1572

1.0   OVERVIEW

The device can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP method.

1.1   Hardware Requirements

1.1.1   HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for VDD and one for the MCLR/VPP pin.

1.1.2   LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, these devices can be programmed using a single VDD source in the operating range. The MCLR/VPP pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1   Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to VIHH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

> **Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR/VPP pin.
>
> **2:** While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

1.2   Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in Table 1-1.

TABLE 1-1:   PIN DESCRIPTIONS DURING PROGRAMMING FOR PIC12(L)F1571/2

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ICSPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ICSPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
MCLR/VPP	Program/Verify mode	P[1]	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

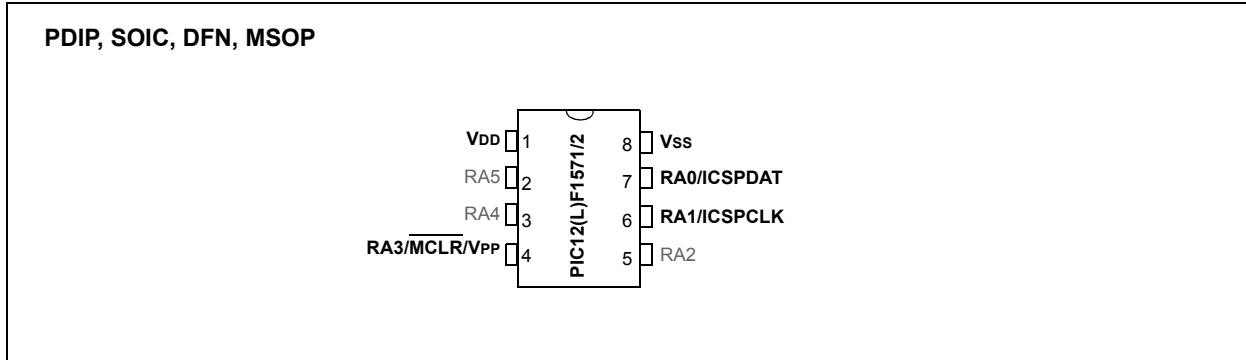**Legend:** I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current.

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2.0   DEVICE PINOUTS

The pin diagram for the PIC12(L)F1571/2 family is shown in Figure 2-1. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagram.
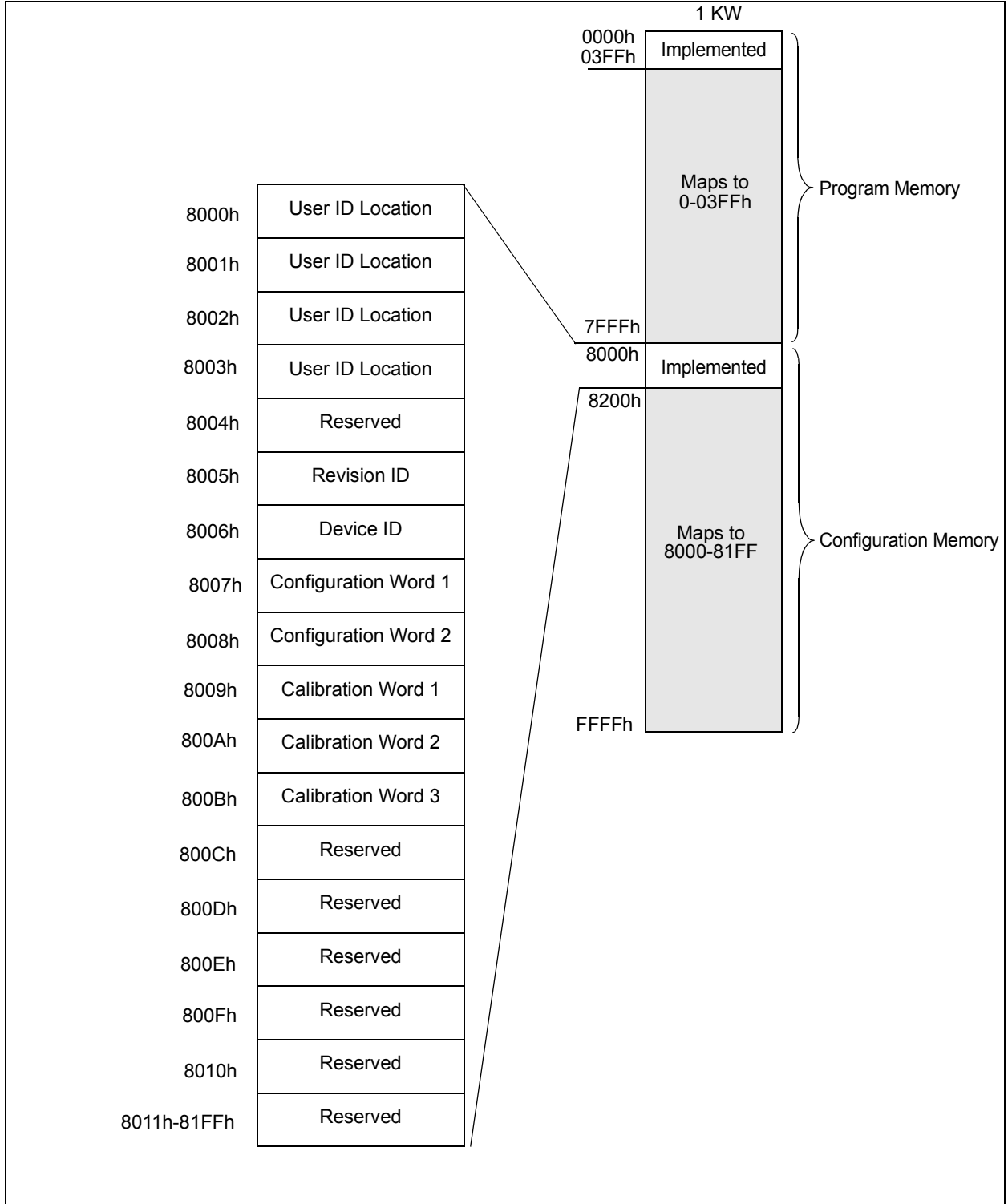
FIGURE 2-1:   8-PIN DIAGRAM FOR PIC12(L)F1571/2

PDIP, SOIC, DFN, MSOP

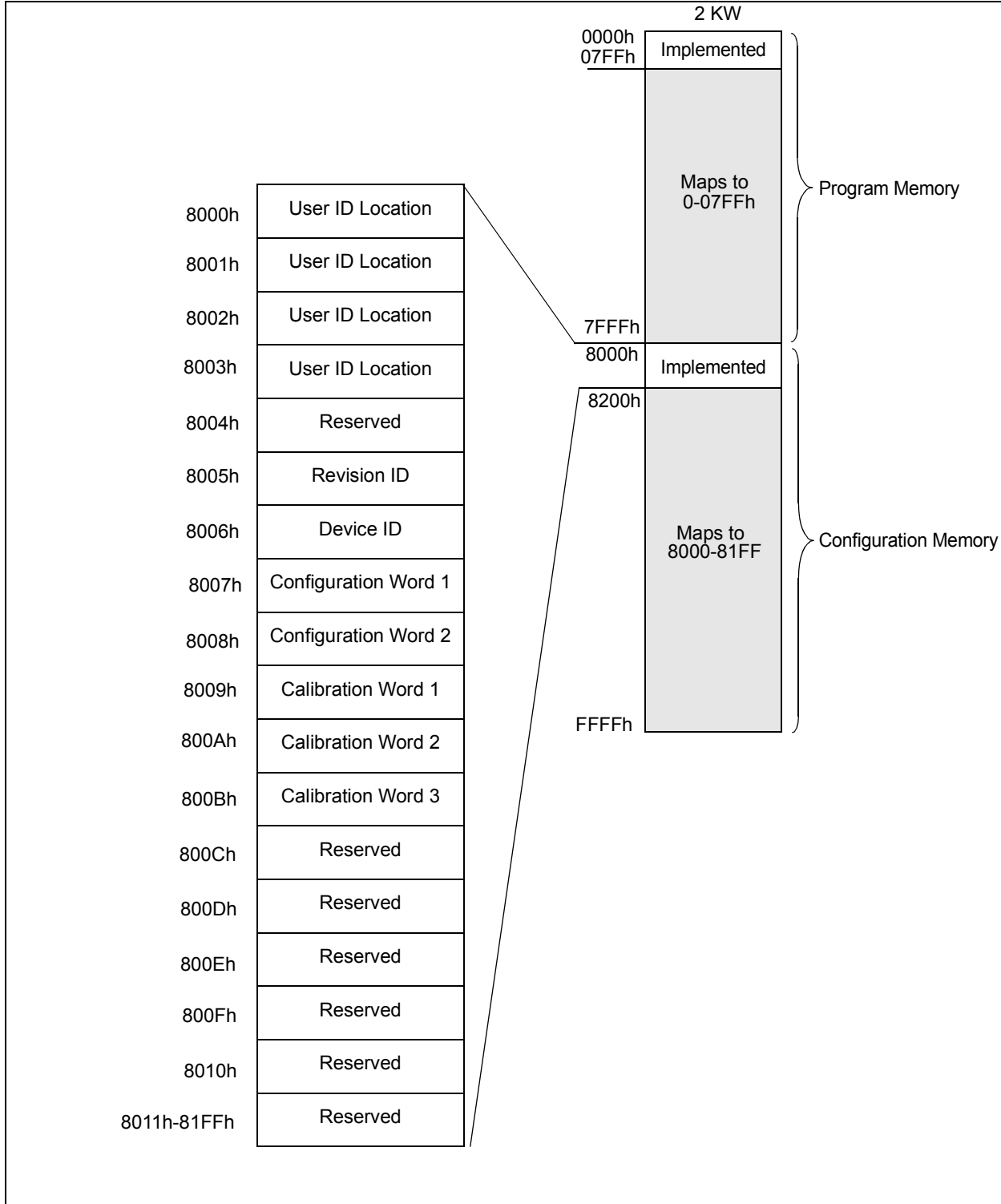|	PIC12(L)F1571/2	
V$_{DD}$ ▯ 1		8 ▯ V$_{SS}$
RA5 ▯ 2		7 ▯ **RA0/ICSPDAT**
RA4 ▯ 3		6 ▯ **RA1/ICSPCLK**
RA3/MCLR/V$_{PP}$ ▯ 4		5 ▯ RA2

3.0   MEMORY MAP

The memory is broken into two sections: program memory and configuration memory.

FIGURE 3-1:   PIC12(L)F1571 PROGRAM MEMORY MAPPING

PIC12(L)F1571/2

PIC12(L)F1572 PROGRAM MEMORY MAPPING

3.1   User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

> **Note:** MPLAB® IDE only displays the seven Least Significant bits (LSb) of each user ID location; the upper bits are not read. It is recommended that only the seven LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2   Revision ID

The revision ID word is located at 8005h. This location is read-only and cannot be erased or modified.

3.3   Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

3.4   Configuration Words

The device has two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.5   Calibration Words

The internal calibration values are factory-calibrated and stored in the Calibration Word locations. See Figure 3-1 for address information.

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

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REGISTER 3-1: **DEVICEID: DEVICE ID REGISTER**[1]

R	R	R	R	R	R
DEV<13:8>					

bit 13   bit 8

R	R	R	R	R	R	R	R
DEV<7:0>							

bit 7   bit 0

Legend:		
R = Readable bit		
'0' = Bit is cleared	'1' = Bit is set	x = Bit is unknown

bit 13-0   **DEV<13:0>:** Device ID bits

                        Refer to Table 3-1 to determine what these bits will read on which device. A value of 3FFFh is invalid.

Note 1: This location cannot be written.

REGISTER 3-2: **REVISIONID: REVISION ID REGISTER**[1]

R	R	R	R	R	R
REV<13:8>					

bit 13   bit 8

R	R	R	R	R	R	R	R
REV<7:0>							

bit 7   bit 0

Legend:		
R = Readable bit		
'0' = Bit is cleared	'1' = Bit is set	x = Bit is unknown

bit 13-0   **REV<13:0>:** Revision ID bits

                        These bits are used to identify the device revision.

Note 1: This location cannot be written.

TABLE 3-1: **DEVICE ID VALUES**

DEVICE	Device ID	Revision ID
PIC12F1571	3051h	2xxxh
PIC12LF1571	3053h	2xxxh
PIC12F1572	3050h	2xxxh
PIC12LF1572	3052h	2xxxh

REGISTER 3-3: CONFIGURATION WORD 1

U-1	U-1	R/P-1	R/P-1	R/P-1	U-1
—	—	CLKOUTEN	BOREN<1:0>[1]		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1
$\overline{CP}$[2]	MCLRE	$\overline{PWRTE}$[1]	WDTE<1:0>		—	FOSC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13-12   **Unimplemented:** Read as '1'

bit 11   **CLKOUTEN:** Clock Out Enable bit
      1 = OFF - CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin
      0 = ON - CLKOUT function is enabled on CLKOUT pin

bit 10-9   **BOREN<1:0>:** Brown-out Reset Enable bits[1]
      11 = ON   - Brown-out Reset enabled. The SBOREN bit is ignored.
      10 = SLEEP - Brown-out Reset enabled while running and disabled in Sleep. The SBOREN bit is ignored.
      01 = SBODEN - Brown-out Reset controlled by the SBOREN bit in the PCON register
      00 = OFF   - Brown-out Reset disabled. The SBOREN bit is ignored.

bit 8   **Unimplemented:** Read as '1'

bit 7   **$\overline{CP}$:** Flash Program Memory Code Protection bit[2]
      1 = OFF - Code protection off. Program Memory can be read and written.
      0 = ON - Code protection on. Program Memory cannot be read or written externally.

bit 6   **MCLRE:** $\overline{MCLR}$/VPP Pin Function Select bit
      If LVP bit = 1 (ON):
         This bit is ignored. $\overline{MCLR}$/VPP pin function is $\overline{MCLR}$; Weak pull-up enabled.
      If LVP bit = 0 (OFF):
      1 = ON - $\overline{MCLR}$/VPP pin function is $\overline{MCLR}$; Weak pull-up enabled.
      0 = OFF - $\overline{MCLR}$/VPP pin function is digital input; $\overline{MCLR}$ internally disabled; Weak pull-up under control of pin's WPU control bit.

bit 5   **$\overline{PWRTE}$:** Power-up Timer Enable bit[1]
      1 = OFF - PWRT disabled
      0 = ON - PWRT enabled

bit 4-3   **WDTE<1:0>:** Watchdog Timer Enable bit
      11 = ON   - WDT enabled. SWDTEN is ignored.
      10 = SLEEP - WDT enabled while running and disabled in Sleep. SWDTEN is ignored.
      01 = SWDTEN - WDT controlled by the SWDTEN bit in the WDTCON register
      00 = OFF   - WDT disabled. SWDTEN is ignored.

bit 2   **Unimplemented:** Read as '1'

bit 1-0   **FOSC<1:0>:** Oscillator Selection bits
      11 = ECH   - External Clock, High-Power mode: CLKI on OSC1/CLKI
      10 = ECM   - External Clock, Medium-Power mode: CLKI on OSC1/CLKI
      01 = ECL   - External Clock, Low-Power mode: CLKI on OSC1/CLKI
      00 = INTOSC - I/O function on OSC1/CLKI

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
     2: Once enabled, code-protect can only be disabled by bulk erasing the device.

REGISTER 3-4: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
LVP[(1)]	DEBUG[(2)]	LPBOREN	BORV[(3)]	STVREN	PLLEN

bit 13 .... bit 8

U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	WRT<1:0>	

bit 7 .... bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit[(1)]
  `1 = ON` - Low-voltage programming enabled. MCLR/VPP pin function is MCLR. MCLRE Configuration bit is ignored.
  `0 = OFF` - High Voltage on MCLR/VPP must be used for programming

bit 12 **DEBUG:** Debugger Mode bit[(2)]
  `1 = OFF` - In-Circuit Debugger disabled; ICSPCLK and ICSPDAT are general purpose I/O pins.
  `0 = ON` - In-Circuit Debugger enabled; ICSPCLK and ICSPDAT are dedicated to the debugger.

bit 11 **LPBOREN:** Low-Power Brown-out Reset Enable bit
  `1 = OFF` - Low-power Brown-out Reset is disabled
  `0 = ON` - Low-power Brown-out Reset is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit[(3)]
  `1 = LOW` - Brown-out Reset voltage (Vbor), low trip point selected
  `0 = HIGH` - Brown-out Reset voltage (Vbor), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
  `1 = ON`   - Stack Overflow or Underflow will cause a Reset
  `0 = OFF`   - Stack Overflow or Underflow will not cause a Reset

bit 8 **PLLEN:** PLL Enable bit
  `1 = ON`   - 4xPLL enabled
  `0 = OFF`   - 4xPLL disabled

bit 7-2 **Unimplemented:** Read as '1'

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
  2 kW Flash memory: (PIC12F1572):
    `11 = OFF`   - Write protection off
    `10 = BOOT` - 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
    `01 = HALF` - 000h to 3FFh write-protected, 400h to 7FFh may be modified by PMCON control
    `00 = ALL`   - 000h to 7FFh write-protected, no addresses may be modified by PMCON control
  1 kW Flash memory: (PIC12F1571)
    `11 = OFF`   - Write protection off
    `10 = BOOT` - 000h to 0FFh write-protected, 100h to 3FFh may be modified by PMCON control
    `01 = HALF` - 000h to 1FFh write-protected, 200h to 3FFh may be modified by PMCON control
    `00 = ALL`   - 000h to 3FFh write-protected, no addresses may be modified by PMCON control

Note 1: This bit cannot be programmed to '0' when programming mode is entered via LVP.
  2: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.
  3: See Vbor parameter for specific trip point voltages.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high voltage:

- V_{PP} – First entry mode
- V_{DD} – First entry mode

4.1.1 V_{PP} – FIRST ENTRY MODE

To enter Program/Verify mode via the V_{PP}-first method, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has $\overline{MCLR}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{PWRTE}$ = 0), the internal oscillator is selected (FOSC = 100), and RA0 and RA1 are driven by the user application, the device will execute code. Since this may prevent entry, V_{PP}-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 V_{DD} – FIRST ENTRY MODE

To enter Program/Verify mode via the V_{DD}-first method, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V_{DD} or below to V_{IHH}.

The V_{DD}-first method is useful when programming the device when V_{DD} is already applied, for it is not necessary to disconnect V_{DD} to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{MCLR}$ to V_{DD} or lower (V_{IL}). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit of the Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figures 8-8 and 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{MCLR}$ to V_{IL}. See Figures 8-8 and 8-9.

Note:	To enter LVP mode, the LSb of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

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4.3 Program/Verify Commands

These devices implement 13 programming commands, each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of T_{DLY} between the command and the data. After this delay, 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note:	Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

FIGURE 4-1:   LOAD CONFIGURATION
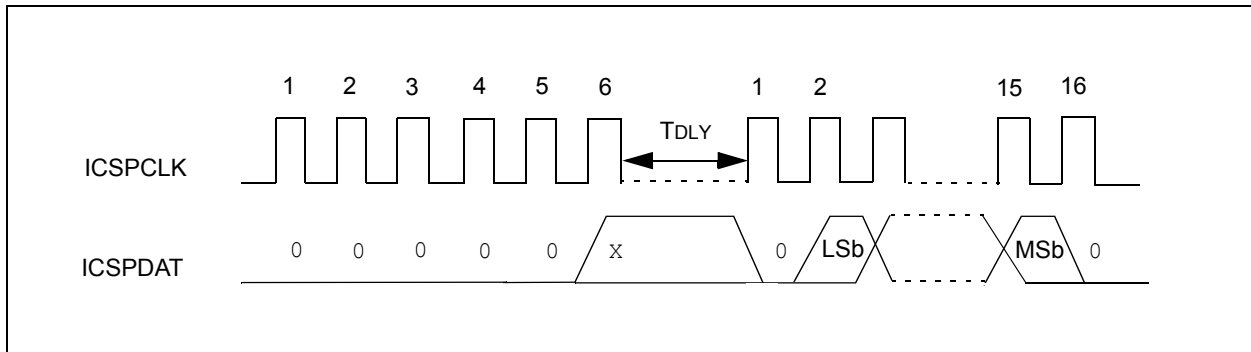
4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

FIGURE 4-2:   LOAD DATA FOR PROGRAM MEMORY
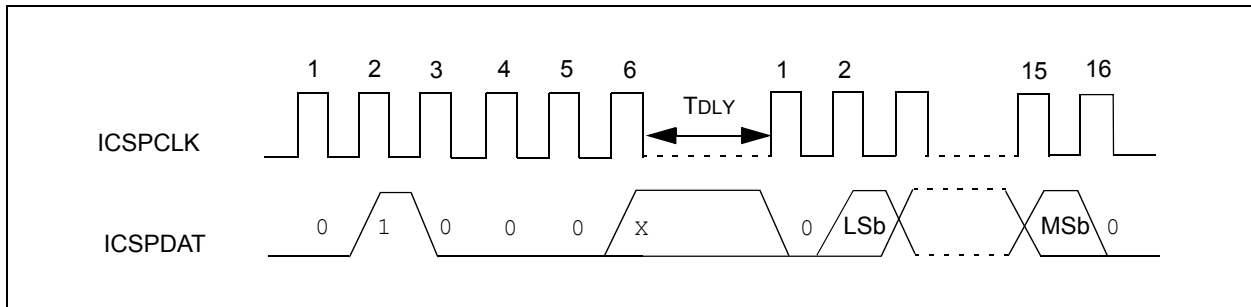
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4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: **READ DATA FROM PROGRAM MEMORY**
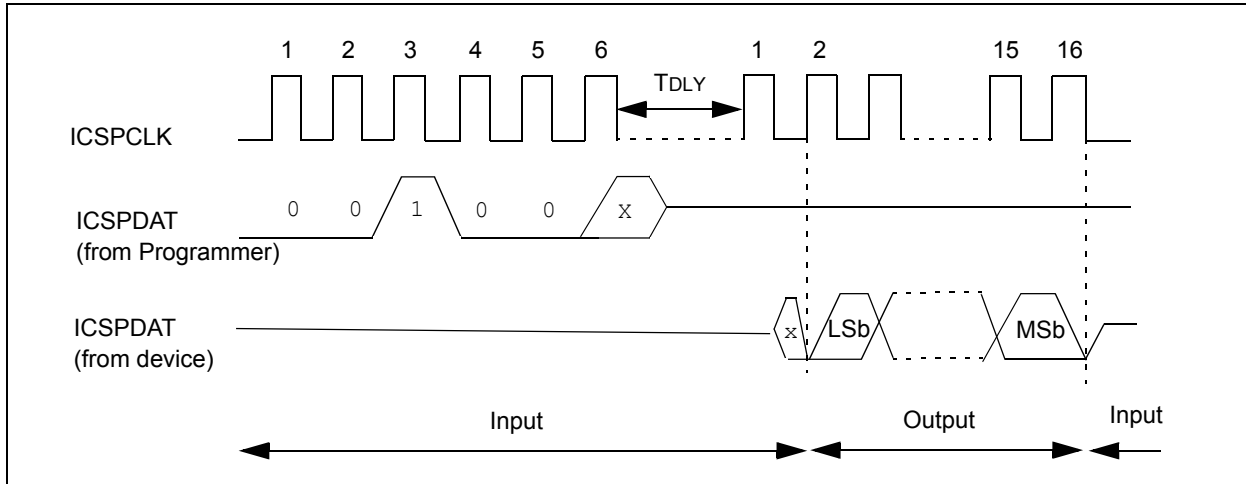
4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it.

If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h (see Figure 4-4).

FIGURE 4-4: **INCREMENT ADDRESS**
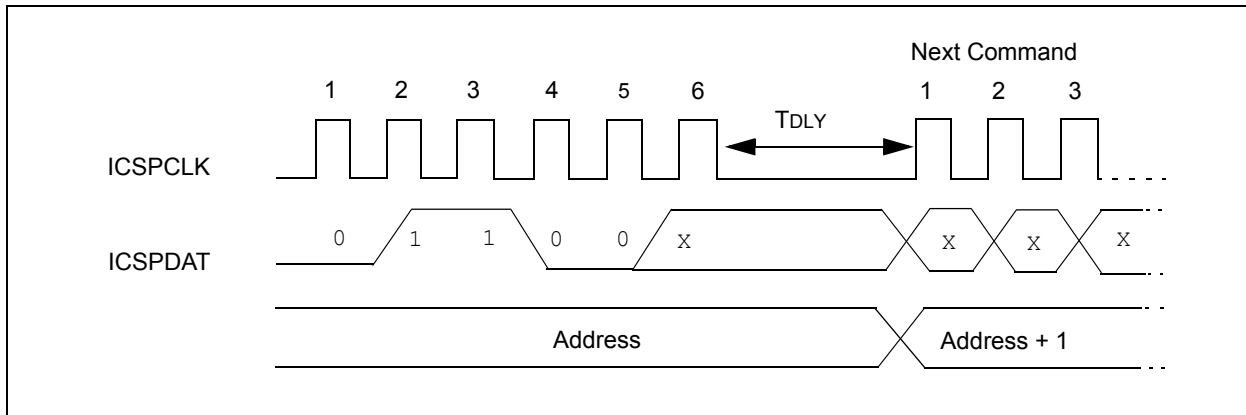
4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory (see Figure 4-5).
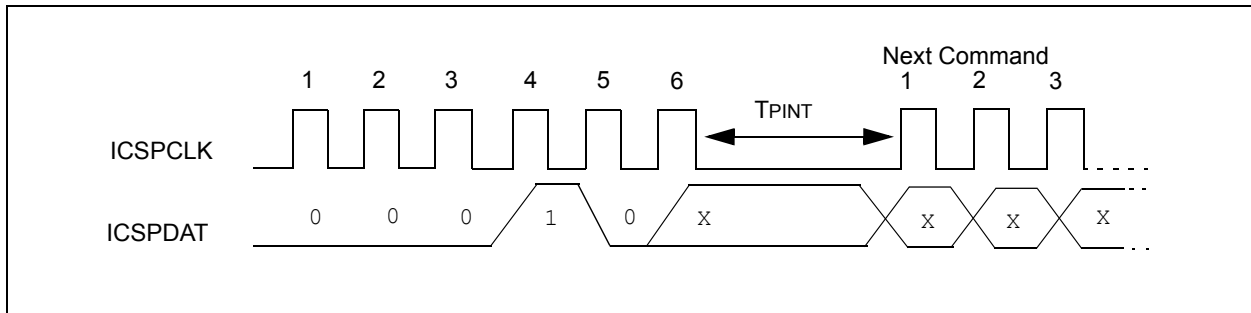
FIGURE 4-5: **RESET ADDRESS**
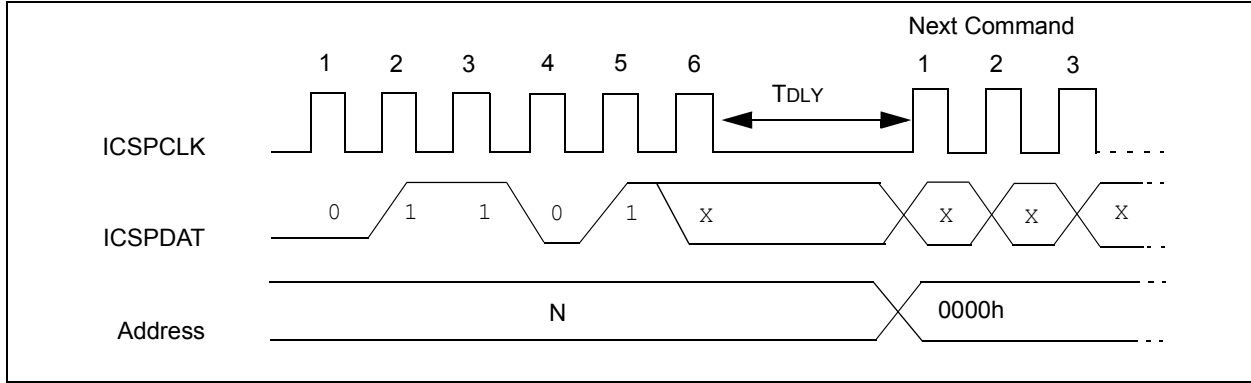
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, T_{PINT}, in order for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed (see Figure 4-6).

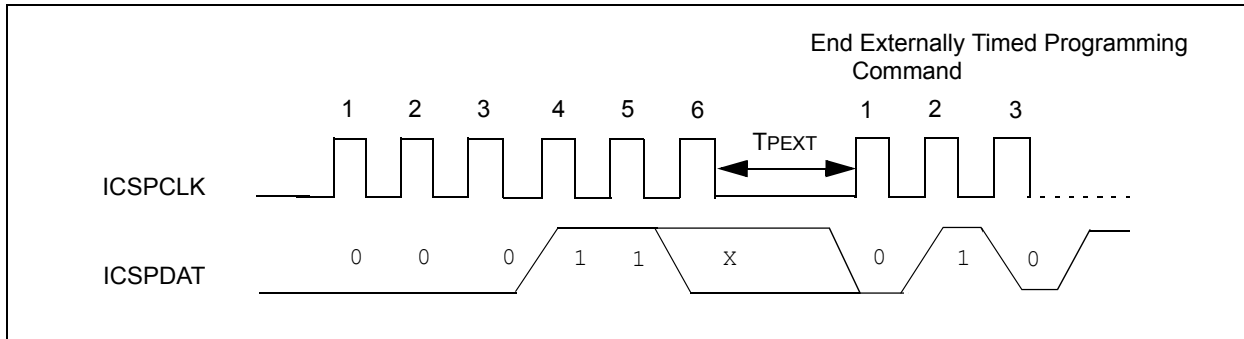**FIGURE 4-6:** **BEGIN INTERNALLY TIMED PROGRAMMING**

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4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: **BEGIN EXTERNALLY TIMED PROGRAMMING**

4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by T_{PEXT} after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (T_{DIS}) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: **END EXTERNALLY TIMED PROGRAMMING**
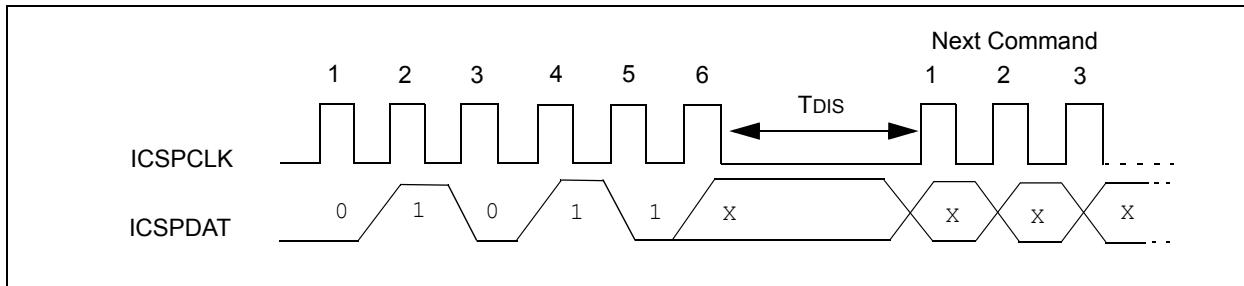
4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

    Program Memory is erased

   Configuration Words are erased

Address 8000h-8008h:

    Program Memory is erased

    Configuration Words are erased

    User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command, the erase will not complete until the time interval, T_{ERAB}, has expired.

> **Note:** The code protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: **BULK ERASE PROGRAM MEMORY**
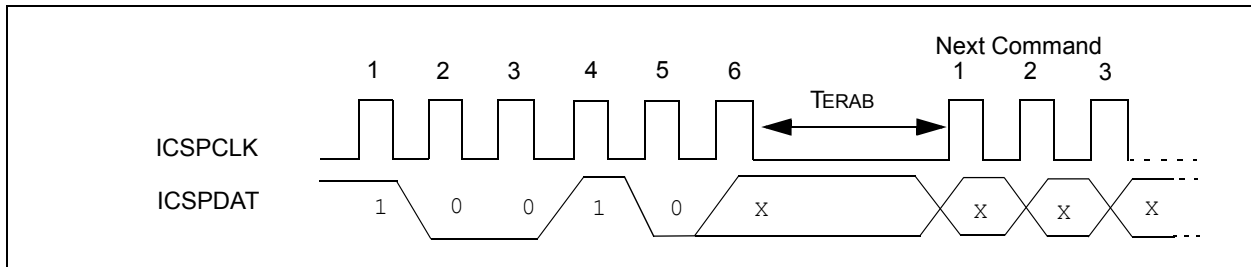
4.3.10 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h, the Row Erase Program Memory command will only erase the user ID locations, regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, T_{ERAR}, has expired (see Figure 4-10).

FIGURE 4-10: **ROW ERASE PROGRAM MEMORY**
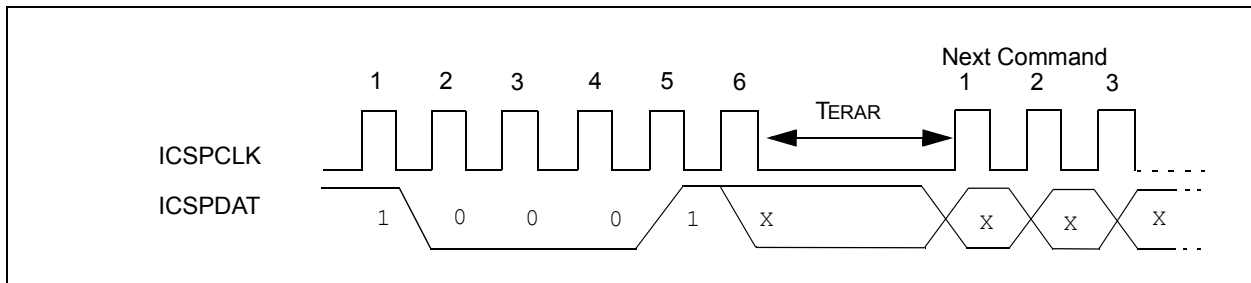
TABLE 4-2: **PROGRAMMING ROW AND LATCH SIZES**

Devices	PC	Erase Row Size (Number of 14-bit Words)	Write Row Size (Number of 14-bit Latches)
PIC12F1571	<15:4>	16	16
PIC12LF1571			
PIC12F1572			
PIC12LF1572			

5.0   PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The lower bits of the address define the data latch addresses and are aligned with the LSbs of the address. The upper bits of the address define the Flash program memory row. The upper bits that define the row address are indicated in Table 4-2.

When the Begin Externally Timed Programming or Begin Internally Timed Programming commands are given, the data contained in the data latches will be programmed into the corresponding addresses of the row specified by the upper bits of the PC. Writes cannot cross a physical row boundary. For example, in a 16-word latch device, attempting to write from address 0002h-0011h will result in data being written to 0010h-001Fh.

If more than the maximum number of latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

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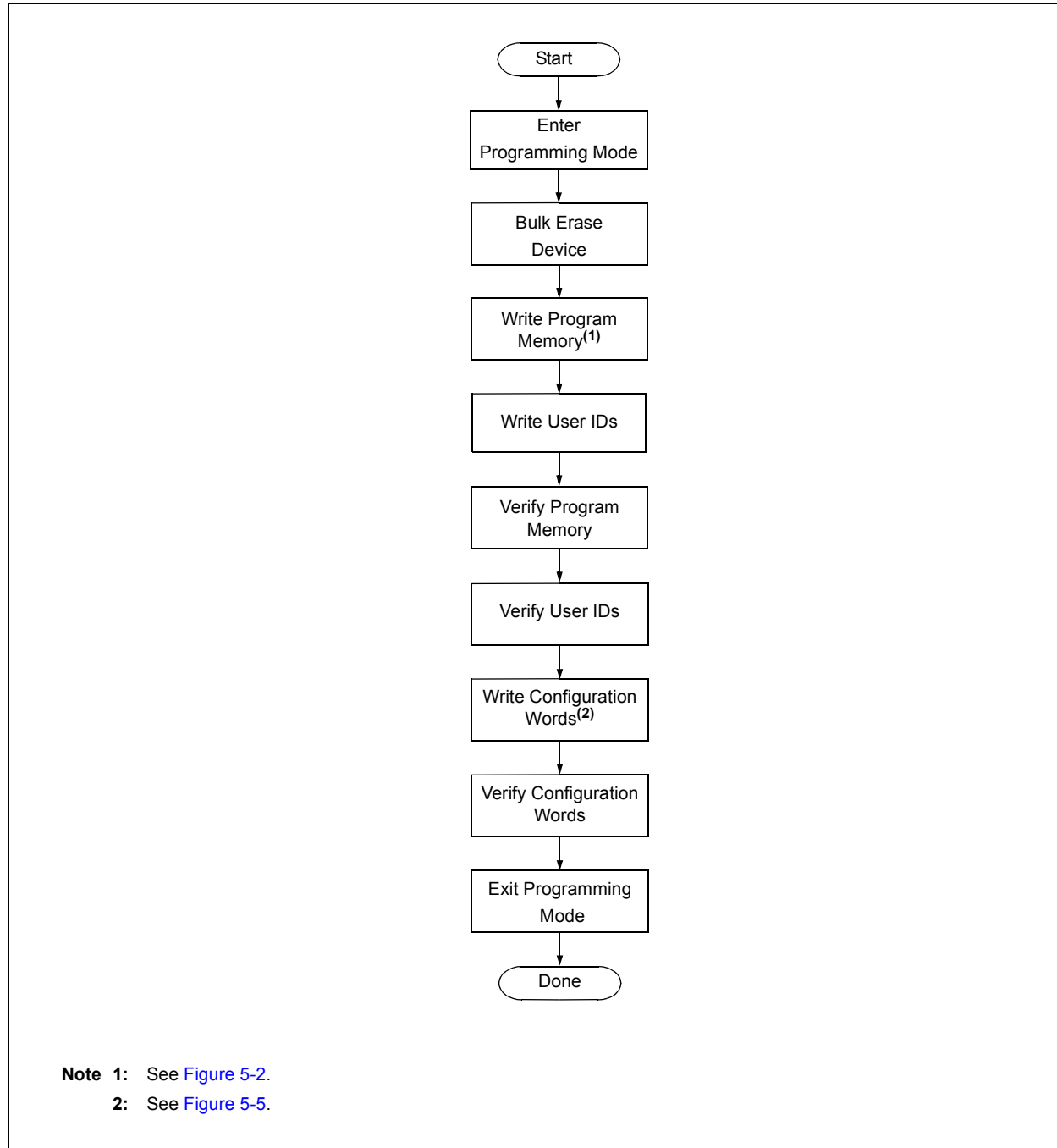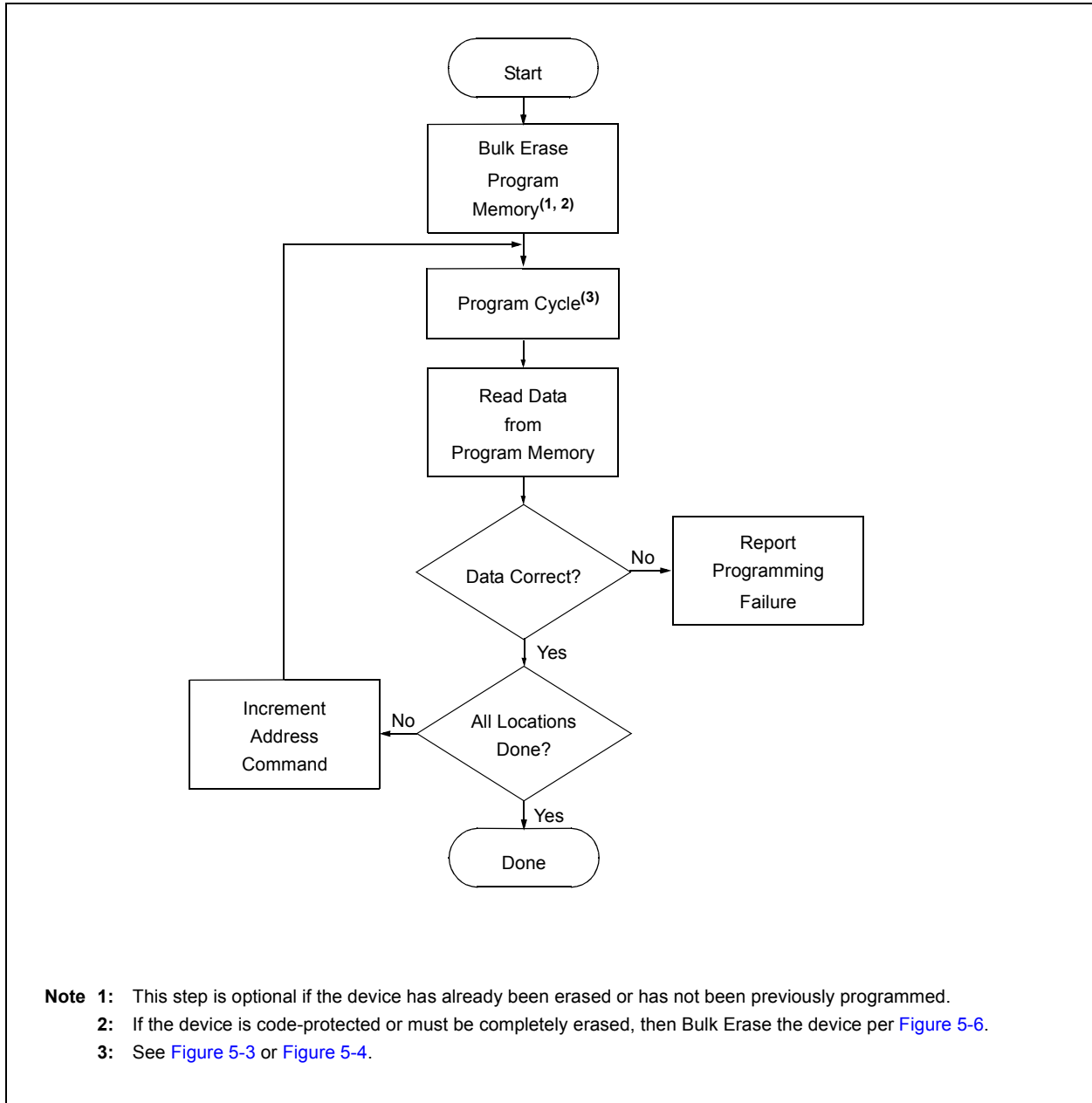**FIGURE 5-1:** DEVICE PROGRAM/VERIFY FLOWCHART

```
                    ( Start )
                        │
                        ▼
              ┌───────────────────┐
              │      Enter         │
              │ Programming Mode   │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │    Bulk Erase      │
              │      Device        │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │  Write Program     │
              │   Memory(1)        │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │   Write User IDs   │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │  Verify Program    │
              │     Memory         │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │  Verify User IDs   │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │Write Configuration │
              │    Words(2)        │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │Verify Configuration│
              │      Words         │
              └───────────────────┘
                        │
                        ▼
              ┌───────────────────┐
              │ Exit Programming   │
              │       Mode         │
              └───────────────────┘
                        │
                        ▼
                    ( Done )
```

Note 1: See Figure 5-2.
   2: See Figure 5-5.

FIGURE 5-2: **PROGRAM MEMORY FLOWCHART**

Note 1: This step is optional if the device has already been erased or has not been previously programmed.
   2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 5-6.
   3: See Figure 5-3 or Figure 5-4.

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FIGURE 5-3:   **ONE-WORD PROGRAM CYCLE**

Program Cycle

```
                    ┌────────────────┐
                    │   Load Data    │
                    │      for       │
                    │ Program Memory │
                    └────────────────┘
                      │            │
          ┌───────────┘            └───────────┐
          ▼                                    ▼
┌──────────────────┐              ┌──────────────────────┐
│      Begin       │              │        Begin         │
│   Programming    │              │     Programming       │
│     Command      │              │      Command          │
│ (Internally timed)│             │ (Externally timed)(1) │
└──────────────────┘              └──────────────────────┘
          │                                    │
          ▼                                    ▼
┌──────────────────┐              ┌──────────────────────┐
│   Wait TPINT     │              │     Wait TPEXT        │
└──────────────────┘              └──────────────────────┘
                                               │
                                               ▼
                                  ┌──────────────────────┐
                                  │        End            │
                                  │    Programming        │
                                  │     Command           │
                                  └──────────────────────┘
                                               │
                                               ▼
                                  ┌──────────────────────┐
                                  │     Wait TDIS         │
                                  └──────────────────────┘
```

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.
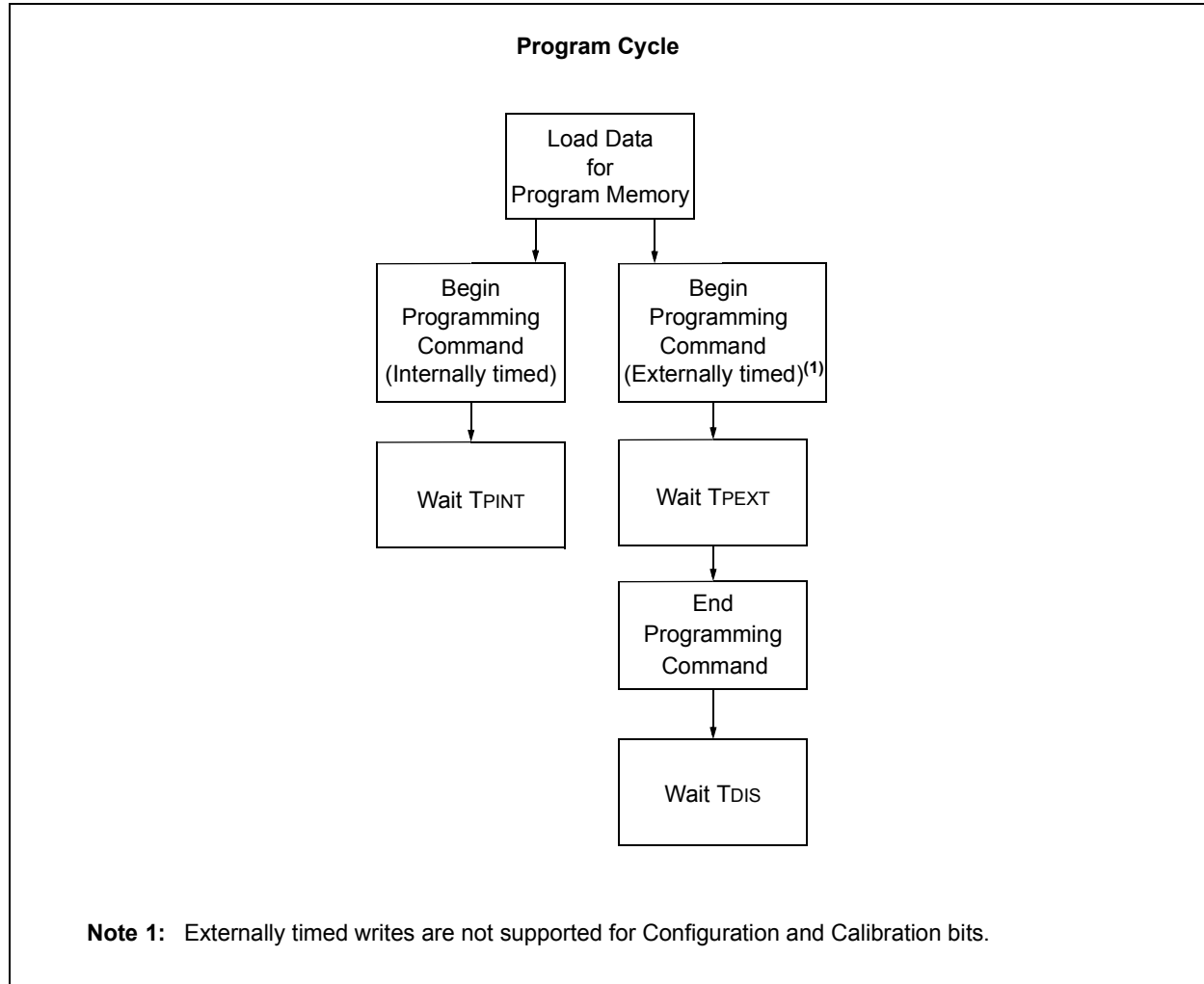
FIGURE 5-4: **MULTIPLE-WORD PROGRAM CYCLE**

Program Cycle

Load Data
for
Program Memory — Latch 1

↓

Increment
Address
Command

↓

Load Data
for
Program Memory — Latch 2

●
●
●

Increment
Address
Command

↓

Load Data
for
Program Memory — Latch 32

↓   ↓

Begin
Programming
Command
(Internally timed)

Begin
Programming
Command
(Externally timed)

↓   ↓

Wait T$_{PINT}$

Wait T$_{PEXT}$

↓

End
Programming
Command

↓

Wait T$_{DIS}$
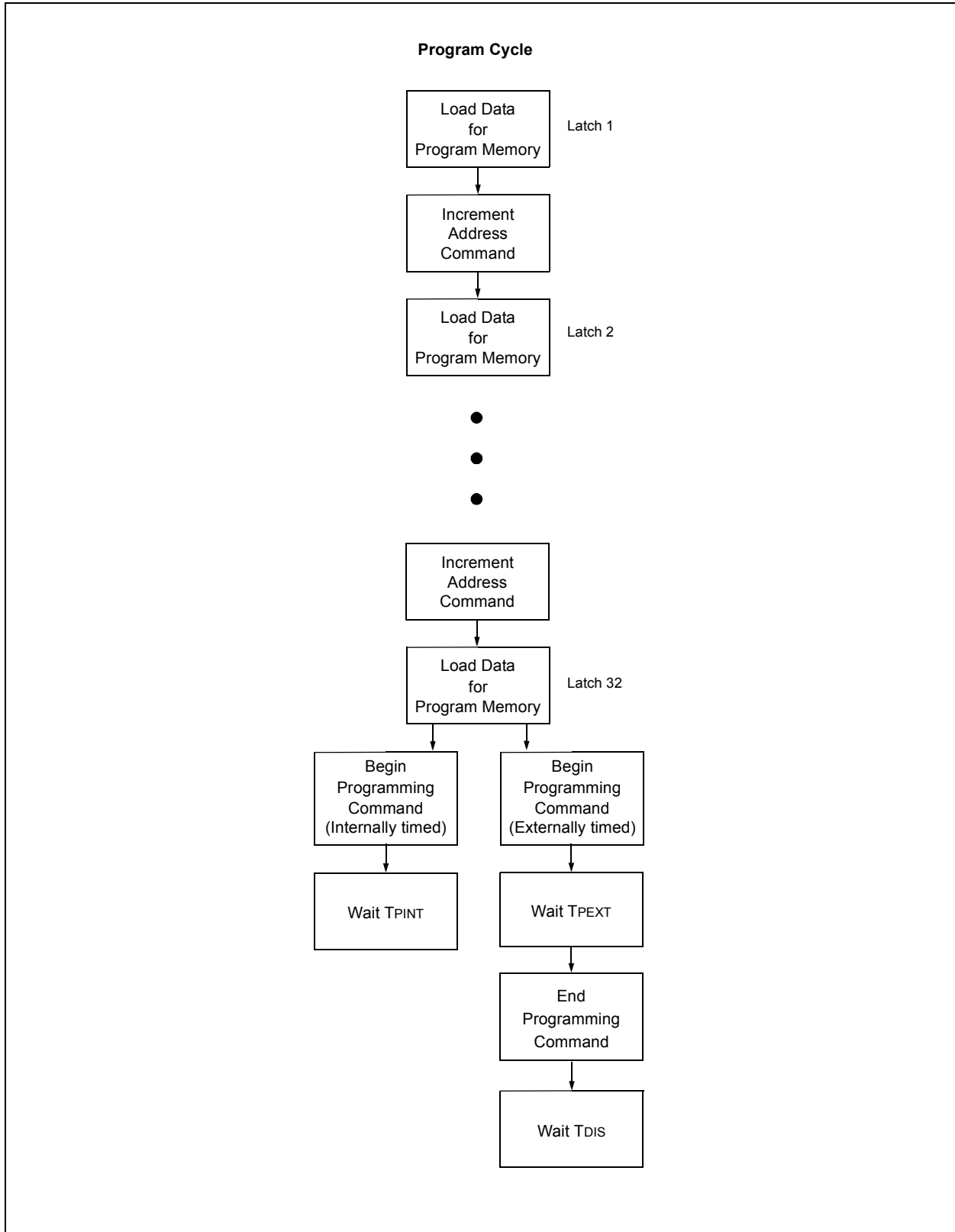
PIC12(L)F1571/2

FIGURE 5-5: **CONFIGURATION MEMORY PROGRAM FLOWCHART**

Start

Load Configuration

Bulk Erase Program Memory[1]

One-word Program Cycle[2] (User ID)

Read Data From Program Memory Command

Data Correct? — No → Report Programming Failure

Yes

Increment Address Command

Address = 8004h? — No (loops back) / Yes →

Increment Address Command

Increment Address Command

Increment Address Command

One-word Program Cycle[2] (Config. Word 1)

Read Data From Program Memory Command

Data Correct? — No → Report Programming Failure

Yes

Increment Address Command

One-word Program Cycle[2] (Config. Word 2)

Read Data From Program Memory Command → Data Correct? — No → Report Programming Failure

Yes

Done

Note 1: This step is optional if the device is erased or not previously programmed.
  2: See Figure 5-3.

FIGURE 5-6: **ERASE FLOWCHART**

Note: This sequence does not erase the Calibration Words.

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6.0 CODE PROTECTION

Code protection is controlled using the $\overline{\text{CP}}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh). Program memory can still be programmed and read during program execution.

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{\text{CP}}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: The Configuration Word 1 is stored at 8007h. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID against the value read from the part. On a mismatch condition, the programmer should generate a warning message.

7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{\text{CP}}$ Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC12F1571	0EFBh	3F03h
PIC12LF1571	0EFBh	3F03h
PIC12F1572	0EFBh	3F03h
PIC12LF1572	0EFBh	3F03h

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

7.3.2 PROGRAM CODE PROTECTION ENABLED

When the MPLAB IDE check box for Configure->ID Memory...-> Use Unprotected Checksum is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the user ID. Each nibble of the unprotected checksum is stored in the Least Significant nibble of each of the four user ID locations. The Most Significant checksum nibble is stored in the user ID at location 8000h, the second Most Significant nibble is stored at location 8001h, and so forth for the remaining nibbles and ID locations. The protected checksums in Table 7-2 assume that the Use Unprotected Checksum box is checked.

The checksum of a code-protected device is computed in the following manner: the Least Significant nibble of each user ID is used to create a 16-bit value. The Least Significant nibble of user ID location 8000h is the Most Significant nibble of the 16-bit value. The Least Significant nibble of user ID location 8001h is the second Most Significant nibble, and so forth for the remaining user IDs and 16-bit value nibbles. The resulting 16-bit value is summed with the Configuration Words. All unimplemented Configuration bits are masked to '0'.

TABLE 7-2:   CHECKSUMS

| Device | Config1 | | | Config2 | | Checksum | | | |
| | Unprotected | Protected | Mask | Word | Mask | Unprotected | | Code-protected | |
						Blank	00AAh First and Last	Blank	00AAh First and Last
PIC12F1571	3FFFh	3F7Fh	0EFBh	3FFFh	3F03h	49FEh	CB54h	977Ch	18D2h
PIC12LF1571	3FFFh	3F7Fh	0EFBh	3FFFh	3F03h	49FEh	CB54h	977Ch	18D2h
PIC12F1572	3FFFh	3F7Fh	0EFBh	3FFFh	3F03h	45FEh	C754h	937Ch	14D2h
PIC12LF1572	3FFFh	3F7Fh	0EFBh	3FFFh	3F03h	45FEh	C754h	937Ch	14D2h

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8.0   ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1:   AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
Programming Supply Voltages and Currents						
V$_{DD}$	Supply Voltage (V$_{DDMIN}$[2], V$_{DDMAX}$)	PIC12LF1571/2 1.80	—	3.60	V	F$_{OSC}$ ≤ 16 MHz
		2.70	—	3.60	V	F$_{OSC}$ ≤ 32 MHz
		PIC12F1571/2 2.30	—	5.50	V	F$_{OSC}$ ≤ 16 MHz
		2.70	—	5.50	V	F$_{OSC}$ ≤ 32 MHz
V$_{PEW}$	Read/Write and Row Erase operations	V$_{DDMIN}$	—	V$_{DDMAX}$	V	
V$_{BE}$	Bulk Erase operations	2.7	—	V$_{DDMAX}$	V	
I$_{DDI}$	Current on V$_{DD}$, Idle	—	—	1.0	mA	
I$_{DDP}$	Current on V$_{DD}$, Programming	—	—	3.0	mA	
	V$_{PP}$					
I$_{PP}$	Current on MCLR/V$_{PP}$	—	—	600	µA	
V$_{IHH}$	High voltage on MCLR/V$_{PP}$ for Program/Verify mode entry	8.0	—	9.0	V	
T$_{VHHR}$	MCLR rise time (V$_{IL}$ to V$_{IHH}$) for Program/Verify mode entry	—	—	1.0	µs	
	I/O pins					
V$_{IH}$	(ICSPCLK, ICSPDAT, MCLR/V$_{PP}$) input high level	0.8 V$_{DD}$	—	—	V	
V$_{IL}$	(ICSPCLK, ICSPDAT, MCLR/V$_{PP}$) input low level	—	—	0.2 V$_{DD}$	V	
V$_{OH}$	ICSPDAT output high level	V$_{DD}$-0.7 V$_{DD}$-0.7 V$_{DD}$-0.7	—	—	V	I$_{OH}$ = 3.5 mA, V$_{DD}$ = 5V I$_{OH}$ = 3 mA, V$_{DD}$ = 3.3V I$_{OH}$ = 2 mA, V$_{DD}$ = 1.8V
V$_{OL}$	ICSPDAT output low level	—	—	V$_{SS}$+0.6 V$_{SS}$+0.6 V$_{SS}$+0.6	V	I$_{OH}$ = 8 mA, V$_{DD}$ = 5V I$_{OH}$ = 6 mA, V$_{DD}$ = 3.3V I$_{OH}$ = 3 mA, V$_{DD}$ = 1.8V
V$_{BOR}$	Brown-out Reset Voltage: BORV = 0 (high trip)	—	2.70	—	V	PIC12(L)F1571/2
	BORV = 1 (low trip)	—	2.45	—	V	PIC12F1571/2
		—	1.90	—	V	PIC12LF1571/2
Programming Mode Entry and Exit						
T$_{ENTS}$	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before V$_{DD}$ or MCLR↑	100	—	—	ns	
T$_{ENTH}$	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after V$_{DD}$ or MCLR↑	250	—	—	µs	
Serial Program/Verify						
T$_{CKL}$	Clock Low Pulse Width	100	—	—	ns	
T$_{CKH}$	Clock High Pulse Width	100	—	—	ns	
T$_{DS}$	Data in setup time before clock↓	100	—	—	ns	
T$_{DH}$	Data in hold time after clock↓	100	—	—	ns	
T$_{CO}$	Clock↑ to data out valid (during a Read Data command)	0	—	80	ns	
T$_{LZD}$	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
T$_{HZD}$	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

2: Bulk-erased devices default to brown-out enabled. V$_{DDMIN}$ is 2.85 volts when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
T_{DLY}	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase cycle time	—	—	5	ms	
T_{ERAR}	Row Erase cycle time	—	—	2.5	ms	
T_{PINT}	Internally timed programming operation time	—	—	2.5 5	ms	Program memory Configuration Words
T_{PEXT}	Externally timed programming pulse	1.0	—	2.1	ms	**Note 1**
T_{DIS}	Time delay from program to compare (HV discharge time)	300	—	—	µs	
T_{EXIT}	Time delay when exiting Program/Verify mode	1	—	—	µs	

Note **1:** Externally timed writes are not supported for Configuration and Calibration bits.

      2: Bulk-erased devices default to brown-out enabled. V_{DDMIN} is 2.85 volts when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – V_{DD} FIRST
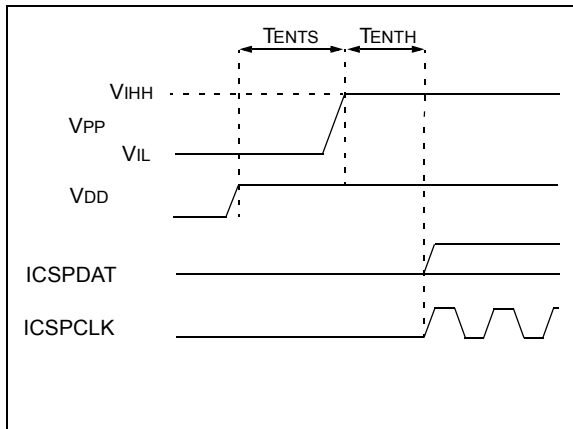
FIGURE 8-2: PROGRAMMING MODE ENTRY – V_{PP} FIRST
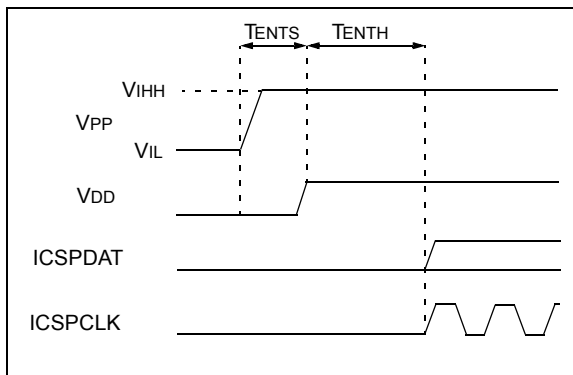
FIGURE 8-3: PROGRAMMING MODE EXIT – V_{PP} LAST
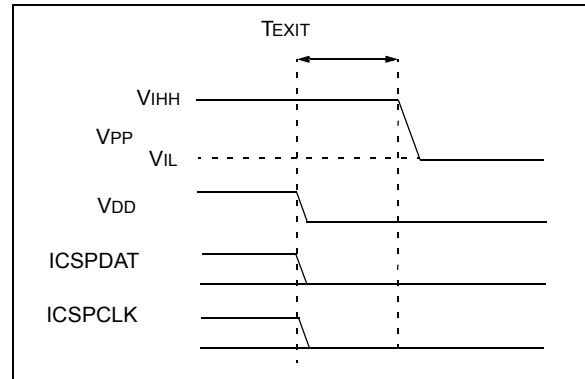
FIGURE 8-4: PROGRAMMING MODE EXIT – V_{DD} LAST
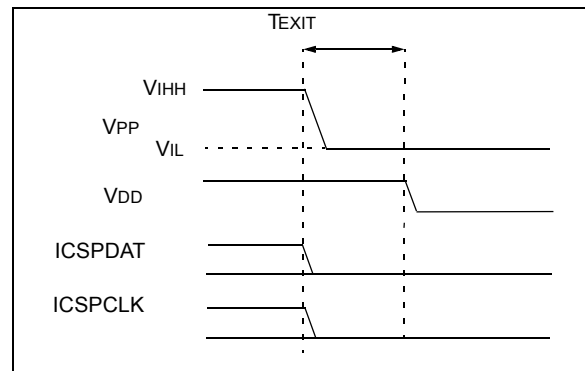
PIC12(L)F1571/2

FIGURE 8-5: **CLOCK AND DATA TIMING**
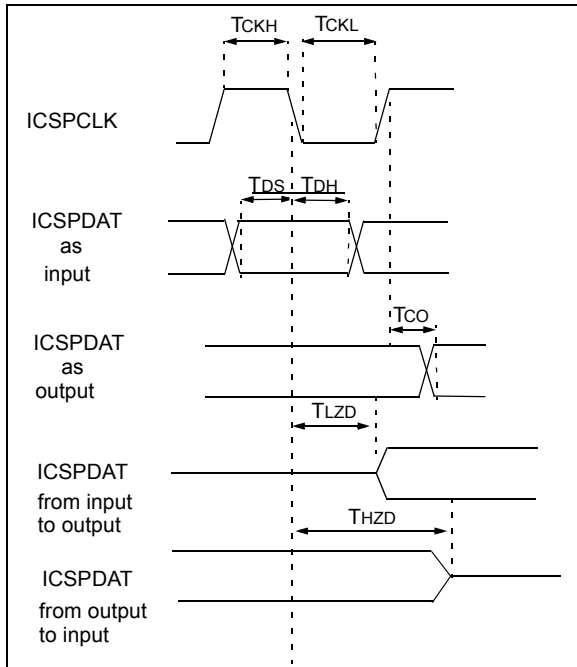
FIGURE 8-6: **WRITE COMMAND – PAYLOAD TIMING**
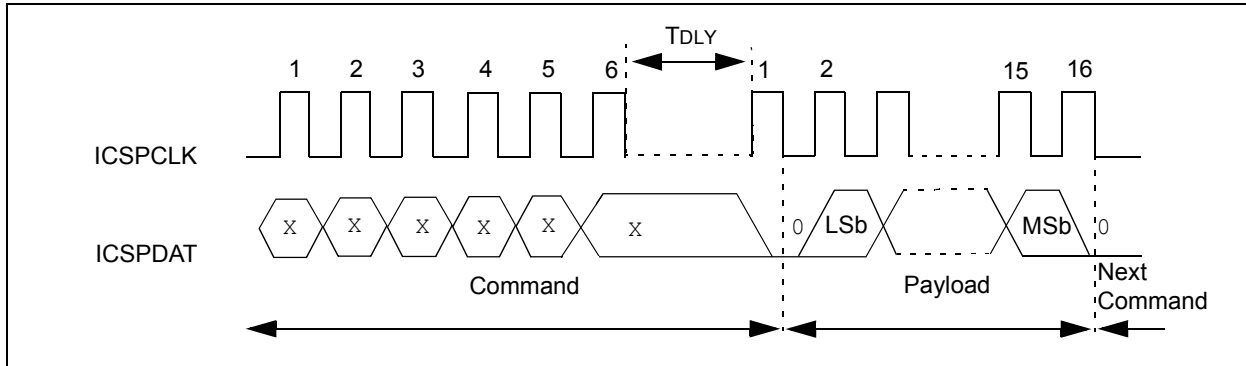
FIGURE 8-7: **READ COMMAND – PAYLOAD TIMING**
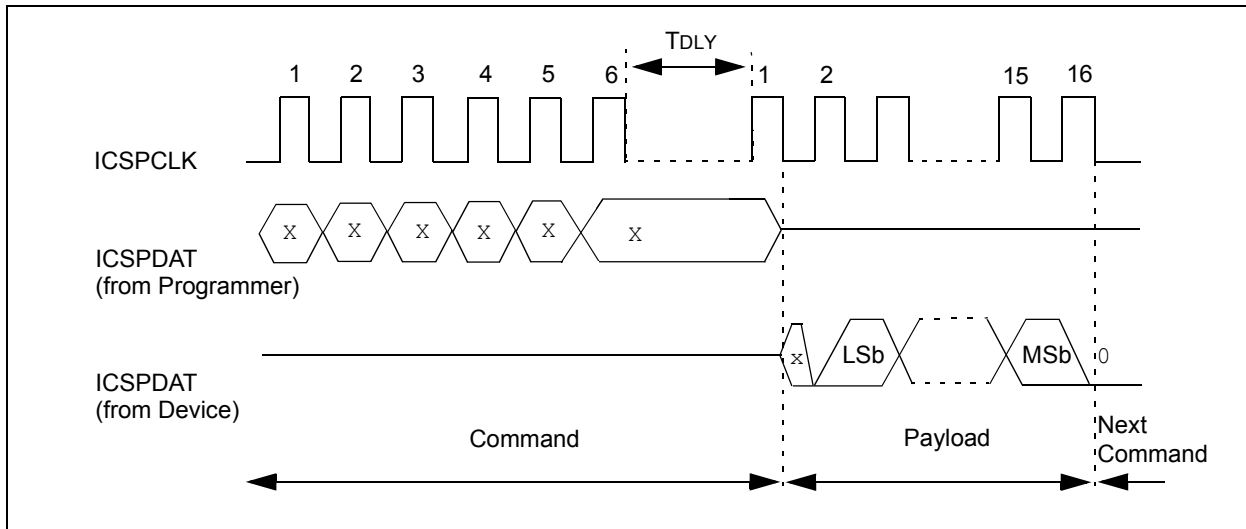
FIGURE 8-8: **LVP ENTRY (POWERING UP)**
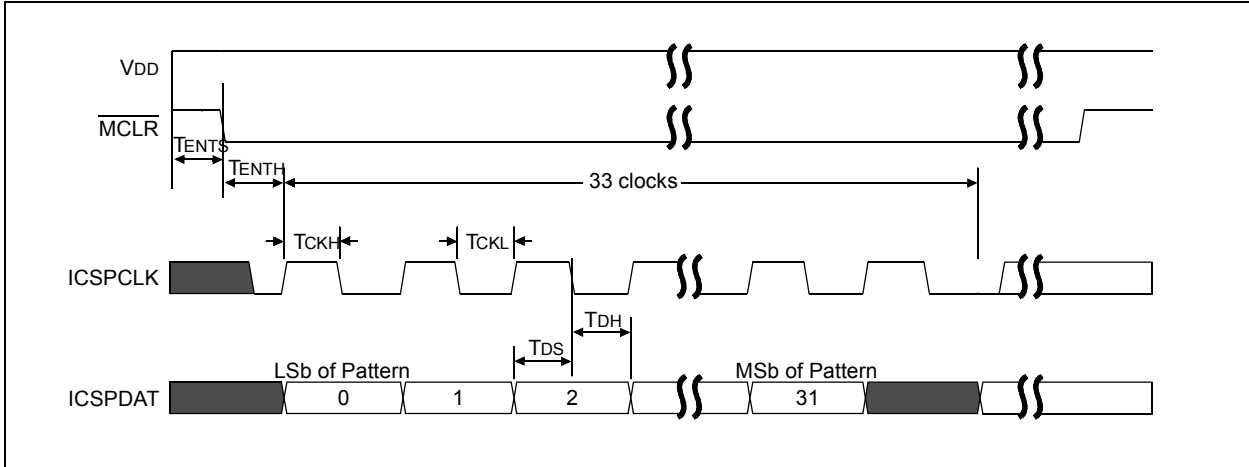
FIGURE 8-9: **LVP ENTRY (POWERED)**

Note 1: Sequence matching can start with no edge on MCLR first.
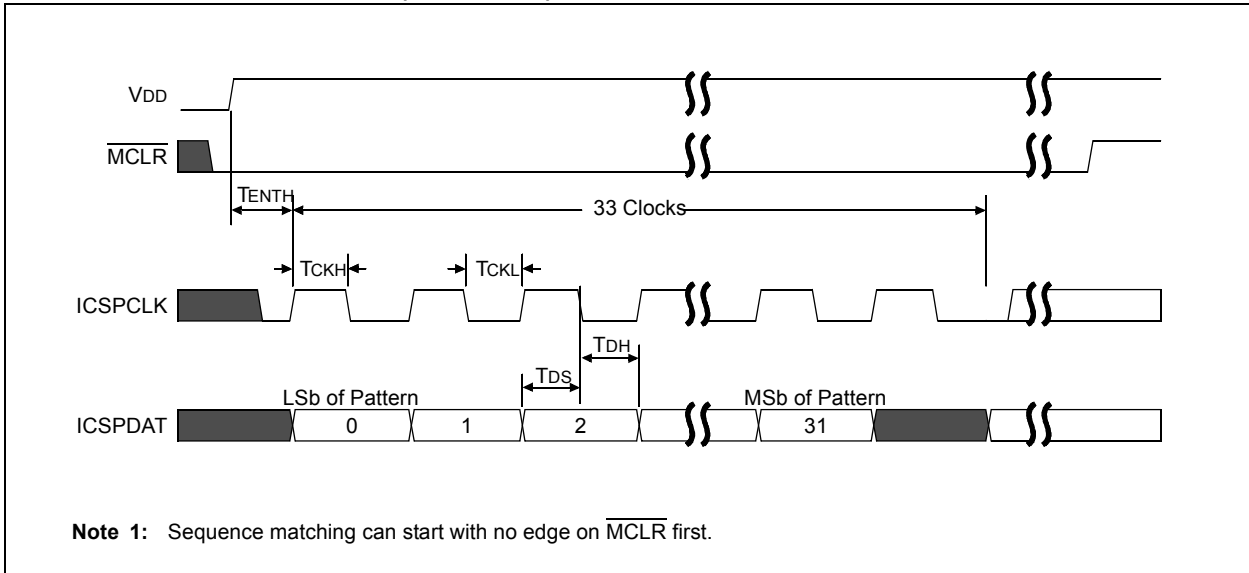
APPENDIX A: REVISION HISTORY

Revision A (06/2013)

Initial release of this document.

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