

SST211DE / SST213DE / SST215DE N-Channel DMOS Switch - Zener Protected

Description:

The SST211DE / SST213DE / SST215DE are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The family is normally used for $\pm 5V$ analog switching or as a high speed driver of the SD214. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated Zener diode provides ESD protection. A poly-silicon gate is featured for manufacturing reliability.

See SST5000 and SST54000 series for quad configurations.
For non-zener protected versions see SST210DE / SST214DE series

Features:

- Ultra-High Speed Switching—tON: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed R_{DS} @5V
- Low Turn-On Threshold Voltage (1.5V max)
- N-Channel Enhancement Mode

Benefits:

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Single Supply Operation & Simple Driver Requirement

Availability:

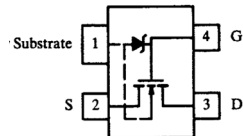
SST211DE / SST213DE / SST215DE – TO-253 (SOT-143)

SST211DE / SST213DE / SST215DE - Bare die form

[Contact Micross](#) for full package dimensions

Pinout:

Top View



Applications:

- Fast Analog Switching
- Fast Sample & Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

MAXIMUM RATINGS	LIMIT IN VOLTS		
	SST211	SST213	SST215
Gate-Drain, Gate-Source Voltage	-30/25	-15/25	-25/30
Gate-Substrate Voltage	-0.3/25	-0.3/25	-0.3/30
Drain-Source Voltage	30	10	20
Source-Drain Voltage	10	10	20
Drain -Substrate Voltage	30	15	25
Source-Substrate Voltage	15	15	25

MAXIMUM RATINGS (Continued)	LIMIT	UNIT
Drain Current	50	mA
Lead Temperature (1/16" from case, 10s)	300	°C
Storage Temperature	-65 to 150	°C
Operating Junction Temperature	-55 to 125	°C
Power Dissipation Derate 3mW/°C above 25°C	300	mW

ELECTRICAL SPECIFICATION $T_A = 25^\circ\text{C}$ unless otherwise noted	SYMBOL	TEST CONDITIONS	TYP	LIMITS						UNIT	
				SST211DE		SST213DE		SST215DE			
				MIN	MAX	MIN	MAX	MIN	MAX		
DRAIN-SOURCE BREAKDOWN VOLTAGE	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0V, I_D = 10\mu A$	35	30	-	-	-	-	-	V	
		$V_{GS} = V_{BS} = -5V, I_D = 10nA$	30	10	-	10	-	20	-		
SOURCE-DRAIN BREAKDOWN VOLTAGE	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5V, I_S = 10nA$	22	10	-	10	-	20	-	V	
DRAIN-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)DBO}$	$V_{GB} = 0V, I_D = 10nA$ Source Open	35	15	-	15	-	25	-		
SOURCE-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)SBO}$	$V_{GB} = 0V, I_S = 10\mu A$ Drain Open	35	15	-	15	-	25	-		
DRAIN-SOURCE LEAKAGE	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5V$	$V_{DS} = 10V$	0.4	-	10	-	10	-	-	nA
			$V_{DS} = 20V$	0.9	-	-	-	-	-	10	
SOURCE-DRAIN LEAKAGE	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5V$	$V_{SD} = 10V$	0.5	-	10	-	10	-	-	
			$V_{SD} = 20V$	1	-	-	-	-	-	10	
GATE LEAKAGE	I_{GBS}	$V_{DB} = V_{SB} = 0V, V_{GB} = 30V$	0.01	-	100	-	100	-	100	V	
THRESHOLD VOLTAGE	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1\mu A, V_{SB} = 0V$	0.8	0.5	1.5	0.1	1.5	0.1	1.5		
DRAIN-SOURCE-ON RESISTANCE	$R_{DS(on)}$	$V_{SB} = 0V$ $I_D = 1mA$	$V_{GS} = 5V$	60	-	75	-	75	-	75	Ω
			$V_{GS} = 10V$	40	-	50	-	50	-	50	
			$V_{GS} = 15V$	30	-	-	-	-	-	-	
			$V_{GS} = 20V$	26	-	-	-	-	-	-	
			$V_{GS} = 25V$	24	-	-	-	-	-	-	
FORWARD TRANSCONDUCTANCE	g_{fs}	$V_{DS} = 10V, V_{SB} = 0V$ $I_D = 20mA, f = 1kHz$	10.5	9	-	9	-	-	9	mS	
	g_{os}		0.9	-	-	-	-	-	9		
GATE NODE CAPACITANCE	$C_{(GS+GD+GB)}$	$V_{DS} = 10V, f = 1MHz$ $V_{GS} = V_{BS} = -15V$	2.5	-	3.5	-	3.5	-	3.5	pF	
DRAIN NODE CAPACITANCE	$C_{(GD+GB)}$		1.1	-	1.5	-	1.5	-	1.5		
SOURCE NODE CAPACITANCE	$C_{(GS+SB)}$		3.7	-	5.5	-	5.5	-	5.5		
REVERSE TRANSFER CAPACITANCE	C_{rss}		0.2	-	0.5	-	0.5	-	0.5		
TURN-ON TIME	$t_{D(on)}$		$V_{SB} = 0V, V_{IN} 0 \text{ to } 5V,$ $R_G = 25\Omega, V_{DD} = 5V, R_L = 680\Omega$	0.5	-	1	-	1	-		1
	t_r	0.6		-	1	-	1	-	1		
TURN-OFF TIME	$t_{D(off)}$	2		-	-	-	-	-	-		
	t_f	6		-	-	-	-	-	-		

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