

Small Signal Product

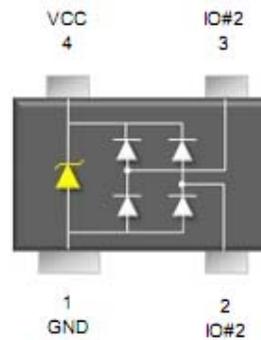
5V, 2-Channels ESD Protection Array

FEATURES

- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Protects two directional I/O lines
- Working voltage: 5V
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)



SOT-143



MECHANICAL DATA

- Case: SOT-143 small outline plastic package
- Terminal: Matte tin plated, lead free.
- High temperature soldering guaranteed : 260°C/10s
- Molding compound flammability Rating : UL 94V-0
- Weight: 10 ± 0.5 mg
- Marking code : SL3

APPLICATIONS

- USB Power & Data Line Protection
- I²C Bus Protection
- Video Line Protection
- Microcontroller Input Protections
- T1/E1 Secondary IC Side Protection
- ISDN S/T Interface
- WAN/LAN Equipment
- Ethernet 10BaseT

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T _A =25°C unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20µs waveform)	P _{PP}	200	W
Peak Pulse Current (tp=8/20µs waveform)	I _{PP}	10	A
ESD per IEC 61000-4-2 (Air)	V _{ESD}	± 15	KV
ESD per IEC 61000-4-2 (Contact)		± 8	
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

PARAMETER	SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage	V _{RWM}	-	5	V
Reverse Breakdown Voltage	V _(BR)	6	-	V
Reverse Leakage Current				
Clamping Voltage	V _C	-	9.8	V
			17	
Junction Capacitance	C _J	3		pF

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RATINGS AND CHARACTERISTICS CURVES

($T_A=25^\circ\text{C}$ unless otherwise noted)

Fig. 1 Admissible Power Dissipation Curve

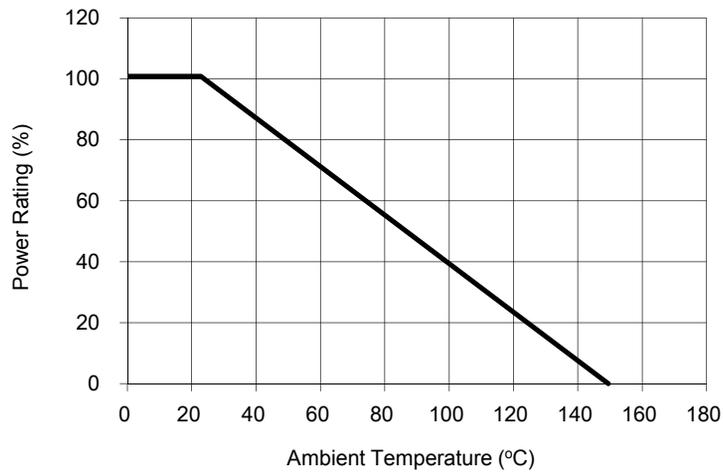


Fig. 2 Pulse Waveform

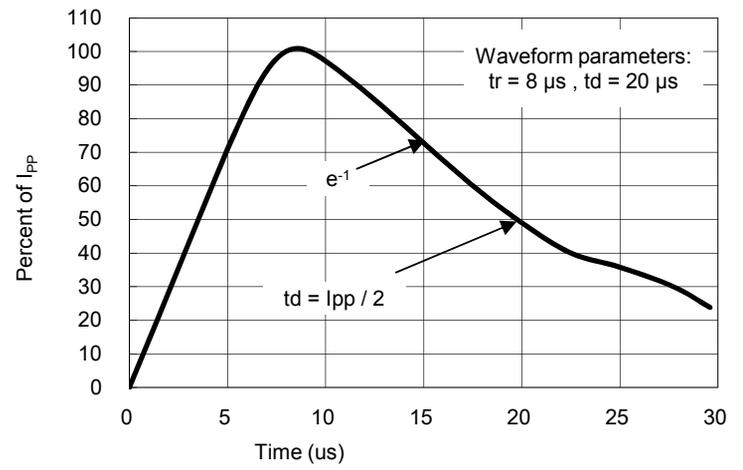


Fig. 3 Clamping Voltage VS. Peak Pulse Current

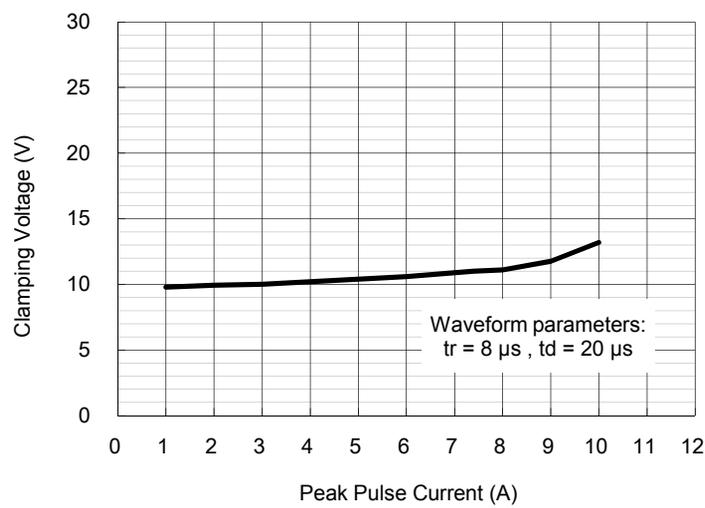
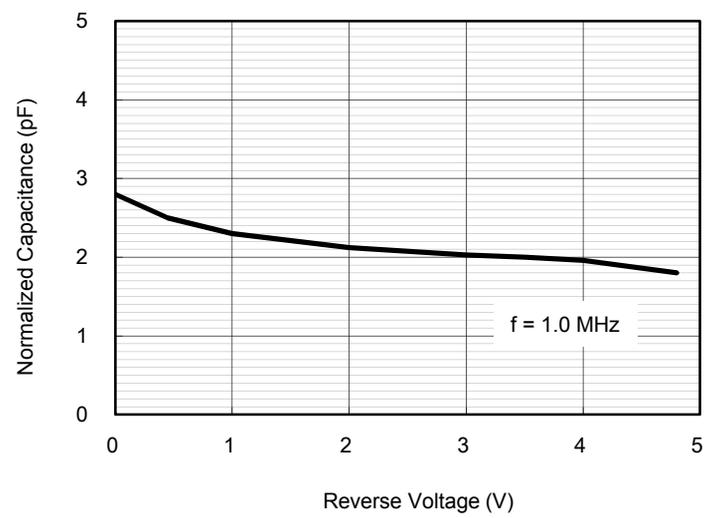


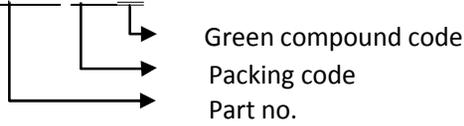
Fig. 4 Typical Junction Capacitance



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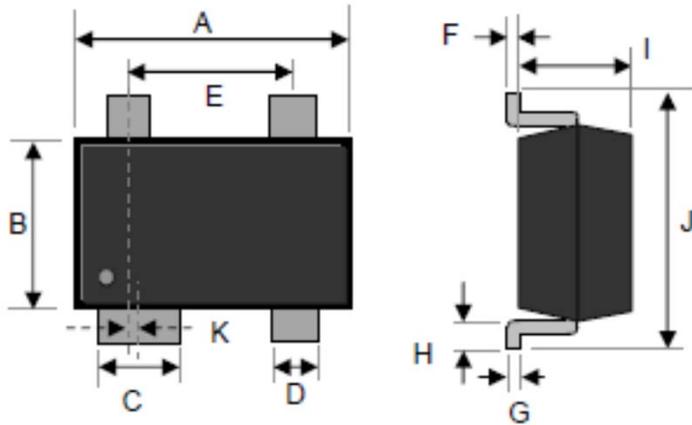
ORDER INFORMATION (EXAMPLE)

TESDB5V0A RBG



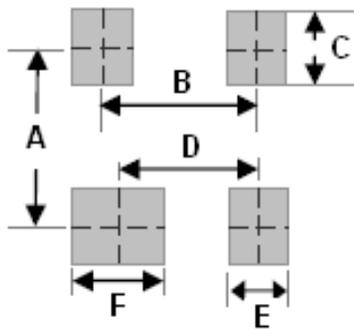
PACKAGE OUTLINE DIMENSIONS

SOT-143



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.80	3.04	0.110	0.120
B	1.20	1.40	0.047	0.055
C	0.75	0.94	0.030	0.037
D	0.30	0.51	0.012	0.020
E	1.80	2.64	0.071	0.104
F	0.00	0.10	0.000	0.004
G	0.08	0.20	0.003	0.008
H	0.30	0.60	0.012	0.024
I	0.75	1.15	0.030	0.045
J	2.10	2.64	0.083	0.104
K	0.2 TYP.		0.008 TYP.	

SUGGEST PAD LAYOUT

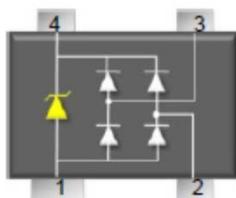


DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
Z	2.8	0.110
X	0.7	0.028
Y	0.9	0.035
C	1.9	0.075
E	1.0	0.039

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

APPLICATIONS INFORMATION

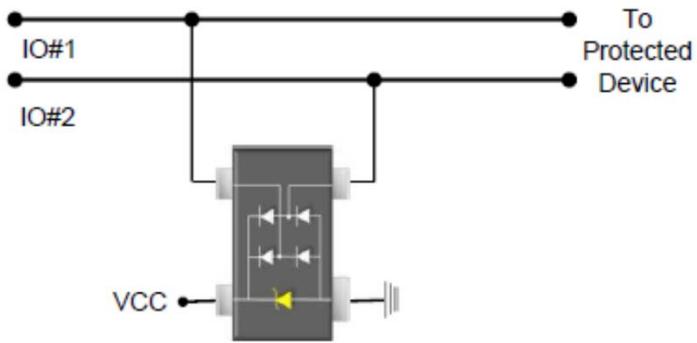
- ◇ Designed for the protect tow data lines from transient over-voltages by clamping them to afixed reference
- ◇ Data lines are connected at pins 2 and 3
- ◇ The negative reference (REF1) is connected at pin 1 and which should be connected directly to a ground plane
- ◇ The positive reference (REF2) is connected at pin 4



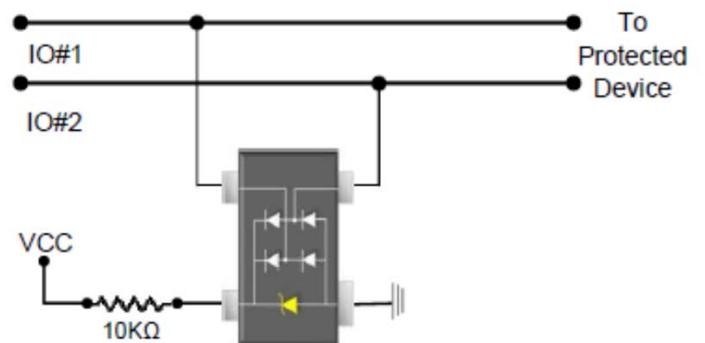
Pin	Definition
2, 3	I/O Lines
1	Ground
4	VCC

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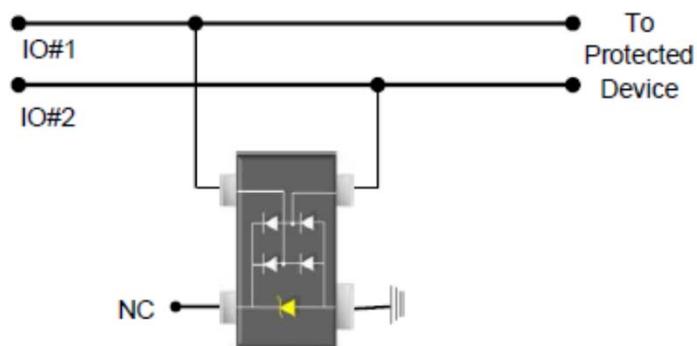
Schematic Diagram for Gigabit Ethernet ESD Protection



◇ Data Line and Power Supply Protection Using VCC



◇ Data Line Protection with Bias and Power Supply Isolation Resistor



◇ Data Line Protection Using Internal ESD Diode

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