
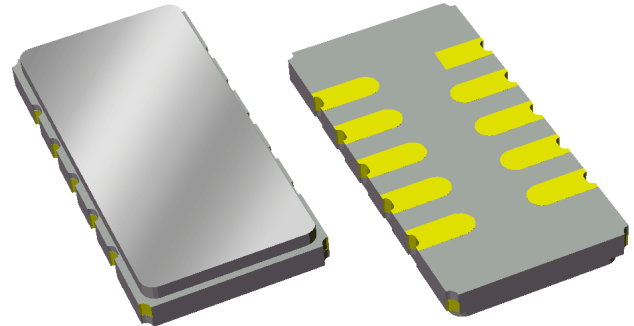


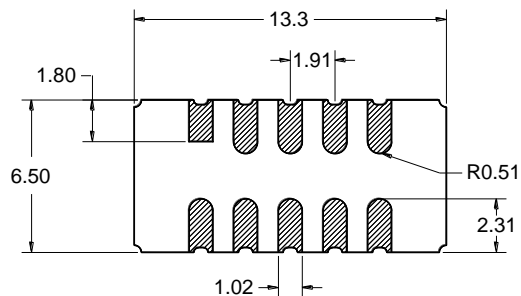
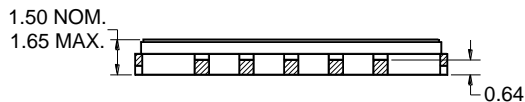
## Features

- For GSM and EDGE applications
- Usable bandwidth 0.22 MHz
- Typical 1dB bandwidth of 0.34 MHz
- Low loss
- High attenuation
- Balanced operation at 200Ω or Single-ended operation at 50Ω (different matching required)
- Ceramic Surface Mount Package (SMP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



## Package

Surface Mount 13.30 x 6.50 x 1.50 mm  
SMP-53C

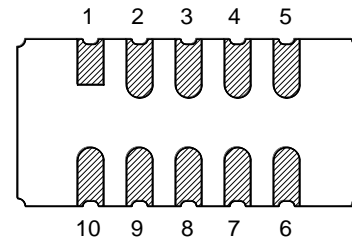


Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.15\text{mm}$  except overall  
length and width  $\pm 0.10\text{mm}$

Body:  $\text{Al}_2\text{O}_3$  ceramic  
Lid: Kovar, Ni plated  
Terminations: Au plating 0.5 - 1.0 $\mu\text{m}$ ,  
over a 2 - 6 $\mu\text{m}$  Ni plating

## Pin Configuration

Bottom View



### Balanced Configuration

Pin No.	Description
10,1	Input
5,6	Output
2,3,4	Case Ground
7,8,9	Case Ground

**Electrical Specifications <sup>(1)</sup>**

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

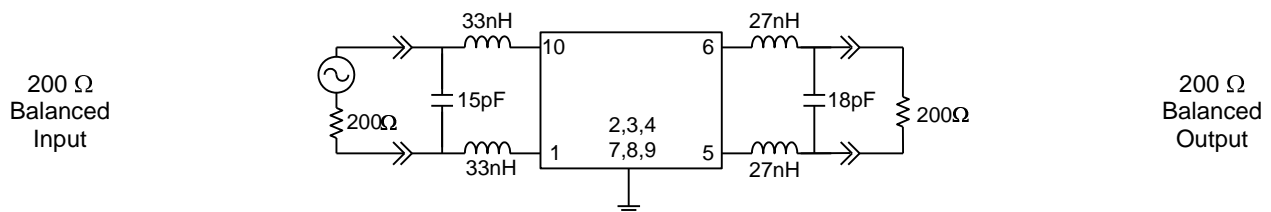
Parameter <sup>(3)</sup>	Minimum	Typical <sup>(4)</sup>	Maximum	Unit
Center Frequency ( $f_c$ )	-	201	-	MHz
Insertion Loss	-	6.1	7.0	dB
Lower 1 dB Band Edge	-	200.83	200.89	MHz
Upper 1 dB Band Edge	201.11	201.17	-	MHz
Amplitude Variation <sup>(5)</sup> 200.89 – 201.11 MHz	-	0.6	1.0	dB p-p
Absolute Group Delay at $f_c$	2.05	2.3	2.55	$\mu$ s
Group Delay Variation 200.89 – 201.11 MHz	-	0.8	1.5	$\mu$ s
Stopband Attenuation <sup>(6)</sup>				
$f_c \pm 0.3$ MHz to $f_c \pm 0.4$ MHz	16	25	-	dB
$f_c \pm 0.4$ MHz to $f_c \pm 0.6$ MHz	27	29	-	dB
$f_c \pm 0.6$ MHz to $f_c \pm 0.8$ MHz	28	32	-	dB
$f_c \pm 0.8$ MHz to $f_c \pm 1.5$ MHz	36	40	-	dB
$f_c \pm 1.5$ MHz to $f_c \pm 35$ MHz	38	40	-	dB
Source Impedance (Balanced) <sup>(7)</sup>	-	200	-	$\Omega$
Load Impedance (Balanced) <sup>(7)</sup>	-	200	-	$\Omega$

**Notes:**

1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. Amplitude variation is defined as the difference between the lowest loss and the highest loss within defined frequency points
6. Relative to insertion loss at 201 MHz
7. This is the optimum impedance in order to achieve the performance shown

**Test Circuit:**

Actual matching values may vary due to PCB layout and parasitics



**Electrical Specifications <sup>(1)</sup>**

Operating Temperature Range: <sup>(2)</sup> -40 to +85 °C

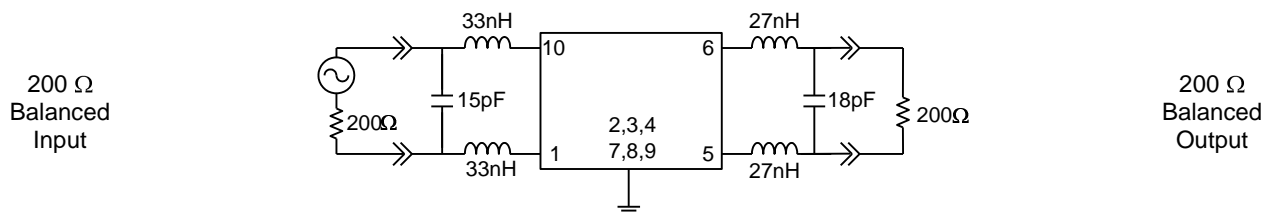
Parameter <sup>(3)</sup>	Minimum	Typical <sup>(4)</sup>	Maximum	Unit
Center Frequency ( $f_c$ )	-	201	-	MHz
Insertion Loss	-	6.1	7.2	dB
Lower 1 dB Band Edge	-	200.83	200.89	MHz
Upper 1 dB Band Edge	201.081	201.17	-	MHz
Amplitude Variation <sup>(5)</sup> 200.89 – 201.11 MHz	-	0.6	1.4	dB p-p
Absolute Group Delay at $f_c$	2.05	2.3	2.55	$\mu$ s
Group Delay Variation 200.89 – 201.11 MHz	-	0.8	1.5	$\mu$ s
Stopband Attenuation <sup>(6)</sup>				
$f_c - 35$ MHz to $f_c - 1.5$ MHz	38	40	-	dB
$f_c - 1.5$ MHz to $f_c - 0.8$ MHz	35	40	-	dB
$f_c - 0.8$ MHz to $f_c - 0.6$ MHz	28	32	-	dB
$f_c - 0.6$ MHz to $f_c - 0.4$ MHz	25	29	-	dB
$f_c - 0.4$ MHz to $f_c - 0.3$ MHz	10.5	25	-	dB
$f_c + 0.3$ MHz to $f_c + 0.4$ MHz	16	25	-	dB
$f_c + 0.4$ MHz to $f_c + 0.6$ MHz	27	29	-	dB
$f_c + 0.6$ MHz to $f_c + 0.8$ MHz	28	32	-	dB
$f_c + 0.8$ MHz to $f_c + 1.5$ MHz	35	40	-	dB
$f_c + 1.5$ MHz to $f_c + 35$ MHz	38	40	-	dB
Source Impedance (Balanced) <sup>(7)</sup>	-	200	-	$\Omega$
Load Impedance (Balanced) <sup>(7)</sup>	-	200	-	$\Omega$

**Notes:**

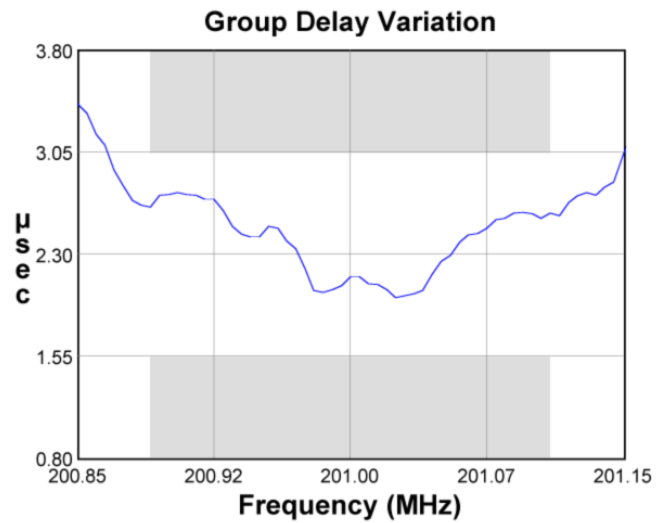
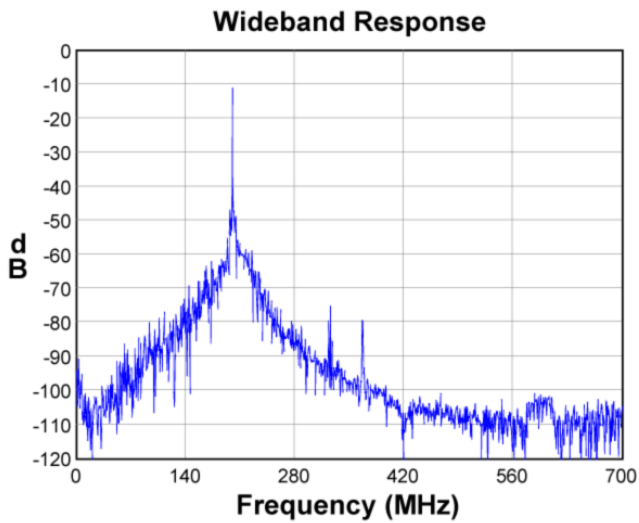
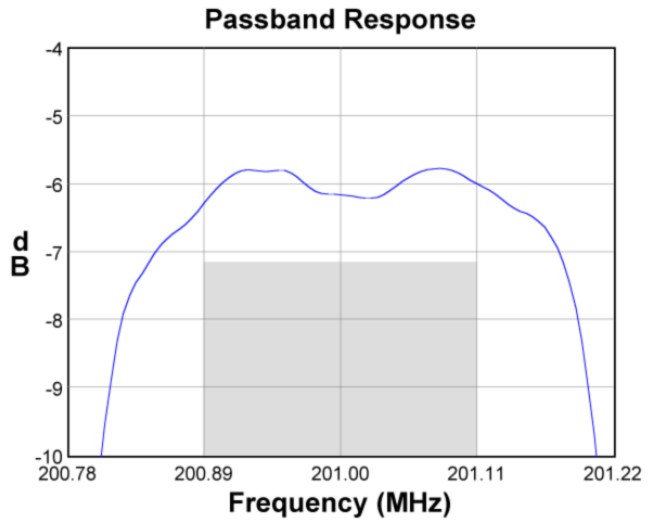
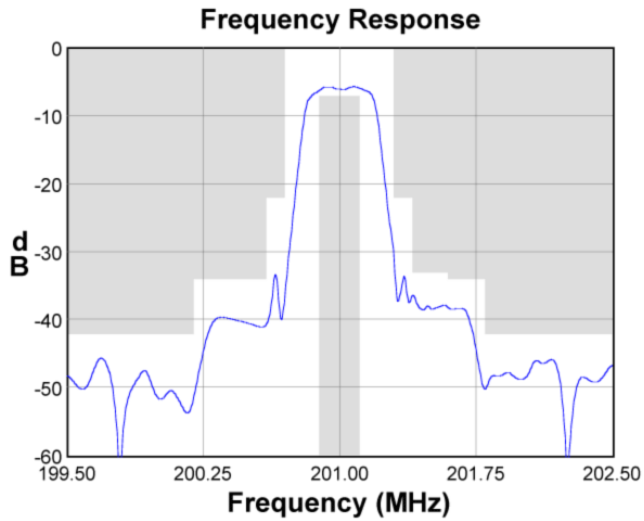
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2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
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6. Relative to insertion loss at 201 MHz
7. This is the optimum impedance in order to achieve the performance shown

**Test Circuit:**

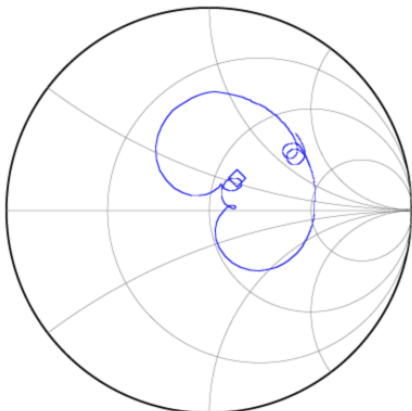
Actual matching values may vary due to PCB layout and parasitics



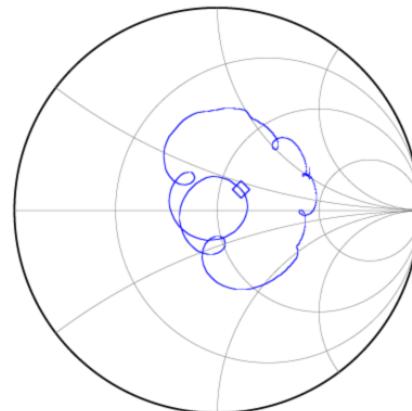
**Typical Performance (at room temperature)**



**Input Smith Chart**

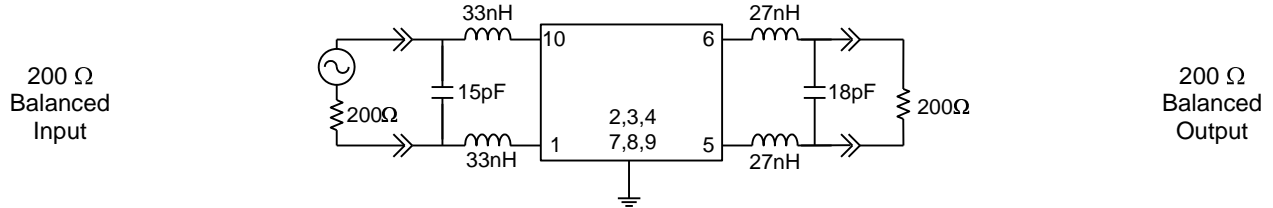


**Output Smith Chart**

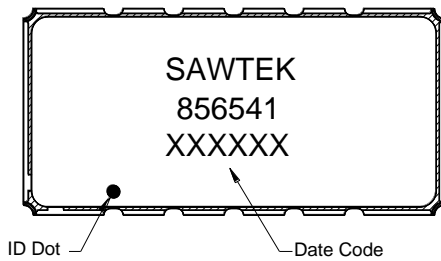


**Matching Schematics**

Actual matching values may vary due to PCB layout and parasitics

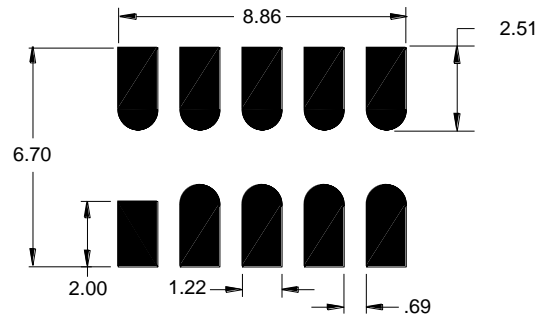


**Marking**



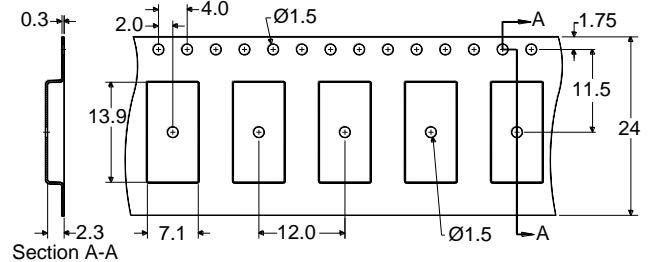
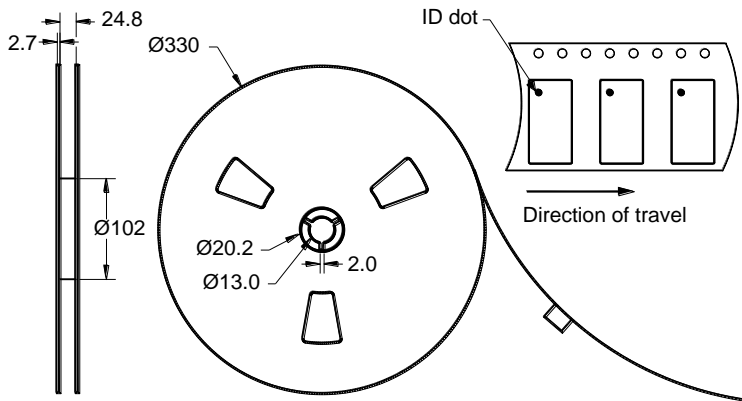
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

**PCB Footprint**



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**




Dimensions shown are nominal in millimeters  
Packaging quantity: 2000 units/reel

### Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-40	+85	°C
Storage Temperature Range	T <sub>stg</sub>	-40	+85	°C

### Important Notes

#### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

#### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

#### Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

### Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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