19-5235; Rev 1; 2/11

Stereo Audio CODEC with FlexSound Technology

General Description

The MAX9888 is a full-featured audio CODEC whose high performance and low power consumption make it ideal for portable applications.

Class D speaker amplifiers provide efficient amplification for two speakers. Low radiated emissions enable completely filterless operation. Integrated bypass switches optionally connect an external amplifier to the transducer when the Class D amplifiers are disabled.

DirectDrive® headphone amplifiers provide a true ground-referenced output, eliminating the need for large DC-blocking capacitors. 1.8V headphone operation ensures low power consumption. The device also includes a differential receiver amplifier.

Three differential analog microphone inputs are available as well as support for two PDM digital microphones. Integrated switches allow microphone signals to be routed out to external devices. Two flexible single-ended or differential line inputs may be connected to an FM radio or other sources.

Integrated FlexSound™ technology improves loudspeaker performance by optimizing the signal level and frequency response while limiting the maximum distortion and power at the output to prevent speaker damage. Automatic gain control (AGC) and a noise gate optimize the signal level of microphone input signals to make best use of the ADC dynamic range.

The device is fully specified over the -40°C to +85°C extended temperature range.

DirectDrive is a registered trademark and FlexSound is a trademark of Maxim Integrated Products, Inc.

Features

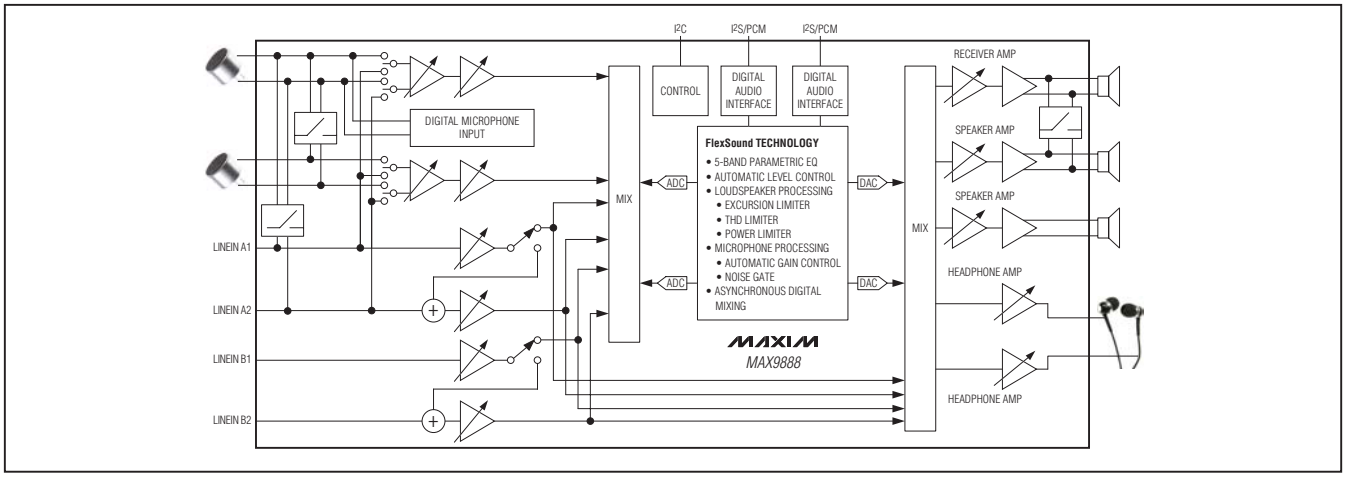
- **100dB DR Stereo DAC (8kHz < f_S < 96kHz)**
- **91dB DR Stereo ADC (8kHz < f_S < 96kHz)**
- **Stereo Low EMI Class D Amplifiers**
  950mW/Channel (8Ω, $V_{SPKVDD\_}$ = 4.2V)
- **Stereo DirectDrive Headphone Amplifiers**
- **Differential Receiver Amplifier**
- **2 Stereo Single-Ended/Mono Differential Line Inputs**
- **3 Differential Microphone Inputs**
- **FlexSound Technology**
  5-Band Parametric EQ
  Automatic Level Control (ALC)
  Excursion Limiter
  Speaker Power Limiter
  Speaker Distortion Limiter
  Microphone Automatic Gain Control and Noise Gate
- **Dual I²S/PCM/TDM Digital Audio Interfaces**
- **Asynchronous Digital Mixing**
- **Supports Master Clock Frequencies from 10MHz to 60MHz**
- **RF Immune Analog Inputs and Outputs**
- **Extensive Click-and-Pop Reduction Circuitry**
- **I²C Control Interface**
- **63 WLP Package (3.80mm x 3.30mm, 0.4mm Pitch)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9888EWY+	-40°C to +85°C	63 WLP

+Denotes lead(Pb)-free/RoHS-compliant package.

Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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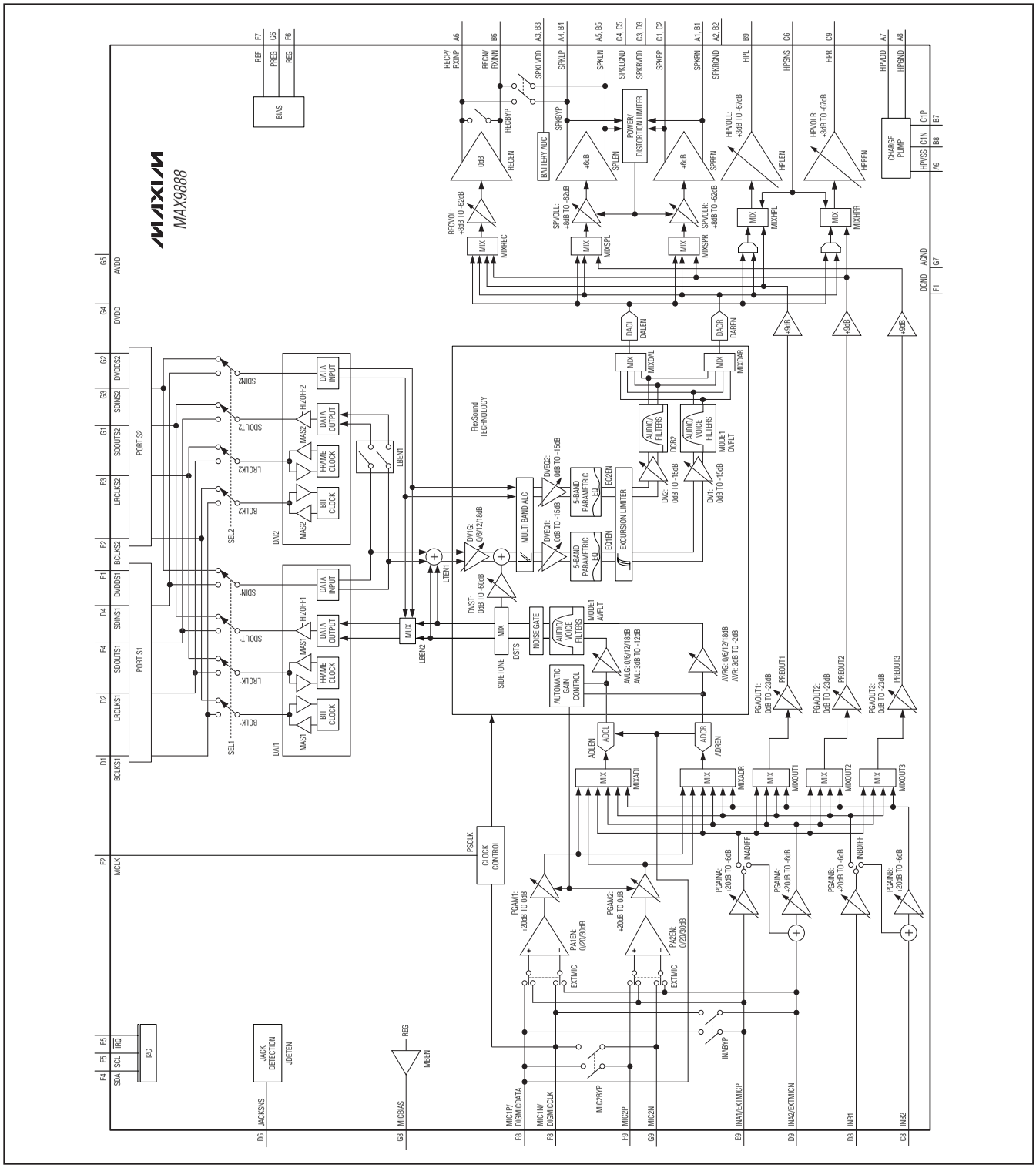
Functional Diagram



Stereo Audio CODEC with FlexSound Technology

ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND.)

DVDD, AVDD, HPVDD .....-0.3V to +2.2V
SPKLVDD, SPKRVDD, DVDDS1, DVDDS2 .....-0.3V to +6.0V
DGND, HPGND, SPKLGND, SPKRGND .....-0.1V to +0.1V
HPVSS .....(HPGND - 2.2V) to (HPGND + 0.3V)
C1N ..... (HPVSS - 0.3V) to (HPGND + 0.3V)
C1P.....(HPGND - 0.3V) to (HPVDD + 0.3V)
PREG ..... -0.3V to (AVDD + 0.3V)
REF, MICBIAS .....-0.3V to (SPKLVDD + 0.3V)
MCLK, SDINS1, SDINS2, JACKSNS,
SDA, SCL, $\overline{IRQ}$ .....-0.3V to +6.0V
LRCLKS1, BCLKS1, SDOUTS1.....-0.3V to (DVDDS1 + 0.3V)
LRCLKS2, BCLKS2, SDOUTS2.....-0.3V to (DVDDS2 + 0.3V)
REG, INA1, INA2, INB1, INB2, MIC1P/DIGMICDATA,
MIC1N/DIGMICCLK, MIC2P, MIC2N .....-0.3V to +2.2V
HPSNS.....(HPGND - 0.3V) to (HPGND + 0.3V)
HPL, HPR .....(HPVSS - 0.3V) to (HPVDD + 0.3V)
RECP, RECN .....(SPKLGND - 0.3V) to (SPKLVDD + 0.3V)
SPKLP, SPKLN .....(SPKLGND - 0.3V) to (SPKLVDD + 0.3V)
SPKRP, SPKRN .....(SPKRGND - 0.3V) to (SPKRVDD + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
63-Bump WLP (derate 25.6mW/°C above +70°C).....2.05W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range		Guaranteed by PSRR	$V_{SPKLVDD}$, $V_{SPKRVDD}$	2.8		5.5	V
			V_{DVDD}, V_{AVDD}, V_{HPVDD}	1.65	1.8	2.0	
			V_{DVDDS1}, V_{DVDDS2}	1.65		3.6	
Total Supply Current (Note 2)	I_{VDD}	Full-duplex 8kHz mono, receiver output (Note 3)	Analog		6.37	10	mA
			Speaker		1.98	3.5	
			Digital		1.49	3	
		DAC playback 48kHz stereo, headphone outputs (Note 3)	Analog		2.71	4	
			Speaker		1.65	2.5	
			Digital		2.93	4.5	
		DAC playback 48kHz stereo, speaker outputs (Note 3)	Analog		1.85	3	
			Speaker		8.22	18	
			Digital		2.94	5	
		Full-duplex 48kHz stereo, microphone inputs, headphone outputs (Note 3)	Analog		12.75	18	
			Speaker		1.7	3	
			Digital		3.75	5.5	
		Stereo line playback, IN_DIF = 0, INA1 to HPL, INA2 to HPR, V_{MCLK} = 0V	Analog		5.11	7	
			Speaker		0.58	1	
			Digital		0.03	0.06	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current (Note 2)		T_A = +25°C	Analog		0.2	2	µA
			Speaker		0.1	1	
			Digital		1	5	
REF Voltage					2.5		V
PREG Voltage					1.6		V
REG Voltage					0.7		V
Shutdown to Full Operation		$\overline{SLEW}$ = 0			30		ms
		$\overline{SLEW}$ = 1			17		
MICROPHONE TO ADC PATH							
Dynamic Range (Note 4)	DR	f_S = 8kHz, MODE = 0 (IIR voice), $AV_{MICPRE\_}$ = 0dB		75	88		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 0.1V_{P-P}, MCLK = 12.288MHz, f_S = 8kHz, f = 1kHz			-77	-65	dB
		$AV_{MICPRE\_}$ = 0dB, V_{IN} = 1V_{P-P}, f = 1kHz			-82		
		$AV_{MICPRE\_}$ = +30dB, V_{IN} = 32mV_{P-P}, f = 1kHz			-71		
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P}, f = 217Hz			65		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 2.0V, input referred, MIC inputs floating		60	100		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred			100		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred			91		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred			70		
Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output	MODE = 0 (IIR voice) 8kHz		2.2		ms
			MODE = 0 (IIR voice) 16kHz		1.1		
			MODE = 1 (FIR audio) 8kHz		4.5		
			MODE = 1 (FIR audio) 48kHz		0.76		

Stereo Audio CODEC with FlexSound Technology

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE PREAMP							
Full-Scale Input		$AV_{MICPRE\_}$ = 0dB			1.05		V_{P-P}
Preamplifier Gain	$AV_{MICPRE\_}$	(Note 5)	PA1EN/PA2EN = 01		0		dB
			PA1EN/PA2EN = 10	19.5	20	20.5	
			PA1EN/PA2EN = 11	29.4	30	30.5	
PGA Gain	$AV_{MICPGA\_}$	(Note 5)	PGAM1/PGAM2 = 0x00	19.5	20	20.5	dB
			PGAM1/PGAM2 = 0x14		0		
MIC Input Resistance	R_{IN_MIC}	All gain settings, measured at MIC1P/MIC1N/ MIC2P/MIC2N		30	50		kΩ
MICROPHONE BIAS							
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA		2.14	2.2	2.25	V
Load Regulation		I_{LOAD} = 1mA to 2mA			0.5	11	mV
Line Regulation		$V_{SPKLVDD}$ = 2.8V to 5.5V			100		µV
Ripple Rejection		f = 217Hz, $V_{RIPPLE\ (SPKLVDD)}$ = 100mV_{P-P}			92		dB
		f = 10kHz, $V_{RIPPLE\ (SPKLVDD)}$ = 100mV_{P-P}			83		
Noise Voltage		A-weighted, f = 20Hz to 20kHz			3.8		μV_{RMS}
		P-weighted, f = 20Hz to 4kHz			2.1		
		f = 1kHz			33		$nV/\sqrt{Hz}$
MICROPHONE BYPASS SWITCH							
On-Resistance	R_{ON}	$I_{MIC1\_}$ = 100mA, INABYP = MIC2BYP = 1, $V_{MIC2\_}$ = $V_{INA\_}$ = (0V, V_{AVDD})			3.5	20	Ω
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 2V_{P-P}, V_{CM} = 0.9V, R_L = 10kΩ, f = 1kHz, INABYP = MIC2BYP = 1			-80		dB
Off-Isolation		V_{IN} = 2V_{P-P}, V_{CM} = 0.9V, R_L = 10kΩ, f = 1kHz			60		dB
Off-Leakage Current		$V_{MIC1\_}$ = (0V, V_{AVDD}), $V_{MIC2\_}/V_{INA\_}$ = (V_{AVDD}, 0V)		-2.5		+2.5	µA
LINE INPUT TO ADC PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz, MCLK = 12.288MHz, MODE = 1 (FIR audio)			91		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 1V_{P-P}, f = 1kHz			-77		dB
Gain Error		DC accuracy			1	5	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINE INPUT PREAMP							
Full-Scale Input	V_{IN}	$AV_{PGAIN\_}$ = 0dB			1		V_{P-P}
		$AV_{PGAIN\_}$ = -6dB			1.4		
Level Adjust Gain	$AV_{PGAIN\_}$	PGAINA/PGAINB = 0x0		19	20	21	dB
		PGAINA/PGAINB = 0x1		13	14	15	
		PGAINA/PGAINB = 0x2	(Note 5)	2	3	4	
		PGAINA/PGAINB = 0x3	T_A = +25°C		0		
		PGAINA/PGAINB = 0x4		-4	-3	-2	
		PGAINA/PGAINB = 0x5, 0x6, 0x7		-7	-6	-5	
Input Resistance	R_{IN}	$AV_{PGAIN\_}$ = +20dB		14.6	21	27.4	kΩ
		$AV_{PGAIN\_}$ = +14dB			20		
		$AV_{PGAIN\_}$ = +3dB			20		
		$AV_{PGAIN\_}$ = 0dB		7.3	10	13.7	
		$AV_{PGAIN\_}$ = -3dB			20		
		$AV_{PGAIN\_}$ = -6dB			20		
Feedback Resistance	R_{IN_FB}	INAEXT/INBEXT = 1	T_A = +25°C	18.5	20	21.5	kΩ
			T_A = T_{MIN} to T_{MAX}	17.5		23	
ADC LEVEL CONTROL							
ADC Level Adjust Range	AV_{ADCLVL}	AVL/AVR = 0xF to 0x0 (Note 5)		-12		+3	dB
ADC Level Adjust Step Size					1		dB
ADC Gain Adjust Range	$AV_{ADCGAIN}$	AVLG/AVRG = 00 to 11 (Note 5)		0		18	dB
ADC Gain Adjust Step Size					6		dB
ADC DIGITAL FILTERS							
VOICE MODE IIR LOWPASS FILTER (MODE1 = 0)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff		0.441 x f_S			Hz
		-3dB cutoff		0.449 x f_S			
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.47 x f_S	Hz
Stopband Attenuation (Note 6)		f > f_{SLP}		74			dB

Stereo Audio CODEC with FlexSound Technology

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOICE MODE IIR HIGHPASS FILTER (MODE1 = 0)						
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)			0.0161 x f_S	Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)			0.0319 x f_S	
		AVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)			0.0321 x f_S	
		AVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)			0.0632 x f_S	
		AVFLT = 0x5 (f_S/240 Butterworth)			0.0043 x f_S	
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)	0.0139 x f_S			Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)	0.0156 x f_S			
		AVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)	0.0279 x f_S			
		AVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)	0.0312 x f_S			
		AVFLT = 0x5 (f_S/240 Butterworth)	0.002 x f_S			
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1 = 0, LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.48 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 6)		f < f_{SLP}	60			dB
ADC STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1 = 1, LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.208 x f_S			Hz
		-3dB cutoff	0.28 x f_S			

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.417 x f_S	Hz
Stopband Attenuation		f < f_{SLP}		60			dB
ADC STEREO AUDIO MODE DC-BLOCKING HIGHPASS FILTER (MODE1 = 1)							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT ≠ 000				0.000125 x fs	Hz
DC Attenuation	DC_{Atten}	AVFLT ≠ 000			90		dB
MICROPHONE AUTOMATIC GAIN CONTROL							
AGC Hold Duration		AGCHLD = 01			50		ms
		AGCHLD = 11			400		
AGC Attack Time		AGCATK = 00			2		ms
		AGCATK = 11			123		
AGC Release Time		AGCRLS = 000			0.078		s
		AGCRLS = 111			10		
AGC Threshold Level		AGCTH = 0x0 to 0xF		-3		+18	dB
AGC Threshold Step Size					1		dB
AGC Gain		(Note 5)		0		20	dB
ADC NOISE GATE							
NG Threshold Level		ANTH = 0x3 to 0xF, referred to 0dBFS		-64		-16	dB
NG Attenuation		(Note 5)		0		12	dB
ADC-TO-DAC DIGITAL SIDETONE (MODE = 0)							
Sidetone Gain Adjust Range	AV_{STGA}	DVST = 0x01			-0.5		dB
		DVST = 0x1F			-60.5		
Sidetone Gain Adjust Step Size					2		dB
Sidetone Path Phase Delay		1kHz, 0dB input, highpass filter disabled	8kHz		2.2		ms
			16kHz		1.1		
ADC-TO-DAC DIGITAL LOOP-THROUGH PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz, MCLK = 12.288MHz, MODE = 1 (FIR audio)			89		dB
Total Harmonic Distortion	THD	f = 1kHz, f_S = 48kHz, MCLK = 12.288MHz, MODE = 1 (FIR audio)			-71	-66	dB
DAC LEVEL CONTROL							
DAC Attenuation Range	$AV_{DACATTN}$	DV1DV2 = 0xF to 0x0 (Note 5)		-15		0	dB
DAC Attenuation Step Size					1		dB
DAC Gain Adjust Range	$AV_{DACGAIN}$	DV1G = 00 to 11 (Note 5)		0		18	dB
DAC Gain Adjust Step Size					6		dB

Stereo Audio CODEC with FlexSound Technology

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC DIGITAL FILTERS						
VOICE MODE IIR LOWPASS FILTER (MODE1 = 0)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.448 x f_S			Hz
		-3dB cutoff	0.451 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.476 x f_S	Hz
Stopband Attenuation (Note 6)		f > f_{SLP}	75			dB
VOICE MODE IIR HIGHPASS FILTER (MODE1 = 0)						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)			0.0161 x f_S	Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)			0.0312 x f_S	
		DVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)			0.0321 x f_S	
		DVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)			0.0625 x f_S	
		DVFLT = 0x5 (f_S/240 Butterworth)			0.0042 x f_S	
Stopband Cutoff (-30dB from Peak)	f_{DHPSB}	DVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)	0.0139 x f_S			Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)	0.0156 x f_S			
		DVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)	0.0279 x f_S			
		DVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)	0.0312 x f_S			
		DVFLT = 0x5 (f_S/240 Butterworth)	0.002 x f_S			
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000		85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1/DHF2 = 0, LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.47 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 6)		f > f_{SLP}	60			dB
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF1/DHF2 = 1 for LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.24 x f_S			Hz
		-3dB cutoff	0.31 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.477 x f_S	Hz
Stopband Attenuation (Note 6)		f < f_{SLP}	60			dB
STEREO AUDIO MODE DC-BLOCKING HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT ≠ 000 (DAI1), DCB2 = 1 (DAI2)			0.000104 x f_S	Hz
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000 (DAI1), DCB2 = 1 (DAI2)		90		dB
AUTOMATIC LEVEL CONTROL						
Dual Band Lowpass Corner Frequency		ALCMB = 1		5		kHz
Dual Band Highpass Corner Frequency		ALCMB = 1		5		kHz
Gain Range			0		12	dB
Low Signal Threshold		ALCTH = 111 to 001	-48		-12	dBFS
Release Time		ALCRLS = 101		0.25		s
		ALCRLS = 000		8		
PARAMETRIC EQUALIZER						
Number of Bands				5		Bands
Per Band Gain Range			-12		+12	dB
Preattenuator Gain Range		(Note 5)	-15		0	dB
Preattenuator Step Size				1		dB

Stereo Audio CODEC with FlexSound Technology

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC-TO-RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz, MCLK = 12.288MHz, f = 1kHz			96		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 25mW, R_{REC} = 32Ω			-70	-63	dB
Click and Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, AV_{REC} = 0dB	Into shutdown		-70		dBV
			Out of shutdown		-73		
PREOUTPUT MIXERS							
Level Adjust Gain	$AV_{PGAOUT\_}$	(Note 5)	PGAOUTA/PGAOUTB/ PGAOUTC = 0x0		0		dB
			PGAOUTA/PGAOUTB/ PGAOUTC = 0xC	-25	-23.4	-22	
Level Adjust Step Size					2		dB
Mute Attenuation		f = 1kHz			85		dB
LINE INPUT-TO-RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	Referenced to full-scale output level			92		dB
Total Harmonic Distortion + Noise	THD+N				-70		dB
Power-Supply Rejection Ratio	PSRR	$V_{SPKLVDD}$ = 2.8V to 5.5V		54	89		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}			-63		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}			-63		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}			-65		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, AV_{REC} = 0dB	Into shutdown		-57		dBV
			Out of shutdown		-55		
RECEIVER AMPLIFIER							
Output Power	P_{OUT}	R_{REC} = 32Ω, f = 1kHz, THD = 1%			100		mW
Full-Scale Output		(Note 7)			1		V_{RMS}
Volume Control	AV_{REC}	(Note 5)	RECVOL = 0x00	-65	-62	-58	dB
			RECVOL = 0x1F	+7.5	+8	+8.5	
Volume Control Step Size		+8dB to +6dB			0.5		dB
		+6dB to +0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -62dB			4		
Mute Attenuation		f = 1kHz			95		dB
Output Offset Voltage	V_{OS}	AV_{REC} = -62dB	T_A = +25°C		±0.13	±1	mV
Capacitive Drive Capability		No sustained oscillations	R_{REC} = 32Ω		500		pF
			R_{REC} = ∞		100		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC-TO-SPEAKER AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 250mW, Z_{SPK} = 8Ω + 68µH			-71		dB
Crosstalk		SPKL to SPKR and SPKR to SPKL, P_{OUT} = 640mW, f = 1kHz			-75		dB
Output Noise		A-weighted			43		μV_{RMS}
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{SPK\_}$ = 0dB	Into shutdown		-65		dBV
			Out of shutdown		-65		
LINE INPUT-TO-SPEAKER AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 200mW, Z_{SPK} = 8Ω + 68µH			-66		dB
Output Noise		A-weighted			56		μV_{RMS}
Power-Supply Rejection Ratio	PSRR	$V_{SPKLVDD}$ = V_{RIPPLE} = 2.8V to 5.5V		43	60		dB
		f = 217Hz, V_{RIPPLE} = 100mV			75		
		f = 1kHz, V_{RIPPLE} = 100mV			73		
		f = 10kHz, V_{RIPPLE} = 100mV			50		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{SPK\_}$ = 0dB	Into shutdown		-48		dBV
			Out of shutdown		-50		
SPEAKER AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD = 1%, Z_{SPK} = 8Ω + 68µH	$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.0V		1370		mW
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 4.2V		954		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V		733		
			$V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.2V		544		
Full-Scale Output		(Note 7)			2		V_{RMS}
Volume Control (Note 5)	$AV_{SPK\_}$	SPVOLL/SPVOLR = 0x00		-69	-64	-59	dB
		SPVOLL/SPVOLR = 0x1F		+7.5	+8	+8.5	
Volume Control Step Size		+8dB to +6dB			0.5		dB
		+6dB to +0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -64dB			4		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Mute Attenuation		f = 1kHz			86		dB
Output Offset Voltage	V_{OS}	$AV_{SPK\_}$ = -64dB, T_A = +25°C			±0.25	±1.25	mV
EXCURSION LIMITER							
Upper-Corner Frequency Range		DHPUCF = 001 to 100		400		1000	Hz
Lower-Corner Frequency		DHPLCF = 01 to 10			400		Hz
Biquad Minimum Corner Frequency		DHPUCF = 000 (fixed mode)			100		Hz
		DHPUCF = 001			200		
		DHPUCF = 010			300		
		DHPUCF = 011			400		
		DHPUCF = 100			500		
Threshold Voltage		Z_{SPK} = 8Ω + 68µH, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.5V, $AV_{SPK\_}$ = +8dB	DHPTH = 000		0.34		V_P
			DHPTH = 111		4.95		
Release Time		ALCRLS = 101			0.25		s
		ALCRLS = 000			4		
POWER LIMITER							
Attenuation					-64		dB
Threshold		Z_{SPK} = 8Ω + 68µH, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 5.5V, $AV_{SPK\_}$ = +8dB	PWRTH = 0x1		0.05		W
			PWRTH = 0xF		1.80		
Time Constant 1	t_{PWR1}	PWRT1 = 0x1			0.5		s
		PWRT1 = 0xF			8.7		
Time Constant 2	t_{PWR2}	PWRT2 = 0x1 to 0xF			0.5		min
		PWRT2 = 0xF			8.7		
Weighting Factor	k_{PWR}	PWRK = 000 to 111		12.5		100	%
DISTORTION LIMITER							
Distortion Limit		THDCLP = 0x1			< 1		%
		THDCLP = 0xF			24		
Release Time Constant		THDT1 = 000			0.76		s
		THDT1 = 111			6.2		
DAC-TO-HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	f_S = 48kHz, MCLK = 12.288MHz	Master or slave mode		100		dB
			Slave mode	94			
Total Harmonic Distortion + Noise	THD+N	f_S = 48kHz, MCLK = 12.288MHz, f = 1kHz, P_{OUT} = 20mW	R_{HP} = 16Ω		-71	-64	dB
			R_{HP} = 32Ω		-75		
		f_S = 48kHz, MCLK = 12.288MHz, f = 1kHz, V_{OUT} = $1V_{RMS}$, R_{HP} = 10kΩ			-79		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk		f = 1kHz, Input = -1dBFS, R_{HP} = 10kΩ			-82		dB
		HPL to HPR and HPR to HPL, P_{OUT} = 5mW, f = 1kHz, R_{HP} = 32Ω			-82		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{HPVDD} = 1.65V to 2.0V		60	84		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{VOL} = 0dB			92		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{VOL} = 0dB			91		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{VOL} = 0dB			57		
DAC Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from digital input to analog output	MODE = 0 (voice) 8kHz		2.2		ms
			MODE = 0 (voice) 16kHz		1.1		
			MODE = 1 (music) 8kHz		4.5		
			MODE = 1 (music) 48kHz		0.76		
Gain Error					1		%
Channel Gain Mismatch					0.5		%
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{HP\_}$ = 0dB	Into shutdown		-66		dBV
			Out of shutdown		-67		
LINE INPUT-TO-HEADPHONE AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $1V_{P-P}$, f =1kHz, R_{HP} = 32Ω			-70		dB
Dynamic Range (Note 4)	DR				91		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{HPVDD} = 1.65V to 2.0V		42	66		dB
		f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$			62		
		f = 1kHz, V_{RIPPLE} = $100mV_{P-P}$			57		
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$			41		
Click and Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{HP\_}$ = 0dB	Into shutdown		-62		dBV
			Out of shutdown		-60		
HEADPHONE AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD = 1%	R_{HP} = 32Ω		32		mW
			R_{HP} = 16Ω		40		
Full-Scale Output		(Note 7)			1		V_{RMS}
Volume Control	$AV_{HP\_}$	T_A = +25°C (Note 5)	HPVOL_ = 0x00	-71	-67	-66	dB
			HPVOL_ = 0x1F	2.4	3	3.5	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Volume Control Step Size		+3dB to +1dB			0.5		dB
		+1dB to -5dB			1		
		-5dB to -19dB			2		
		-19dB to -43dB			3		
		-43dB to -67dB			4		
Mute Attenuation		f = 1kHz			82		dB
Output Offset Voltage	V_{OS}	$AV_{HP\_}$ = -67dB	T_A = +25°C		±0.2	±1	mV
			T_A = T_{MIN} to T_{MAX}			±2	
Capacitive Drive Capability		No sustained oscillations	R_{HP} = 32Ω		500		pF
			R_{HP} = ∞		100		
Charge Pump Oscillator Frequency	f_{CP}			300	667	900	kHz
		Slow mode			74		
SPEAKER BYPASS SWITCH							
On-Resistance	R_{ON}	$I_{SPKL\_}$ = 100mA, SPKBYP = 1, $V_{RXIN\_}$ = [0V, $V_{SPKLVDD}$]			2.8	4.5	Ω
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, Z_{SPK} = 8Ω + 68µH, f = 1kHz, SPKBYP = 1	R_S = 10Ω		-77		dB
			R_S = 0Ω		-60		
Off-Isolation		V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, Z_L = 8Ω + 68µH, f = 1kHz			96		dB
Off-Leakage Current		$V_{RXIN\_}$ = [0V, $V_{SPKLVDD}$], $V_{SPKL\_}$ = [$V_{SPKLVDD}$, 0V]		-1		+1	µA
RECEIVER BYPASS SWITCH							
On-Resistance	R_{ON}	I_{RECP} = 100mA, RECBYP = 1, V_{RECN} = [0V, $V_{SPKLVDD}$]			1.2	2	Ω
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, R_L = 32Ω, f = 1kHz, RECBYP = 1			-66		%
Off-Isolation		V_{IN} = $2V_{P-P}$, V_{CM} = $V_{SPKLVDD}$/2, R_L = 32Ω, f = 1kHz			80		dB
Off-Leakage Current		V_{RECP} = [0V, $V_{SPKLVDD}$], V_{RECN} = [$V_{SPKLVDD}$, 0V]		-15		+15	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JACK DETECTION						
JACKSNS High Threshold	V_{TH1}	MICBIAS enabled	0.92 x $V_{MICBIAS}$	0.95 x $V_{MICBIAS}$	0.98 x $V_{MICBIAS}$	V
		MICBIAS disabled	0.92 x $V_{SPKLVDD}$	0.95 x $V_{SPKLVDD}$	0.98 x $V_{SPKLVDD}$	
JACKSNS Low Threshold	V_{TH2}	MICBIAS enabled	0.06 x $V_{MICBIAS}$	0.10 x $V_{MICBIAS}$	0.17 x $V_{MICBIAS}$	V
		MICBIAS disabled	0.06 x $V_{SPKLVDD}$	0.10 x $V_{SPKLVDD}$	0.17 x $V_{SPKLVDD}$	
JACKSNS Sense Voltage	V_{SENSE}	MICBIAS disabled		$V_{SPKLVDD}$		V
JACKSNS Sense Resistance	R_{SENSE}	MICBIAS disabled, JDWK = 0	1.7	2.4	2.9	kΩ
JACKSNS Weak Pullup Current	I_{WPU}	MICBIAS disabled, JDWK = 1	2	5	9.5	µA
JACKSNS Deglitch Period	t_{GLITCH}	JDEB = 00		25		ms
		JDEB = 11		200		
BATTERY ADC						
Input Voltage Range			2.8		5.5	V
LSB Size				0.1		V

DIGITAL INPUT/OUTPUT CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.65V to 2.0V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
SDINS1, BCLKS1, LRCLKS1—INPUT						
Input High Voltage	V_{IH}		0.7 x DVDDS1			V
Input Low Voltage	V_{IL}				0.29 x DVDDS1	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDS1} = 3.6V, V_{IN} = 0V, 3.6V; T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF

DIGITAL INPUT/OUTPUT CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.65V to 2.0V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BCLKS1, LRCLKS1, SDOUTS1—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDS1} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDS1} = 1.65V, I_{OH} = 3mA	DVDDS1 - 0.4			V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V; T_A = +25°C, high-impedance state	-1		+1	µA
SDINS2, BCLKS2, LRCLKS2—INPUT						
Input High Voltage	V_{IH}		0.7 x DVDDS2			V
Input Low Voltage	V_{IL}				0.29 x DVDDS2	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDS2} = 3.6V, V_{IN} = 0V, 3.6V; T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
BCLKS2, LRCLKS2, SDOUTS2—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDS2} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDS2} = 1.65V, I_{OH} = 3mA	DVDDS2 - 0.4			V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V; T_A = +25°C, high-impedance state	-1		+1	µA
SDA, SCL—INPUT						
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Input Hysteresis				210		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
SDA, $\overline{IRQ}$—OUTPUT						
Output High Current	I_{OH}	V_{OUT} = 5.5V, T_A = +25°C			1	mA
Output Low Voltage	V_{OL}	V_{DVDD} = 1.65V, I_{OL} = 3mA			0.2 x DVDD	V
DIGMICDATA—INPUT						
Input High Voltage	V_{IH}		0.65 x DVDD			V
Input Low Voltage	V_{IL}				0.35 x DVDD	V
Input Hysteresis				125		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 2.0V; T_A = +25°C	-25		+25	µA
Input Capacitance				10		pF

DIGITAL INPUT/OUTPUT CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.65V to 2.0V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGMICCLK—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDD} = 1.65V, I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDD} = 1.65V, I_{OH} = 1mA	DVDD - 0.4			V

INPUT CLOCK CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK Input Frequency	f_{MCLK}		10		60	MHz
MCLK Input Duty Cycle		PSCLK = 01	40	50	60	%
		PSCLK = 10 or 11	30		70	
Maximum MCLK Input Jitter				100		ps_{RMS}
LRCLK Sample Rate (Note 8)		DHF_ = 0	8		48	kHz
		DHF_ = 1	48		96	
DAI1 LRCLK Average Frequency Error (Note 9)		FREQ1 = 0x8 to 0xF	0		0	%
		FREQ1 = 0x0	-0.025		+0.025	
DAI2 LRCLK Average Frequency Error (Note 9)			-0.025		+0.025	%
PLL Lock Time		Rapid lock mode		2	7	ms
		Nonrapid lock mode		12	25	
Maximum LRCLK Jitter to Maintain PLL Lock					100	ns
Soft-Start/Stop Time				10		ms

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AUDIO INTERFACE TIMING CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.65V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BCLK Cycle Time	t_{BCLK}	Slave mode		90			ns
BCLK High Time	t_{BCLKH}	Slave mode		20			ns
BCLK Low Time	t_{BCLKL}	Slave mode		20			ns
BCLK or LRCLK Rise and Fall Time	t_R, t_F	Master mode, C_L = 15pF					ns
SDIN to BCLK Setup Time	t_{SETUP}			20			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$	Slave mode		20			ns
SDIN to BCLK Hold Time	t_{HOLD}			20			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$	Slave mode		20			ns
Minimum Delay Time from LSB BCLK Falling Edge to High-Impedance State	t_{HIZOUT}	Master mode, TDM_ = 1			42		ns
LRCLK Rising Edge to SDOUT MSB Delay	t_{SYNCTX}	C_L = 30pF, TDM_ = 1, FSW_ = 1				50	ns
BCLK to SDOUT Delay	t_{CLKTX}	C_L = 30pF	TDM_ = 1, BCLK rising edge			50	ns
			TDM_ = 0			50	
Delay Time from BCLK to LRCLK	$t_{CLKSYNC}$	Master mode	TDM_ = 1	-15		+15	ns
			TDM_ = 0			0.8 x t_{BCLKL}	
Delay Time from LRCLK to BCLK After LSB	$t_{ENDSYNC}$	Master mode	TDM_ = 1, FSW_ = 1	20			ns

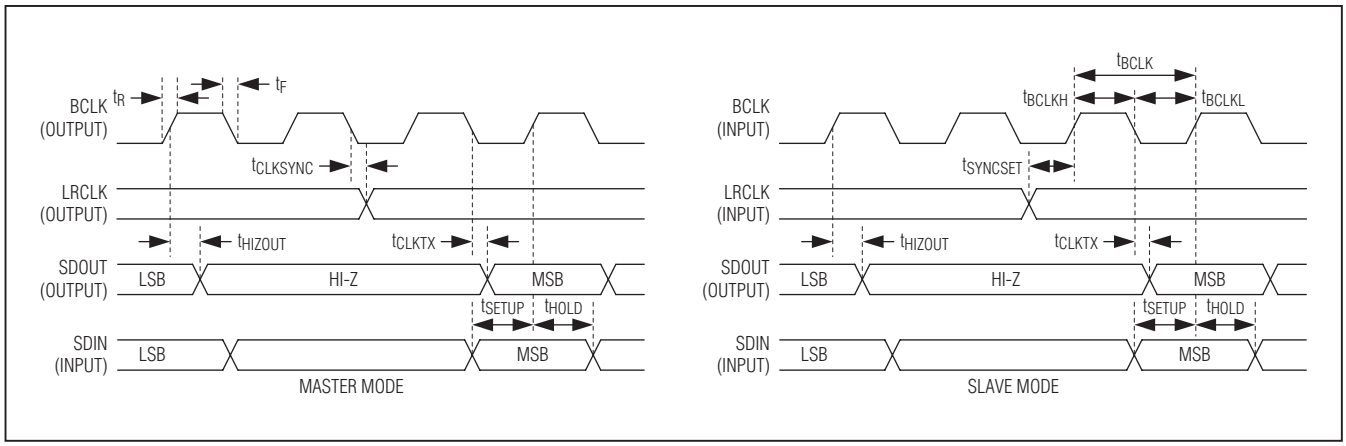

Figure 1. Non-TDM Audio Interface Timing Diagrams (TDM_ = 0)

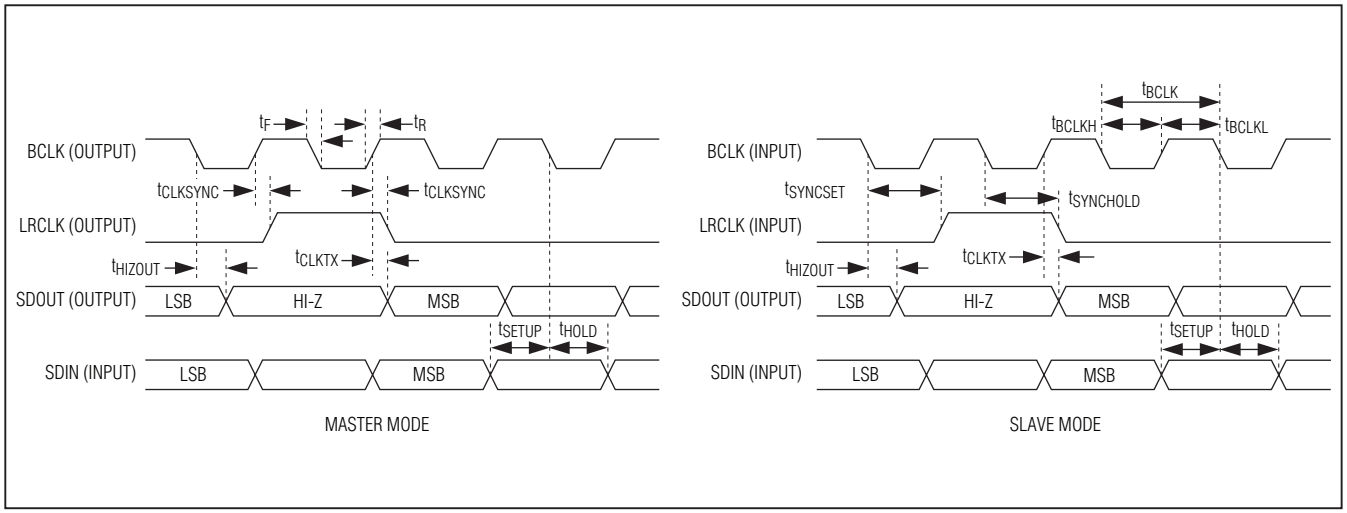

Figure 2. TDM Audio Interface Timing Diagram (TDM_ = 1, FSW_ = 0)

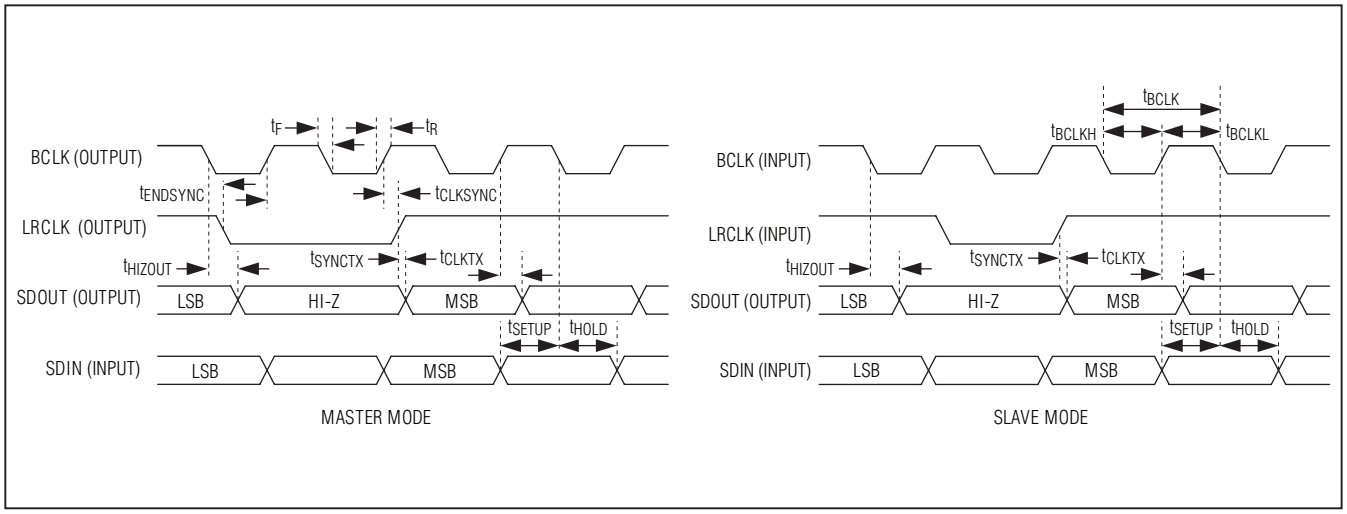

Figure 3. TDM Audio Interface Timing Diagram (TDM_ = 1, FSW_ = 1)

DIGITAL MICROPHONE TIMING CHARACTERSTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 2.0V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGMICCLK Frequency	f_{MICCLK}	MICCLK = 00		MCLK/8		MHz
		MICCLK = 01		MCLK/6		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU,MIC}$	Either clock edge	20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD,MIC}$	Either clock edge	0			ns

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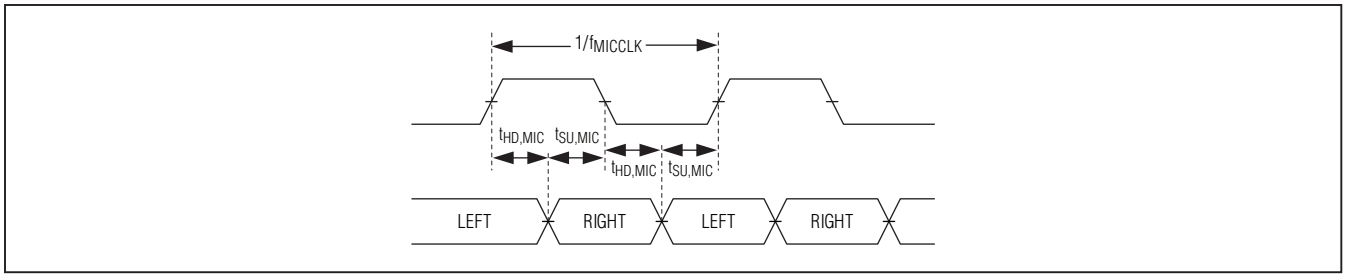

Figure 4. Digital Microphone Timing Diagram

I²C TIMING CHARACTERSTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = 1.65V to 2.0V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}	Guaranteed by SCL pulse-width low and high	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	R_{PU} = 475Ω, CB = 100pF, 400pF	0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	R_{PU} = 475Ω, C_B = 100pF, 400pF (Note 10)	20 + 0.05C_B		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B	Guaranteed by SDA transmitting fall time			400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

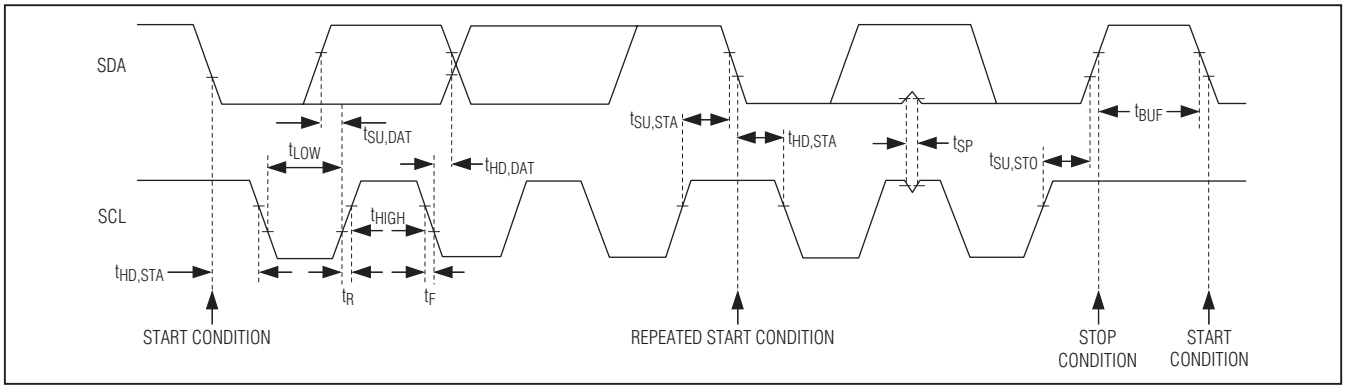

Figure 5. I²C Interface Timing Diagram

Note 1: The IC is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Analog supply current = I_{AVDD} + I_{HPVDD}. Speaker supply current = $I_{SPKLVDD}$ + $I_{SPKRVDD}$. Digital supply current = I_{DVDD} + I_{DVDDS1} + I_{DVDDS2}.
Note 3: Clocking all zeros into the DAC. Slave mode.
Note 4: Dynamic range measured using the EIAJ method. -60dBFS, 1kHz output signal, A-weighted and normalized to 0dBFS. f = 20Hz to 20kHz.
Note 5: Gain measured relative to the 0dB setting.
Note 6: The filter specification is accurate only for synchronous clocking modes, where NI is a multiple of 0x1000.
Note 7: 0dBFS for DAC input. $1V_{P-P}$ for INA/INB inputs.
Note 8: LRCLK may be any rate in the indicated range. Asynchronous or noninteger MCLK/LRCLK ratios may exhibit some full-scale performance degradation compared to synchronous integer related MCLK/LRCLK ratios.
Note 9: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 10: CB is in pF.

Power Consumption

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V)

MODE	I_{AVDD} (mA)	I_{HPVDD} (mA)	$I_{SPKLVDD}$ + $I_{SPKRVDD}$ (mA)	I_{DVDD} (mA)	I_{DVDDS1} + I_{DVDDS2} (mA)	POWER (mW)
DAC Playback 48kHz Stereo HP DAC → HP 24-bit, music filters	1.35	1.37	1.65	2.91	0.02	16.25
DAC Playback 48kHz Stereo HP DAC → HP 24-bit, music filters, 0.1mW/channel, R_{HP} = 32Ω	1.35	4.19	1.65	3.02	0.02	21.55
DAC Playback 48kHz Stereo HP DAC → HP 24-bit, music filters, ALC enabled	1.35	1.37	1.65	2.96	0.02	16.36

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Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V)

MODE	I_{AVDD} (mA)	I_{HPVDD} (mA)	$I_{SPKLVDD}$ + $I_{SPKRVDD}$ (mA)	I_{DVDD} (mA)	I_{DVDDS1} + I_{DVDDS2} (mA)	POWER (mW)
DAC Playback 48kHz Stereo HP DAC → HP 24-bit, music filters, EQ enabled	1.35	1.36	1.65	3.27	0.02	16.90
DAC Playback 48kHz Stereo HP DAC → HP 24-bit, music filters, digital mixing	1.34	1.36	1.65	2.91	0.02	16.27
DAC Playback 44.1kHz Stereo HP DAC → HP 24-bit, music filters	1.35	1.37	1.69	2.85	0.02	16.29
DAC Playback 8kHz Stereo HP DAC → HP 16-bit, voice filters	1.35	1.37	1.65	1.46	0.01	13.65
DAC Playback 8kHz Mono HP DAC → HP 16-bit, voice filters	1.00	0.71	1.01	1.36	0.01	9.27
DAC Playback 48kHz Stereo SPK DAC → SPK 24-bit, music filters	1.83	0.02	8.22	2.92	0.02	39.09
DAC Playback 48kHz Mono SPK DAC → SPK 24-bit, music filters	1.25	0.02	4.31	2.82	0.02	23.32
Line Stereo Record 48kHz INA → ADC 16-bit, music filters	9.91	0.02	0.39	1.62	0.11	22.48
Line Stereo Record 48kHz, Stereo HP INA → ADC INA → HP 16-bit, music filters	10.64	2.65	0.66	1.63	0.11	29.51
Line Stereo Record 48kHz, Stereo SPK INA → ADC INA → SPK 16-bit, music filters	10.97	0.03	7.15	1.63	0.12	49.50
Differential Line Record 48kHz INA → ADCL INB → ADCR Differential input	10.49	0.02	0.39	1.63	0.16	23.58
Microphone Stereo Record 48kHz MIC1/2 → ADC 16-bit, music filters	10.88	0.03	0.69	1.62	0.17	25.43
Microphone Stereo Record 8kHz MIC1/2 → ADC 16-bit, voice filters	10.77	0.02	0.64	1.03	0.06	23.78

Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V)

MODE	I_{AVDD} (mA)	I_{HPVDD} (mA)	$I_{SPKLVDD}$ + $I_{SPKRVDD}$ (mA)	I_{DVDD} (mA)	I_{DVDDS1} + I_{DVDDS2} (mA)	POWER (mW)
Microphone Mono Record 48kHz MIC1/2 → ADC 16-bit, music filters	6.01	0.02	0.66	1.37	0.10	15.97
Microphone Mono Record 8kHz MIC1/2 → ADC 16-bit, voice filters	5.95	0.02	0.64	0.98	0.04	14.94
Microphone Mono Record 8kHz MIC1/2 → ADC 16-bit, voice filters, AGC	5.95	0.02	0.64	0.98	0.04	15.00
Microphone Mono Record 8kHz MIC1/2 → ADC 16-bit, voice filters, AGC, noise gate	5.96	0.02	0.64	0.98	0.04	14.98
Full-Duplex 48kHz Stereo HP MIC1/2 → ADC DAC → HP 24-bit, music filters	11.38	1.37	1.70	3.56	0.19	36.06
Full-Duplex 8kHz Mono RCV MIC1 → ADC DAC → REC 16-bit, voice filters	6.35	0.02	1.98	1.47	0.03	21.47
Full-Duplex 8kHz Mono HP MIC1 → ADC DAC → HP 16-bit, voice filters	6.09	0.71	1.01	1.46	0.03	18.72
Full-Duplex 8kHz Stereo HP MIC1/2 → ADC DAC → HP 16-bit, voice filters	10.92	1.37	1.09	1.51	0.05	28.95
Line Playback Stereo HP INA → HP Single-ended inputs	1.89	2.65	0.58	0.03	0.01	10.41
Line Playback Stereo SPK INA → SPK Single-ended inputs	2.21	0.02	7.05	0.04	0.02	30.19
Line Playback Mono SPK INA → SPK Single-ended inputs	1.68	0.02	3.70	0.03	0.02	16.90
Differential Line Playback Stereo HP INA → HPL INB → HPR Differential input	2.46	2.65	0.58	0.03	0.01	11.42

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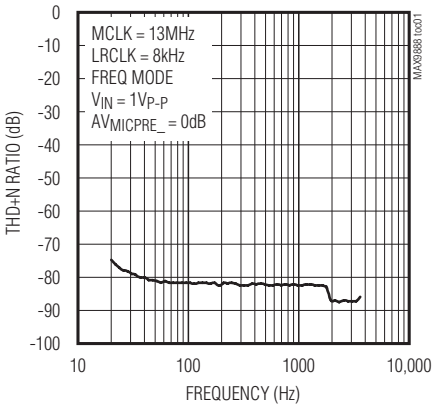
Typical Operating Characteristics

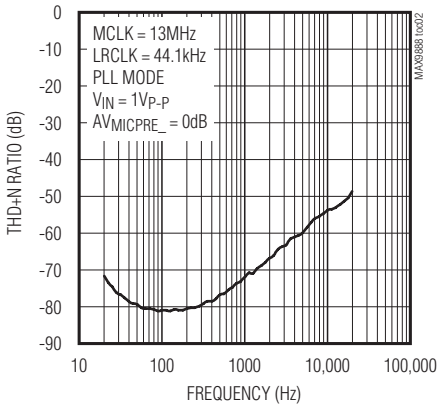
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Microphone to ADC

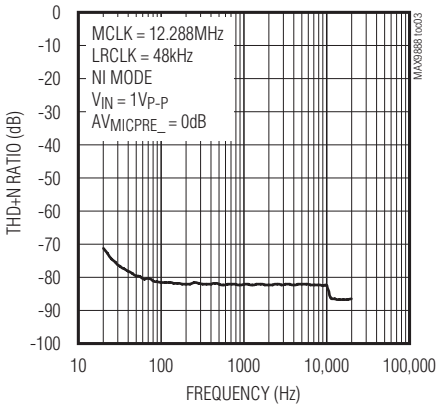
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



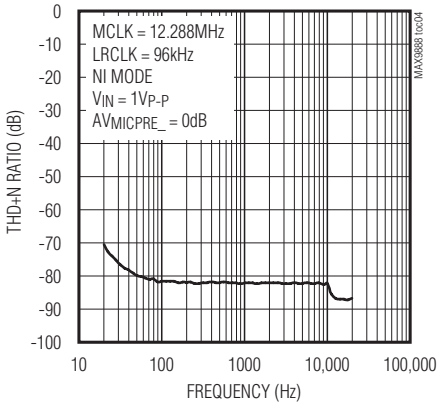
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



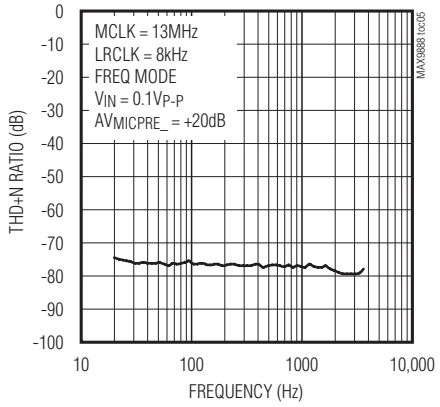
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



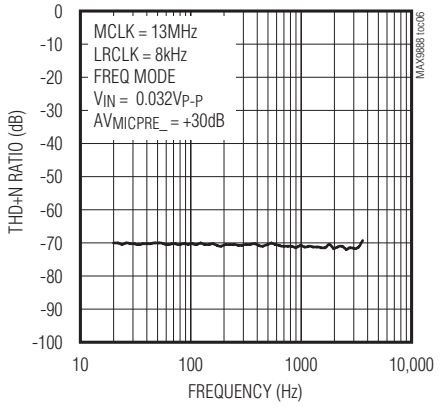
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



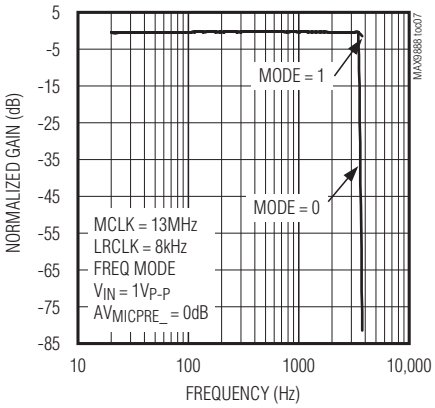
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



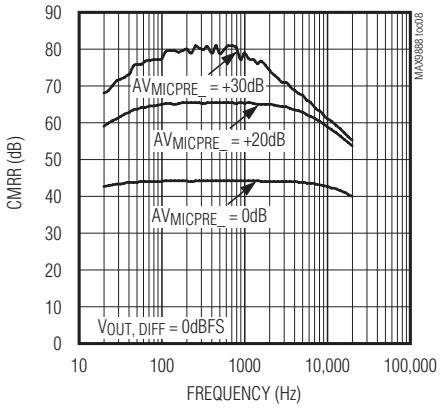
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

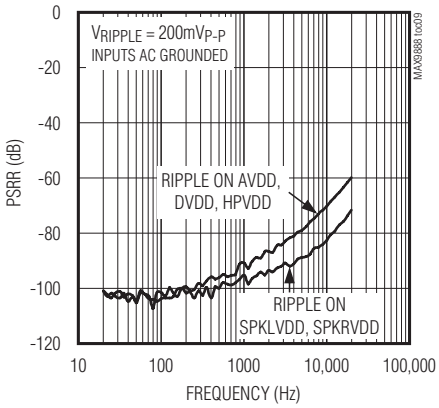
GAIN vs. FREQUENCY (MIC TO ADC)



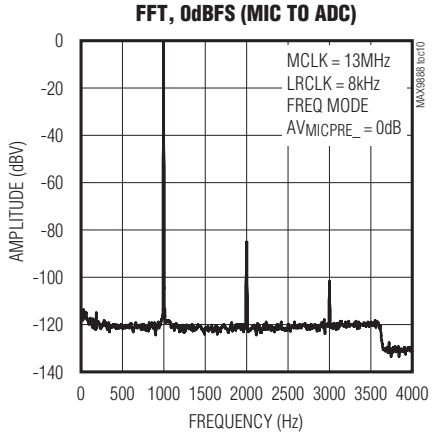
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



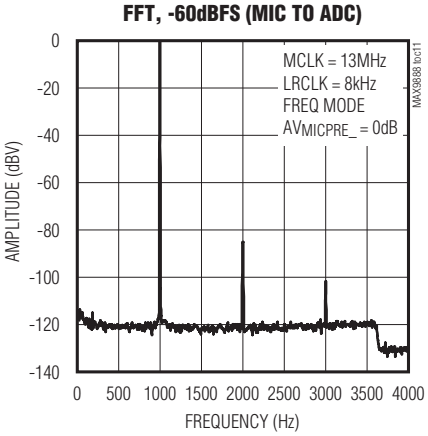
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



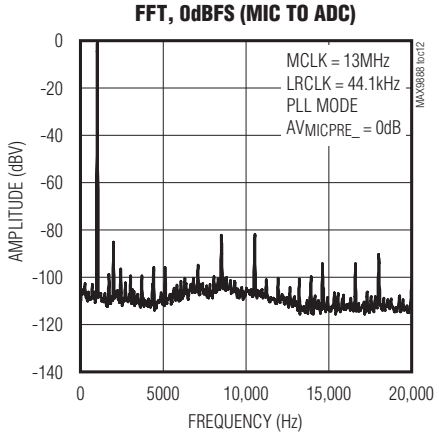
FFT, 0dBFS (MIC TO ADC)



FFT, -60dBFS (MIC TO ADC)



FFT, 0dBFS (MIC TO ADC)

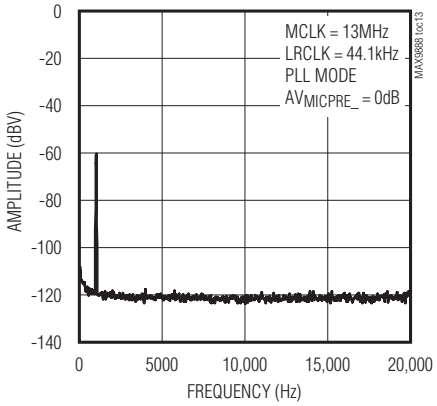


Stereo Audio CODEC with FlexSound Technology

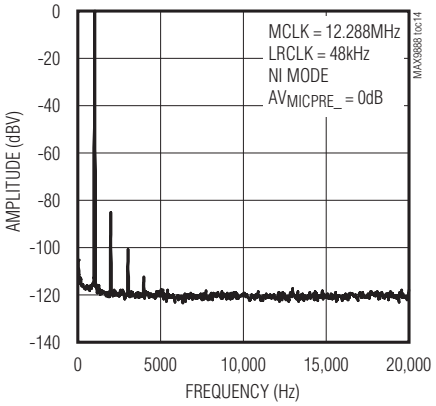
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

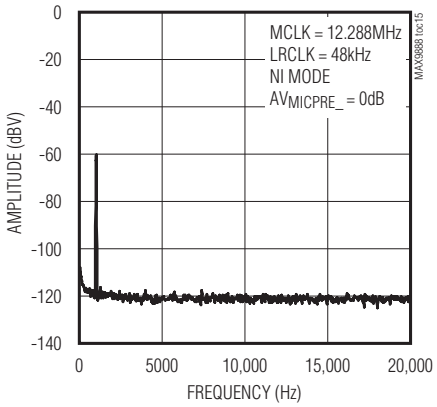
FFT, -60dBFS (MIC TO ADC)



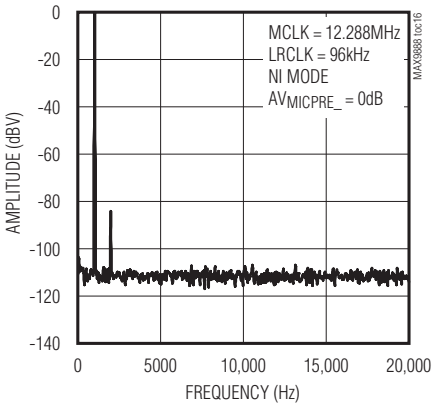
FFT, 0dBFS (MIC TO ADC)



FFT, -60dBFS (MIC TO ADC)



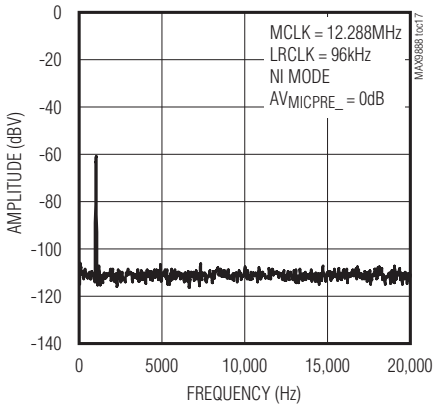
FFT, 0dBFS (MIC TO ADC)



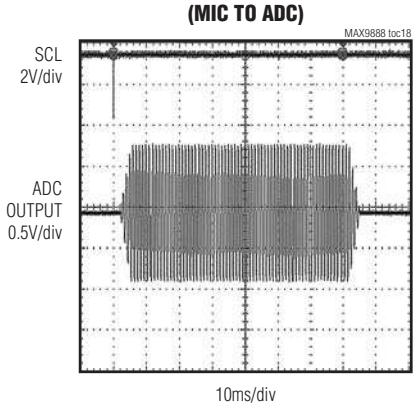
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

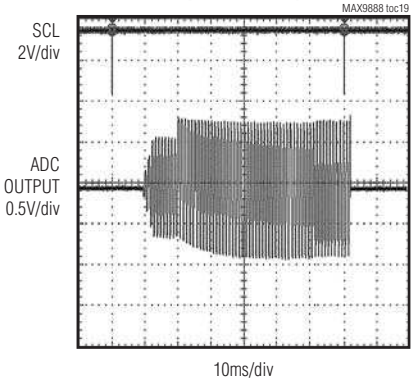
FFT, -60dBFS (MIC TO ADC)



ADC ENABLE/DISABLE RESPONSE (MIC TO ADC)



SOFTWARE TURN-ON/OFF RESPONSE (MIC TO ADC)



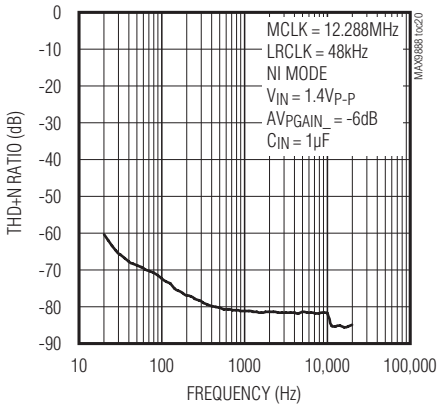
Stereo Audio CODEC with FlexSound Technology

Typical Operating Characteristics (continued)

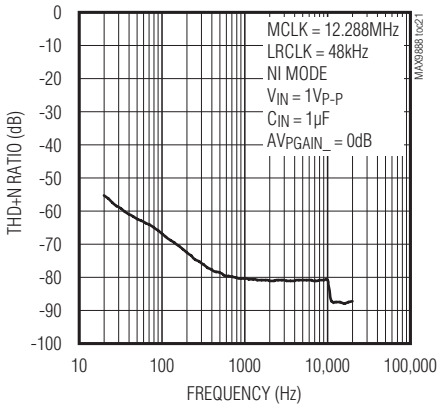
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Line to ADC

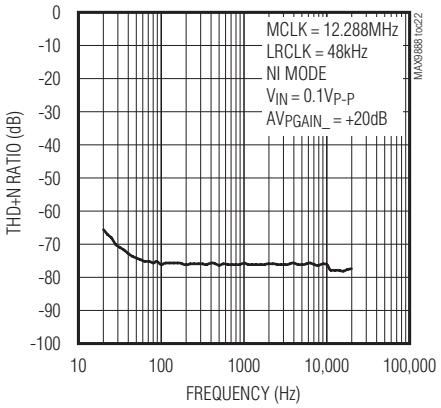
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



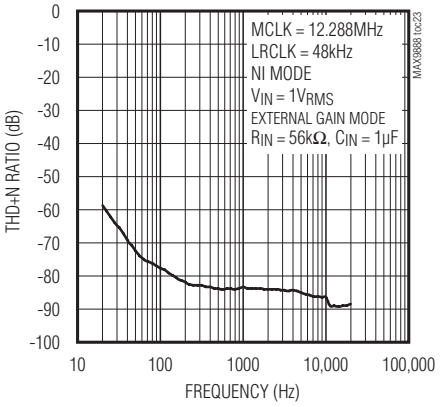
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



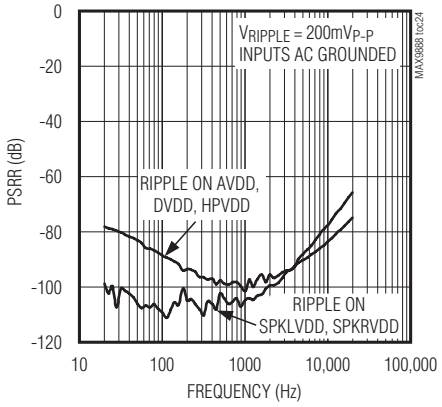
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO ADC)

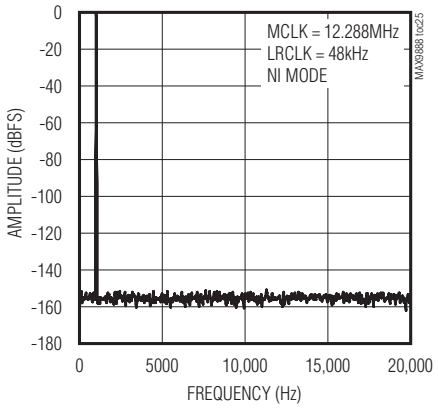


Typical Operating Characteristics (continued)

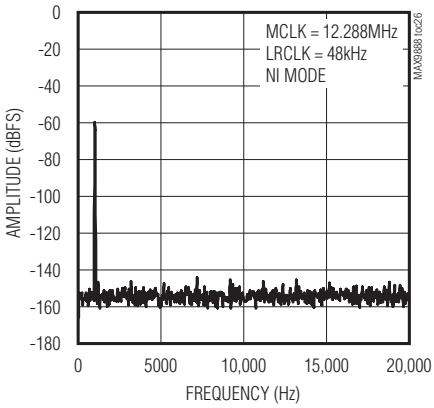
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Digital Loopback

FFT, 0dBFS
(SDINS1 TO SDOUTS2 DIGITAL LOOPBACK)



FFT, -60dBFS
(SDINS1 TO SDOUTS2 DIGITAL LOOPBACK)



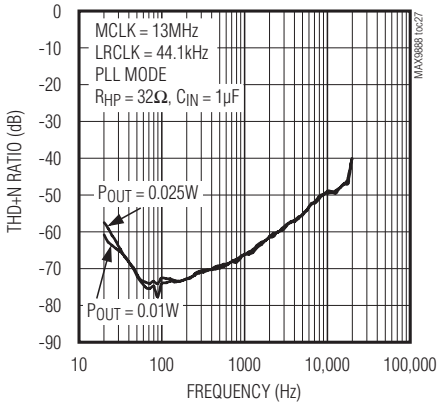
Stereo Audio CODEC with FlexSound Technology

Typical Operating Characteristics (continued)

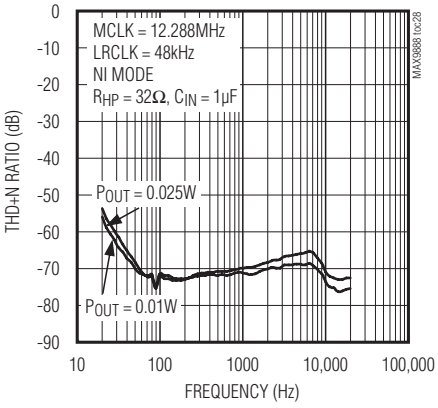
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Analog Loopback

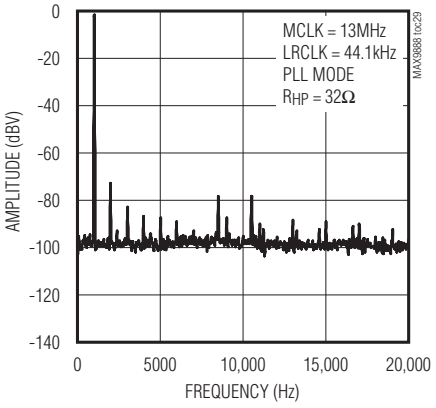
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



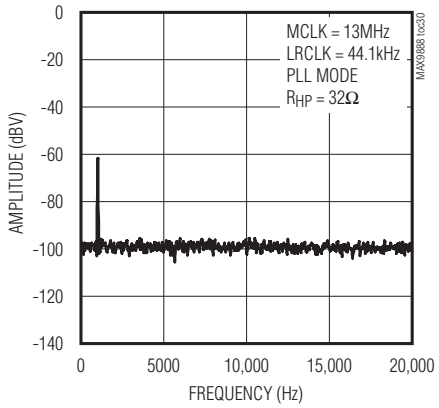
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



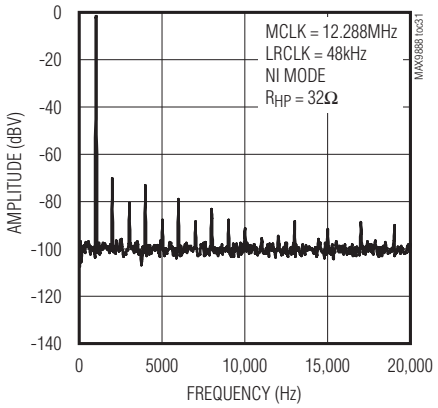
FFT, 0dBFS (LINE TO ADC TO DAC TO HEADPHONE)



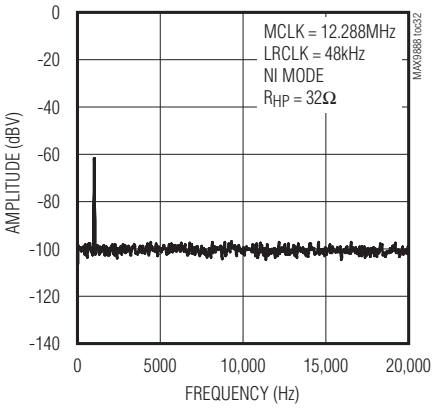
FFT, -60dBFS (LINE TO ADC TO DAC TO HEADPHONE)



FFT, 0dBFS (LINE TO ADC TO DAC TO HEADPHONE)



FFT, -60dBFS (LINE TO ADC TO DAC TO HEADPHONE)

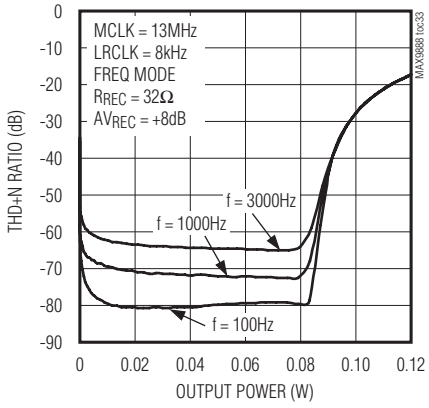


Typical Operating Characteristics (continued)

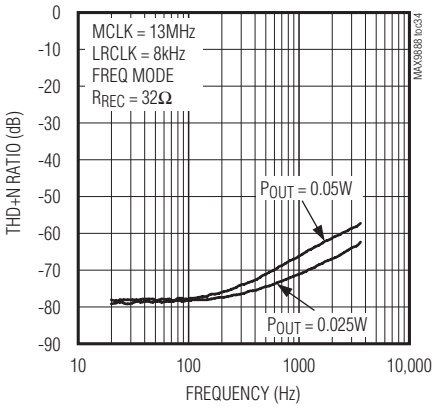
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC to Receiver

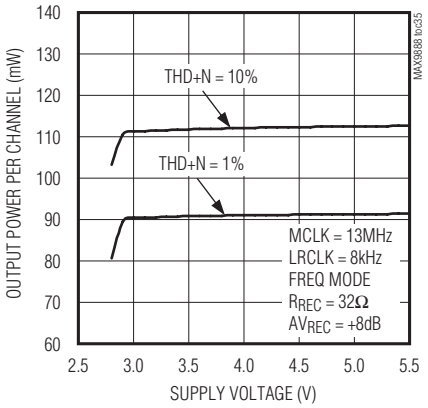
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER (DAC TO RECEIVER)



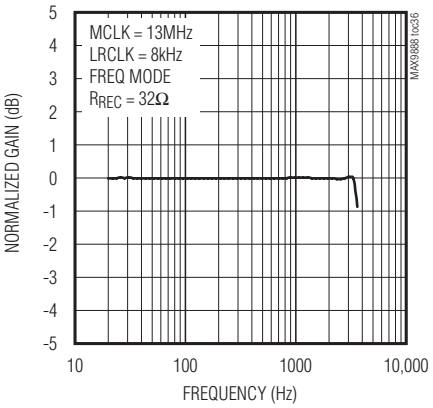
TOTAL HARMONIC DISTORTION vs. FREQUENCY (DAC TO RECEIVER)



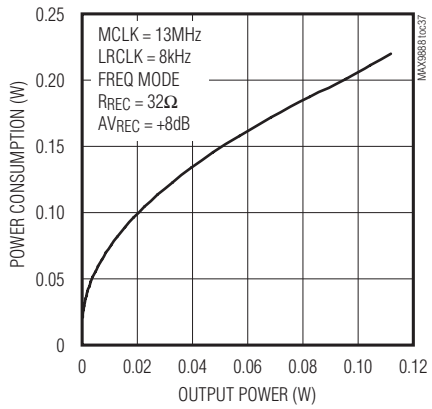
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO RECEIVER)



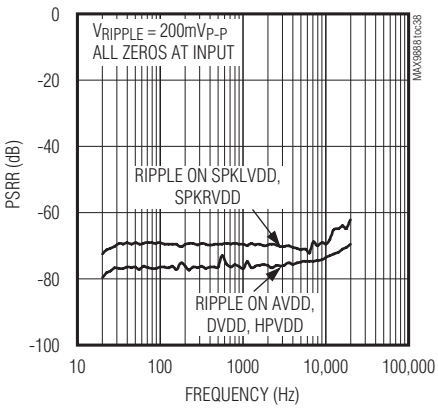
GAIN vs. FREQUENCY (DAC TO RECEIVER)



POWER CONSUMPTION vs. OUTPUT POWER (DAC TO RECEIVER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO RECEIVER)

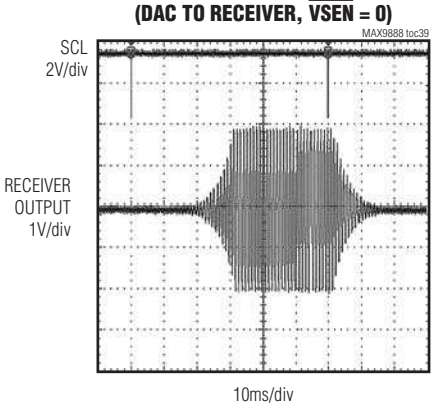


Stereo Audio CODEC with FlexSound Technology

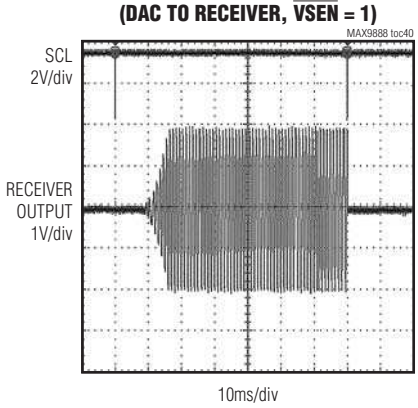
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

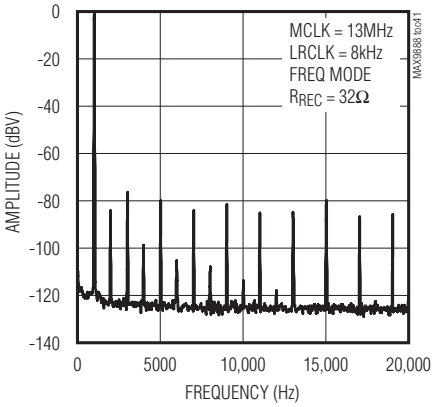
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO RECEIVER, $\overline{VSEN}$ = 0)



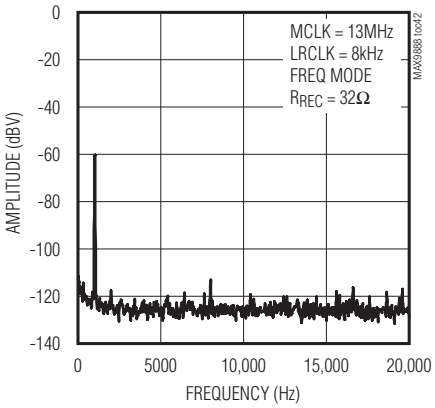
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO RECEIVER, $\overline{VSEN}$ = 1)



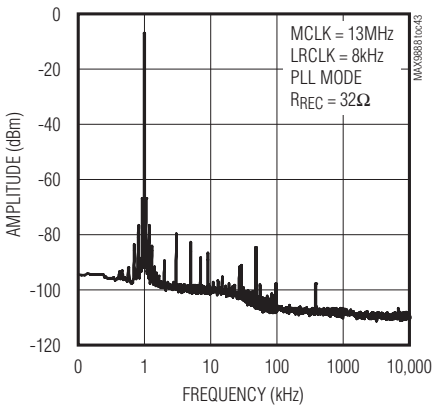
FFT, 0dBFS (DAC TO RECEIVER)



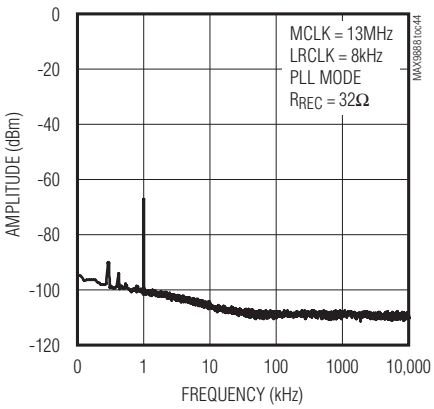
FFT, -60dBFS (DAC TO RECEIVER)



WIDEBAND FFT, 0dBFS (DAC TO RECEIVER)



WIDEBAND FFT, -60dBFS (DAC TO RECEIVER)

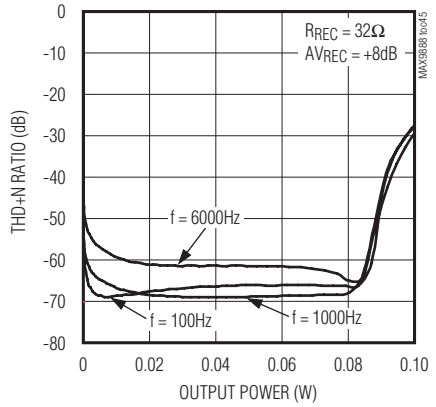


Typical Operating Characteristics (continued)

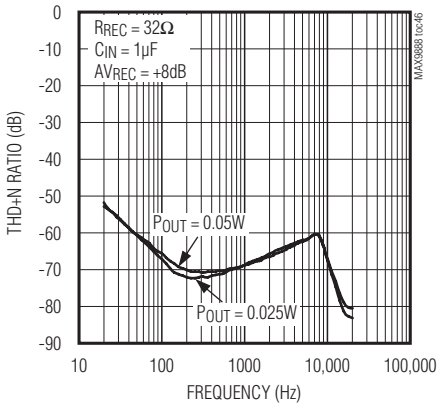
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Line to Receiver

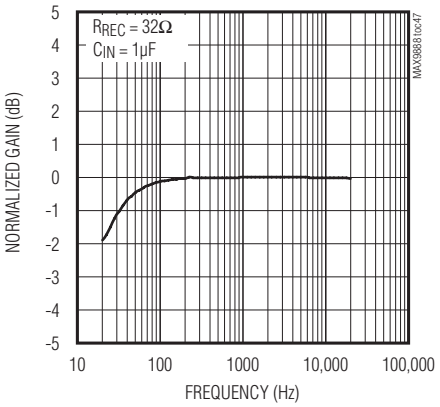
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)



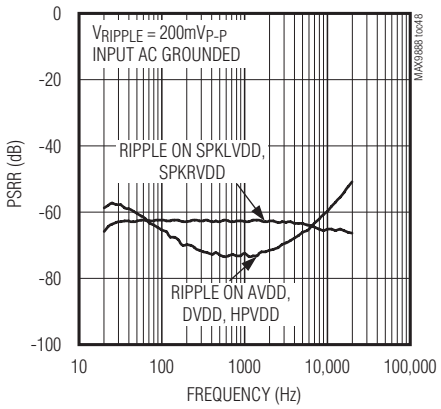
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO RECEIVER)



GAIN vs. FREQUENCY (LINE TO RECEIVER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO RECEIVER)



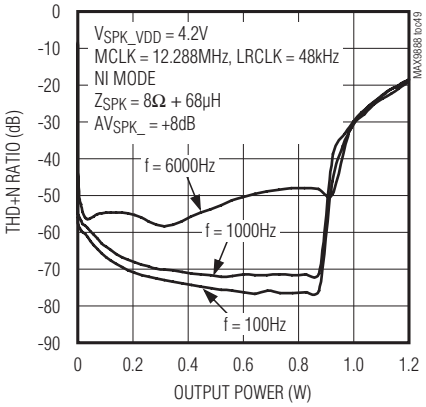
Stereo Audio CODEC with FlexSound Technology

Typical Operating Characteristics (continued)

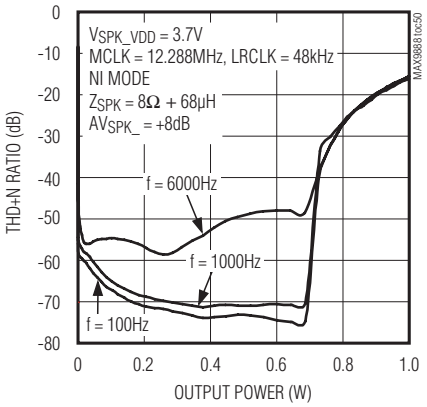
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC to Speaker

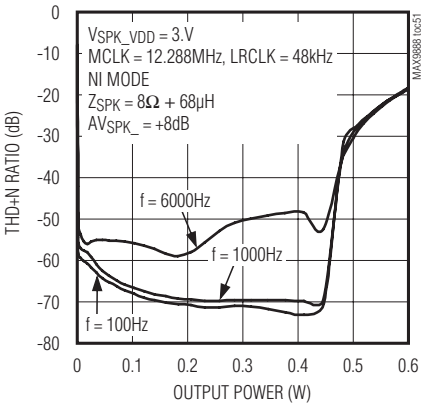
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



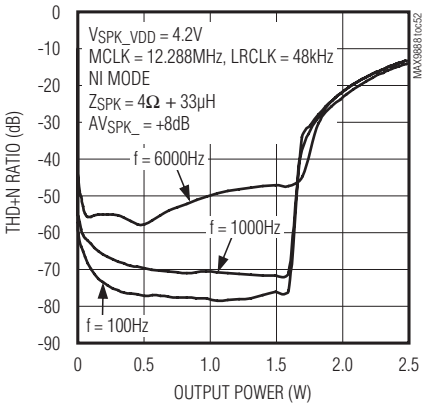
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



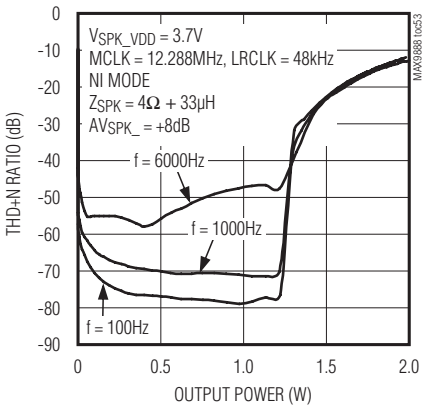
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



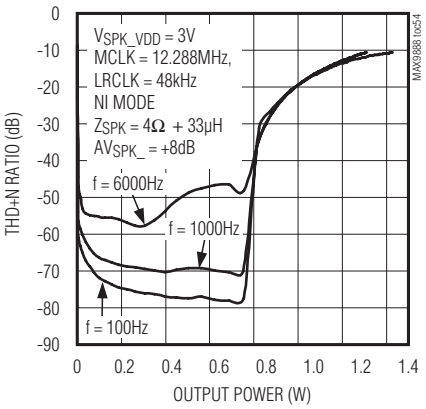
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



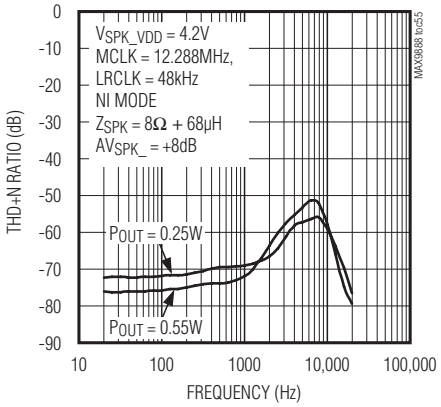
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



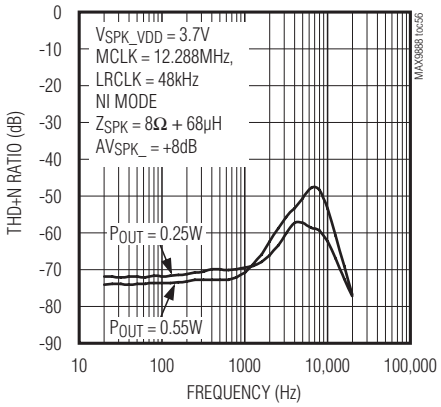
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

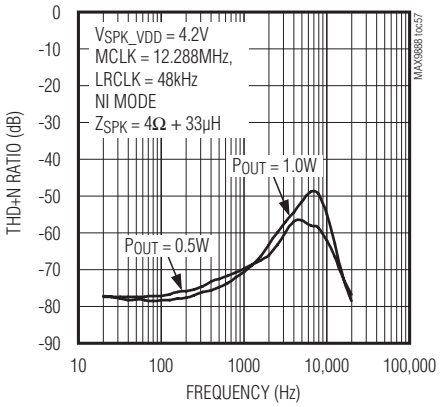
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



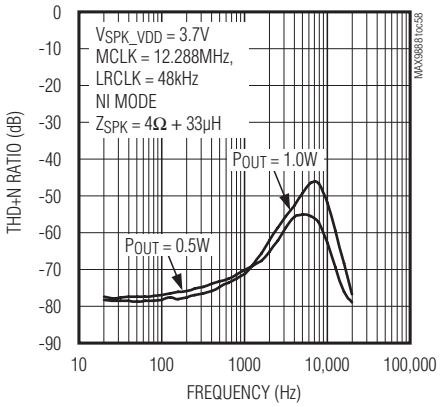
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



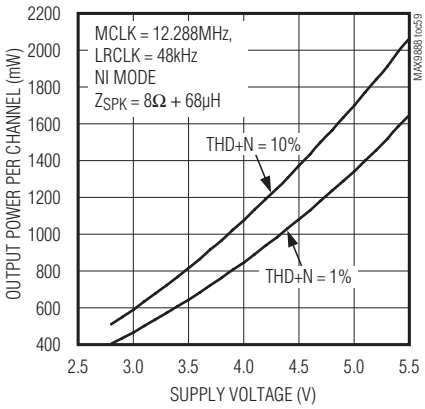
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



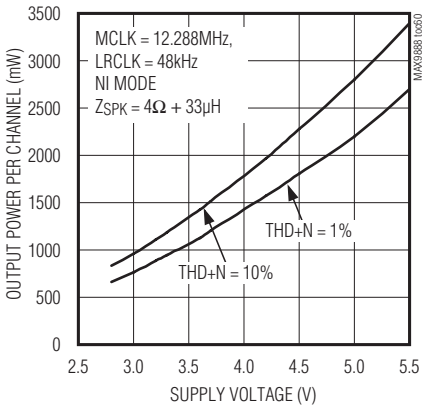
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)

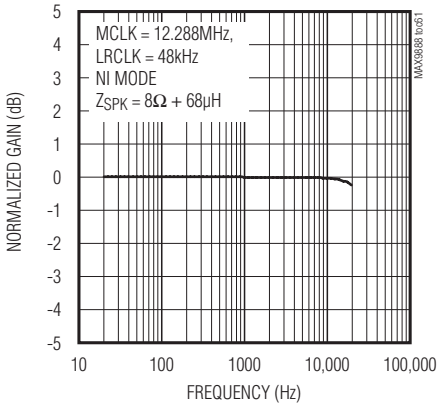


Stereo Audio CODEC with FlexSound Technology

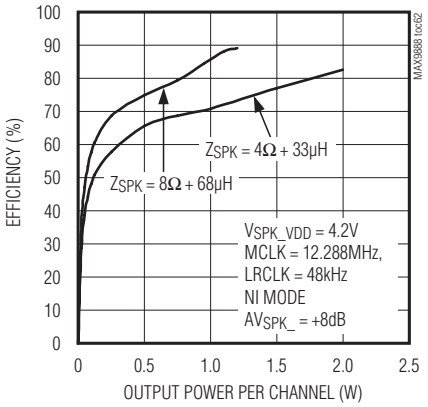
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

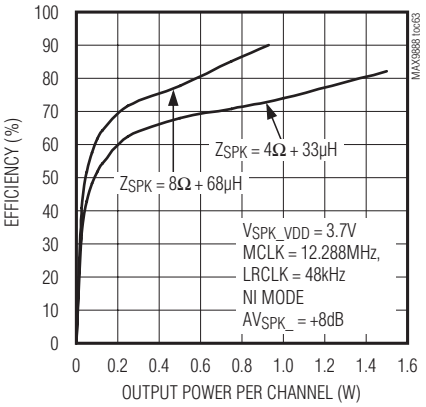
GAIN vs. FREQUENCY (DAC TO SPEAKER)



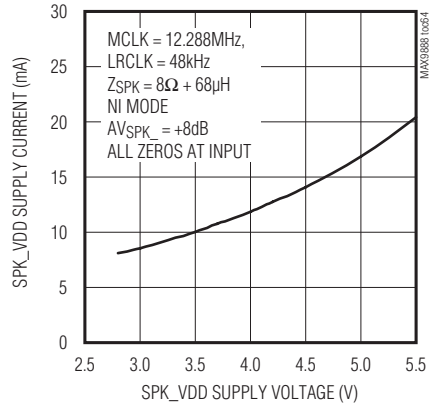
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



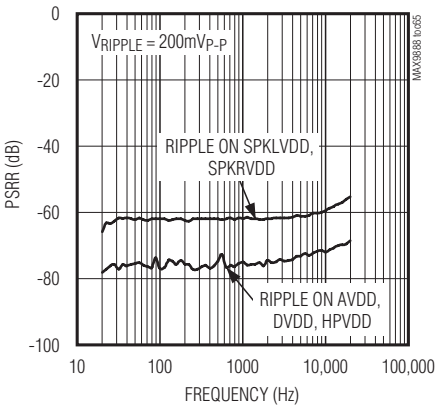
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



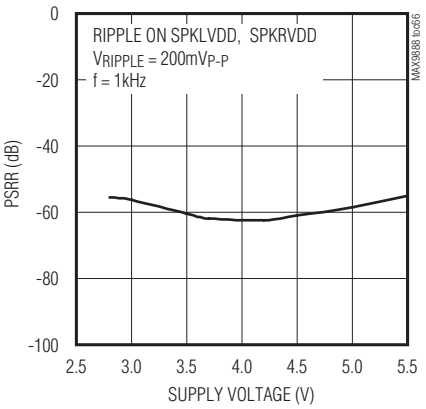
SUPPLY CURRENT vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO SPEAKER)



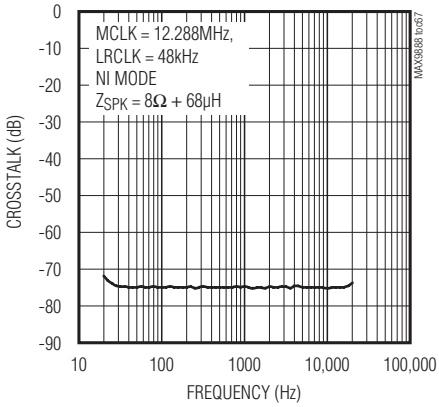
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



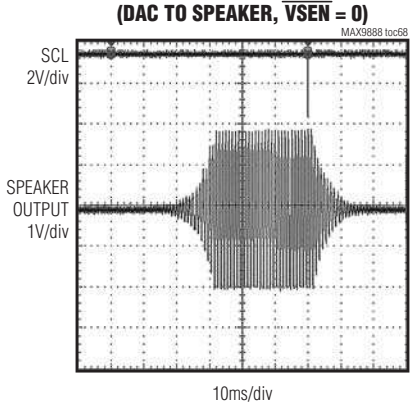
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

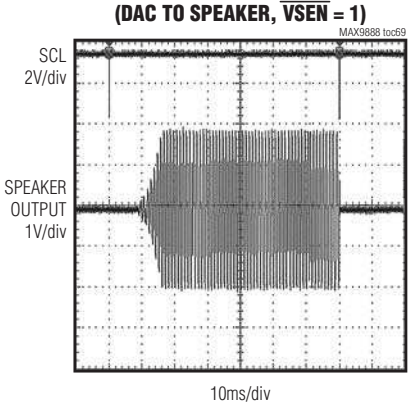
CROSSTALK vs. FREQUENCY (DAC TO SPEAKER)



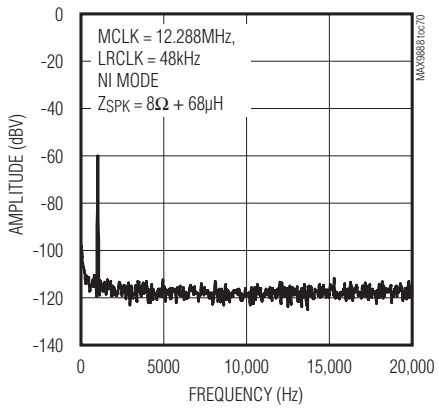
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO SPEAKER, $\overline{VSEN}$ = 0)



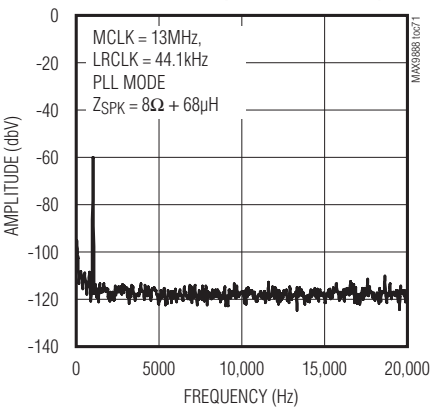
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO SPEAKER, $\overline{VSEN}$ = 1)



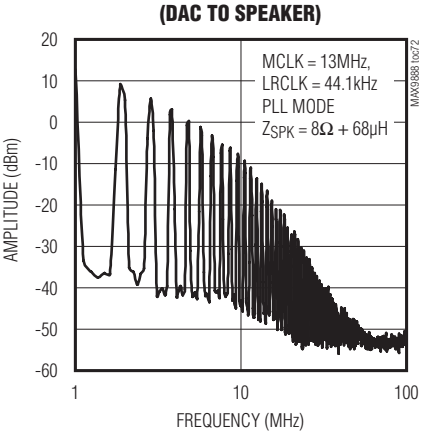
FFT, -60dBFS (DAC TO SPEAKER)



FFT, -60dBFS (DAC TO SPEAKER)



WIDEBAND FFT (DAC TO SPEAKER)



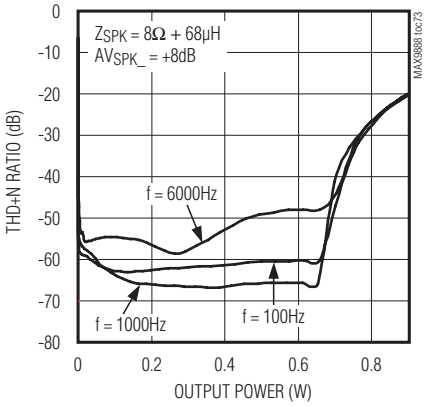
Stereo Audio CODEC with FlexSound Technology

Typical Operating Characteristics (continued)

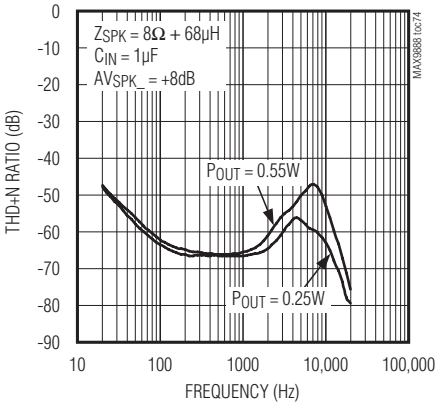
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Line to Speaker

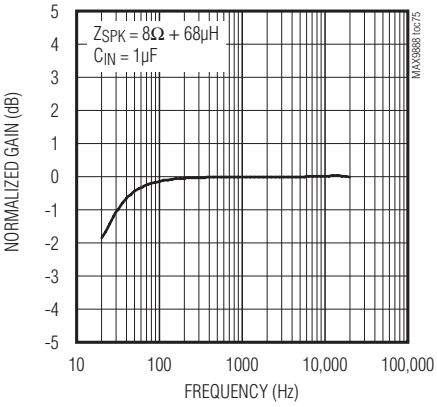
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO SPEAKER)



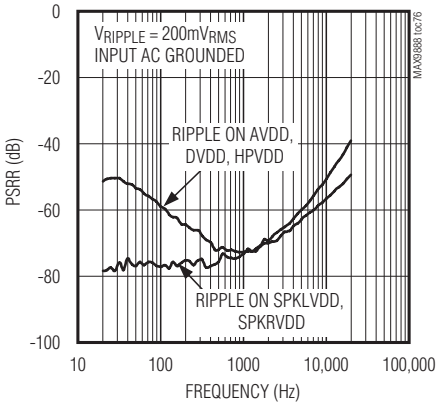
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO SPEAKER)



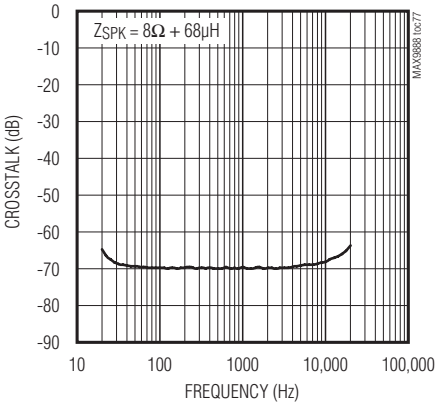
GAIN vs. FREQUENCY (LINE TO SPEAKER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO SPEAKER)



CROSSTALK vs. FREQUENCY (LINE TO SPEAKER)

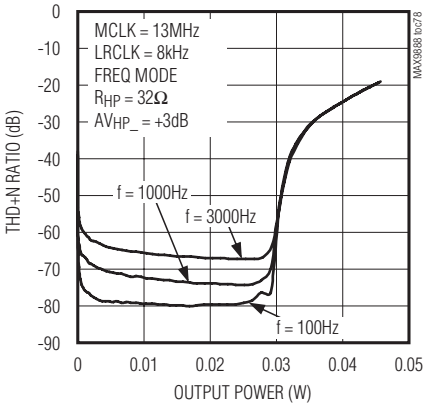


Typical Operating Characteristics (continued)

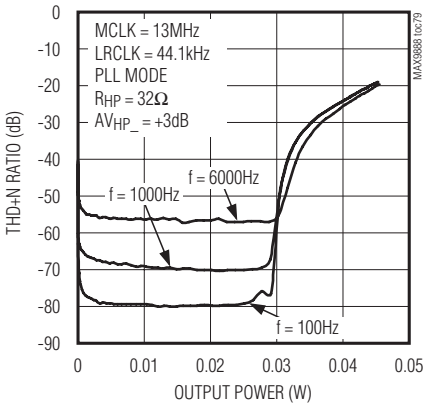
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

DAC to Headphone

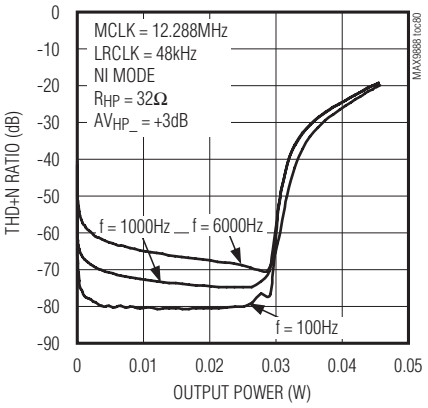
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



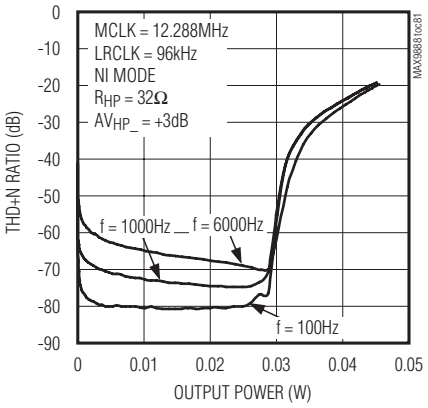
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



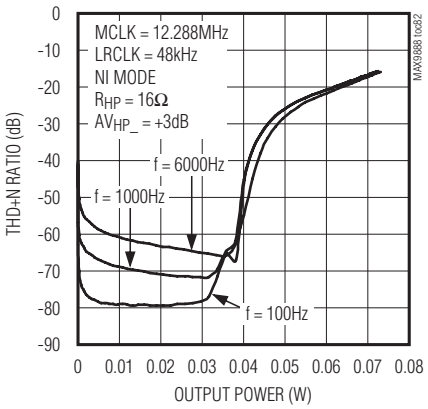
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



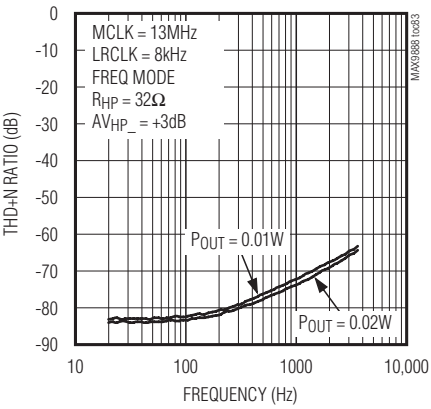
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO SPEAKER)

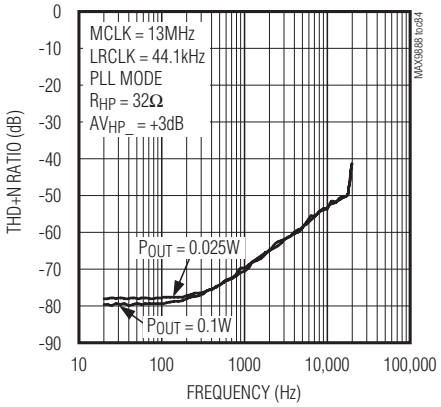


Stereo Audio CODEC with FlexSound Technology

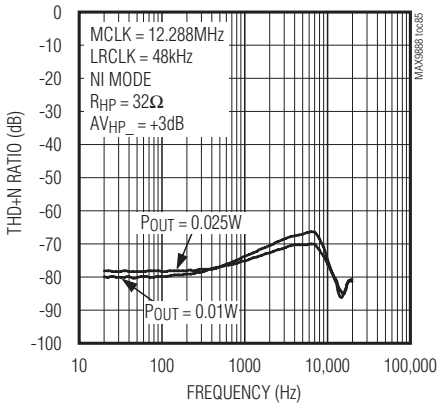
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

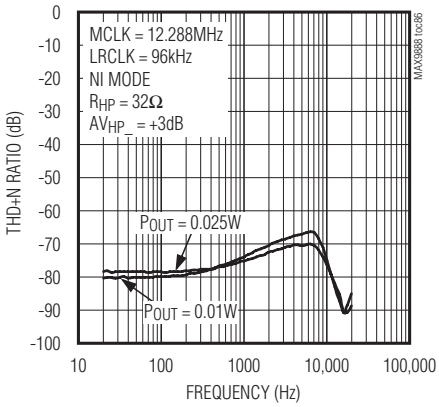
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



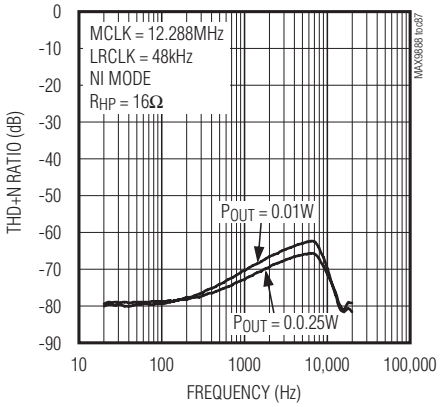
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



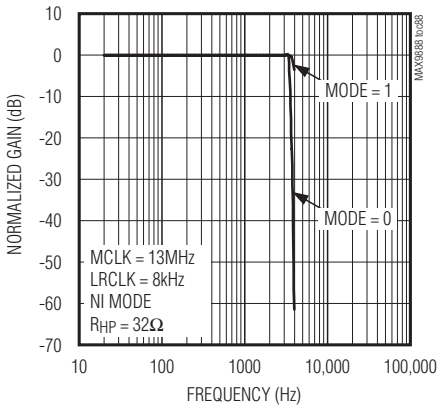
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



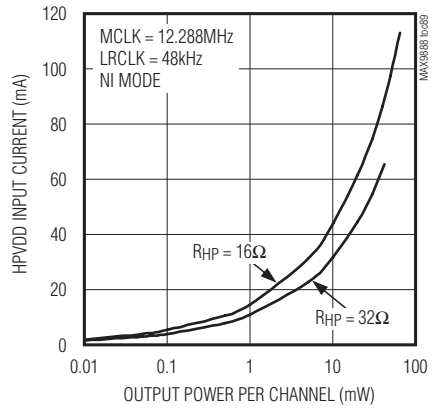
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



GAIN vs. FREQUENCY (DAC TO HEADPHONE)



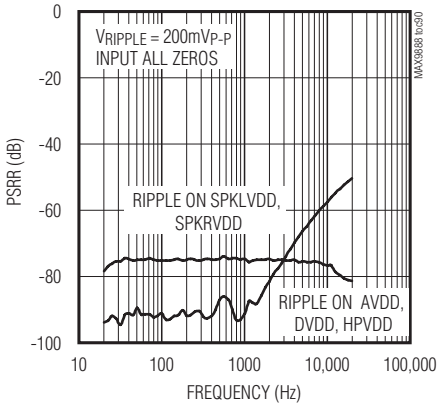
HPVDD INPUT CURRENT vs. OUTPUT POWER (DAC TO HEADPHONE)



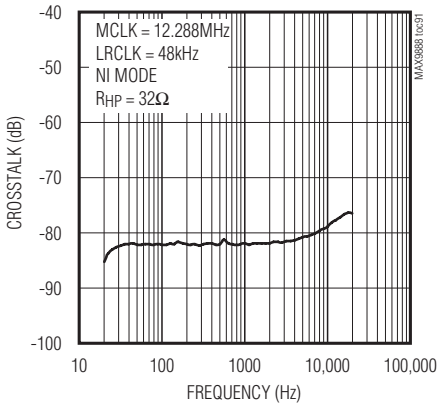
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

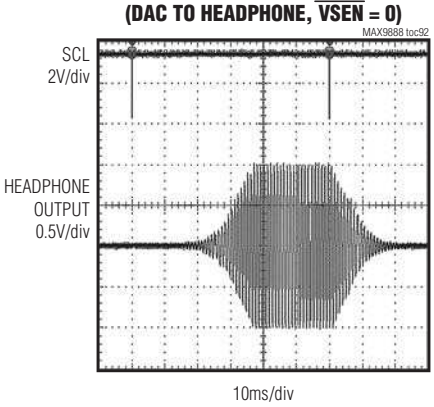
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



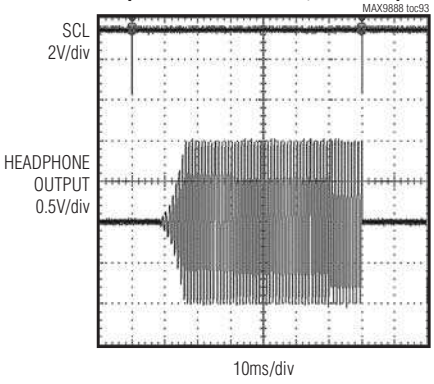
CROSSTALK vs. FREQUENCY (DAC TO HEADPHONE)



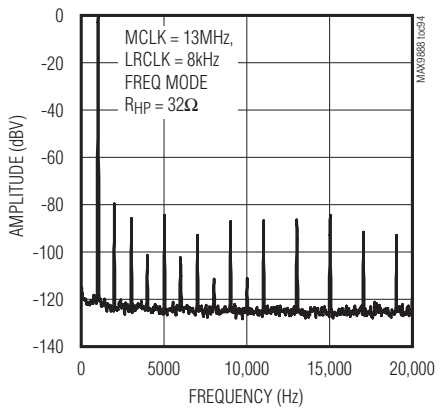
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO HEADPHONE, $\overline{VSEN}$ = 0)



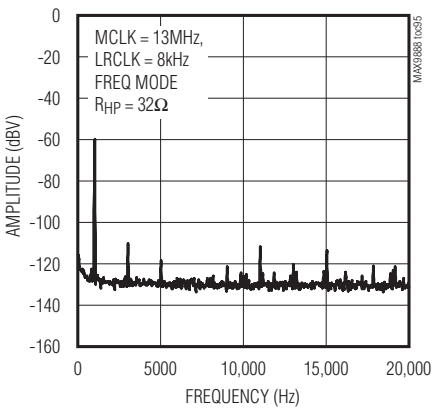
SOFTWARE TURN-ON/OFF RESPONSE (DAC TO HEADPHONE, $\overline{VSEN}$ = 1)



FFT, 0dBFS (DAC TO HEADPHONE)



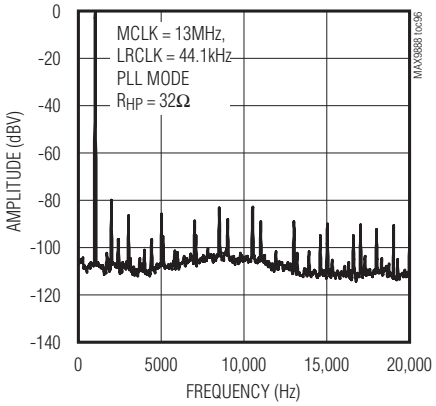
FFT, -60dBFS (DAC TO HEADPHONE)



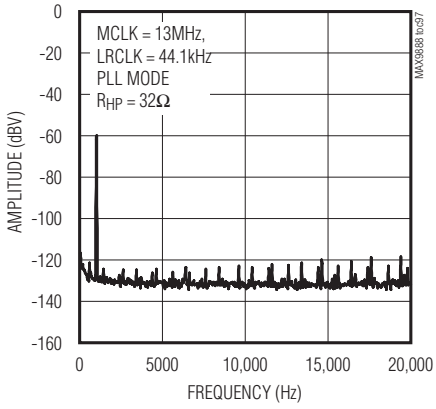
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

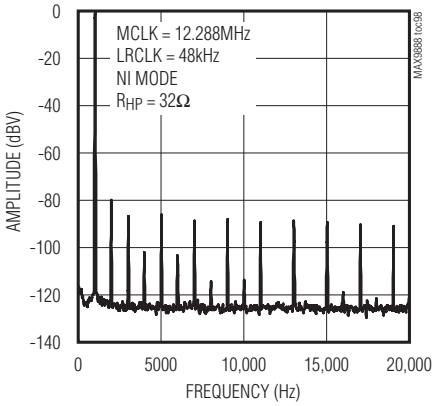
FFT, 0dBFS (DAC TO HEADPHONE)



FFT, -60dBFS (DAC TO HEADPHONE)



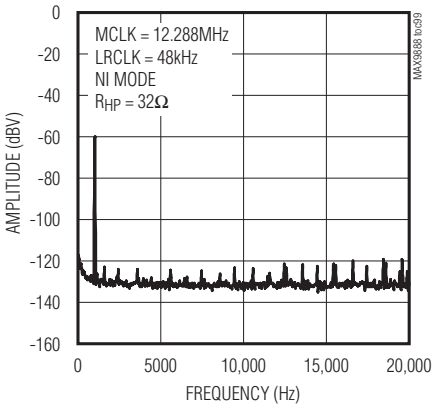
FFT, 0dBFS (DAC TO HEADPHONE)



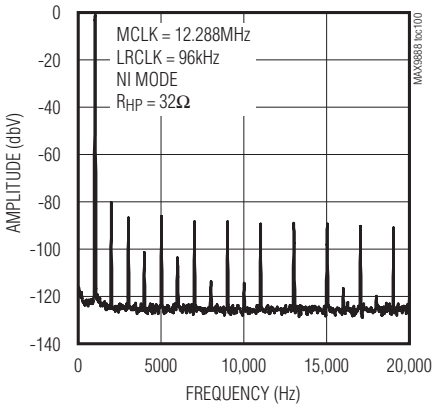
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

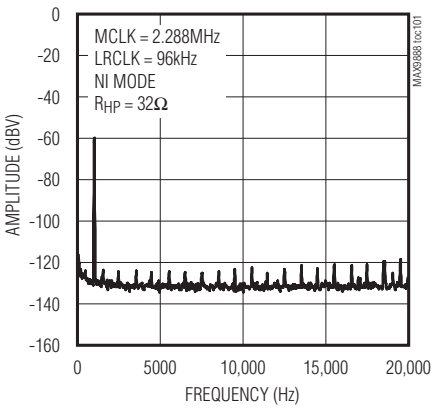
FFT, -60dBFS (DAC TO HEADPHONE)



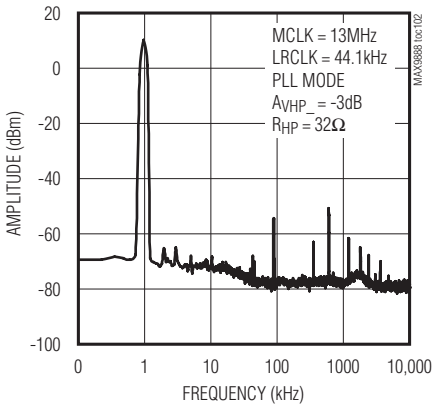
FFT, 0dBFS (DAC TO HEADPHONE)



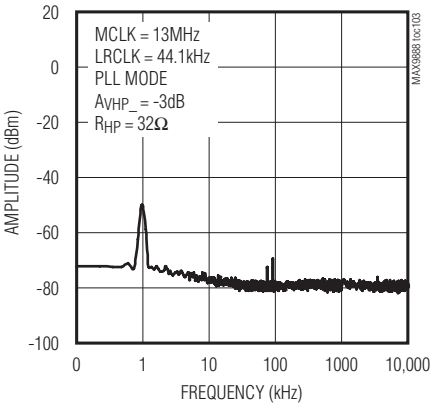
FFT, -60dBFS (DAC TO HEADPHONE)



WIDEBAND FFT, 0dBFS (DAC TO HEADPHONE)



WIDEBAND FFT, -60dBFS (DAC TO HEADPHONE)



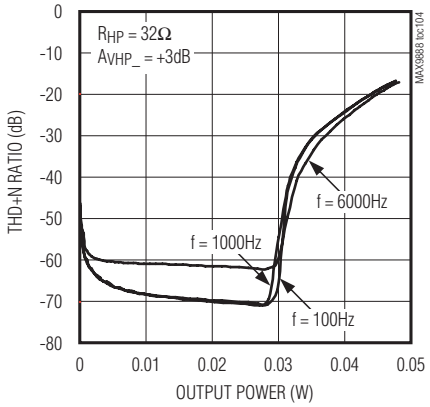
Stereo Audio CODEC with FlexSound Technology

Typical Operating Characteristics (continued)

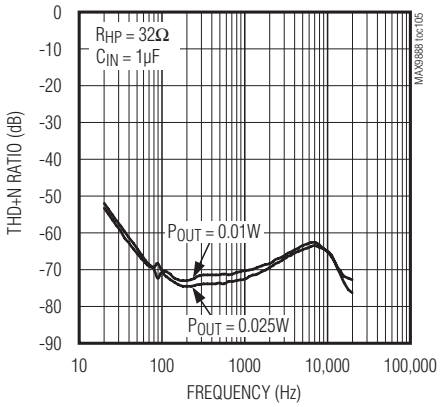
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Line to Headphone

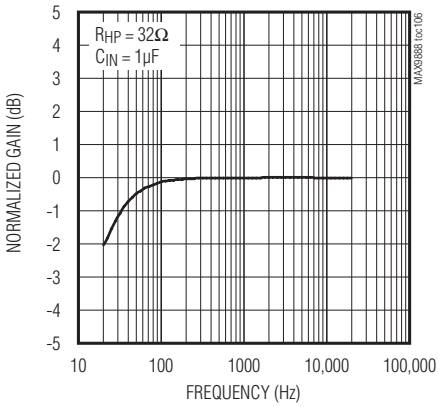
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO HEADPHONE)



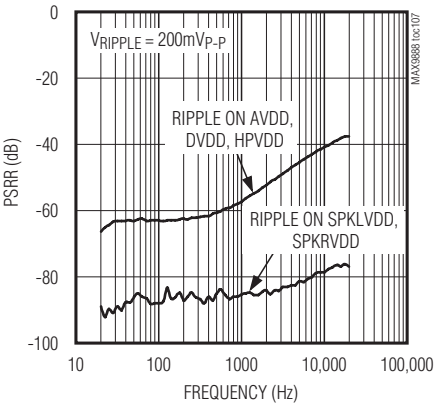
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO HEADPHONE)



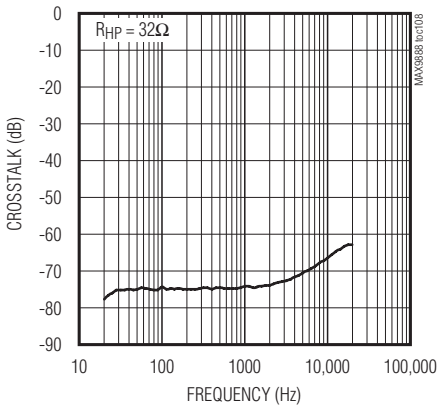
GAIN vs. FREQUENCY (LINE TO HEADPHONE)



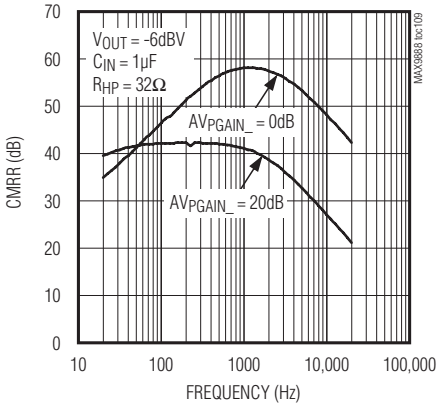
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)



CROSSTALK vs. FREQUENCY (LINE TO HEADPHONE)



COMMON-MODE REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)

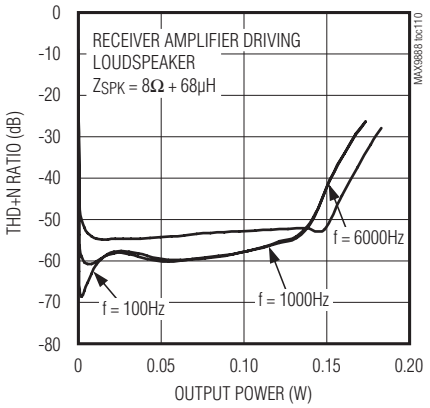


Typical Operating Characteristics (continued)

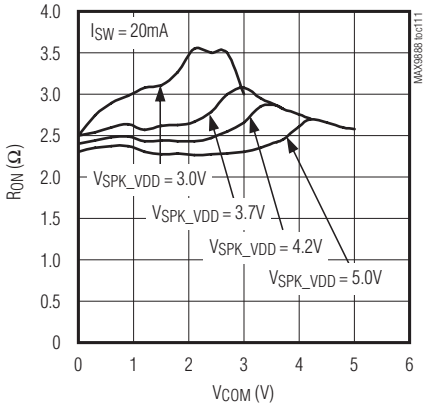
(V_{AVDD} = V_{HPVDD} = V_{DVDD} = V_{DVDDS1} = V_{DVDDS2} = +1.8V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = 3.7V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{REC}) connected between RECP and RECN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. R_{HP} = ∞, R_{REC} = ∞, Z_{SPK} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{HPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB, $AV_{MICPGA\_}$ = 0dB, $AV_{DACATTN}$ = 0dB, $AV_{DACGAIN}$ = 0dB, AV_{ADCLVL} = 0dB, $AV_{ADCGAIN}$ = 0dB, $AV_{PGAIN\_}$ = 0dB, $AV_{PGAOUT\_}$ = 0dB, $AV_{HP\_}$ = 0dB, AV_{REC} = 0dB, $AV_{SPK\_}$ = 0dB, MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 1. T_A = +25°C, unless otherwise noted.)

Speaker Bypass Switch

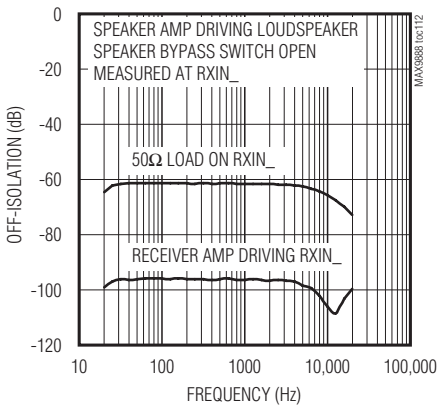
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER BYPASS SWITCH)



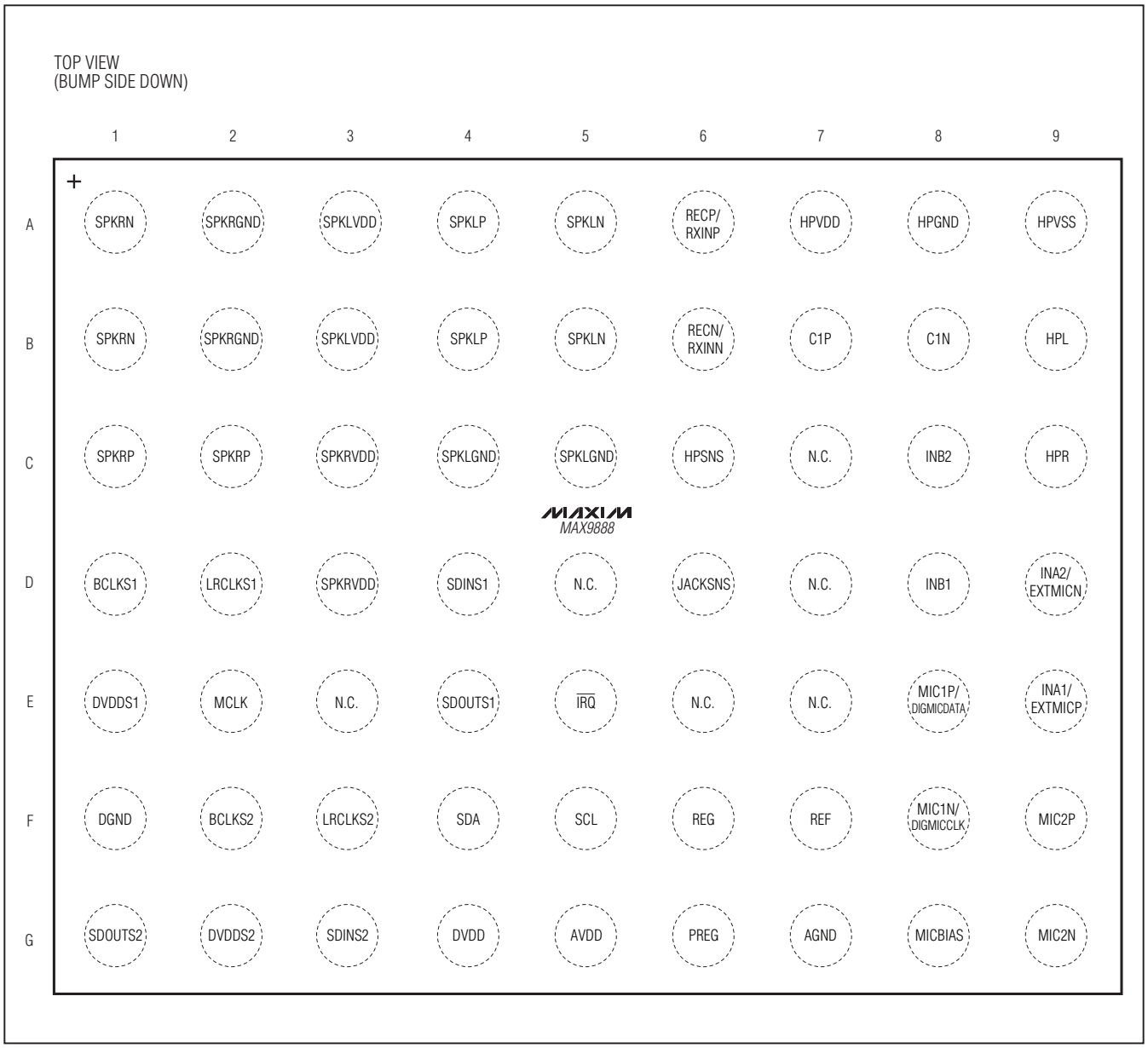
ON RESISTANCE vs. V_{COM} (SPEAKER BYPASS SWITCH)



OFF-ISOLATION vs. FREQUENCY (SPEAKER BYPASS SWITCH)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1, B1	SPKRN	Negative Right-Channel Class D Speaker Output
A2, B2	SPKRGND	Right-Speaker Ground
A3, B3	SPKLVDD	Left-Speaker, REF, Receiver Amplifier Power Supply. Bypass to SPKLGND with a 1µF and a 10µF capacitor.
A4, B4	SPKLP	Positive Left-Channel Class D Speaker Output
A5, B5	SPKLN	Negative Left-Channel Class D Speaker Output
A6	RECP/RXINP	Positive Receiver Amplifier Output. Can be positive bypass switch input when receiver amp is shut down.
A7	HPVDD	Headphone Power Supply. Bypass to HPGND with a 1µF capacitor.
A8	HPGND	Headphone Ground
A9	HPVSS	Inverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.
B6	RECN/RXINN	Negative Receiver Amplifier Output. Can be negative bypass switch input when receiver amp is shut down.
B7	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
B8	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
B9	HPL	Left-Channel Headphone Output
C1, C2	SPKRP	Positive Right-Channel Class D Speaker Output
C3, D3	SPKRVDD	Right-Speaker Power Supply. Bypass to SPKRGND with a 1µF capacitor.
C4, C5	SPKLGND	Left-Speaker Ground
C6	HPSNS	Headphone Amplifier Ground Sense. Connect to the headphone jack ground terminal or connect to ground.
C7, D5, D7, E3, E6, E7	N.C.	No Connection
C8	INB2	Single-Ended Line Input B2. Also positive differential line input B.
C9	HPR	Right-Channel Headphone Output
D1	BCLKS1	S1 Digital Audio Bit Clock Input/Output. BCLKS1 is an input when the MAX9888 is in slave mode and an output when in master mode. The input/output voltage is referenced to DVDDS1.
D2	LRCLKS1	S1 Digital Audio Left-Right Clock Input/Output. LRCLKS1 is the audio sample rate clock and determines whether S1 audio data is routed to the left or right channel. In TDM mode, LRCLKS1 is a frame sync pulse. LRCLKS1 is an input when the MAX9888 is in slave mode and an output when in master mode. The input/output voltage is referenced to DVDDS1.
D4	SDINS1	S1 Digital Audio Serial-Data DAC Input. The input voltage is referenced to DVDDS1.
D6	JACKSNS	Jack Sense. Detects the insertion of a jack. See the *Headset Detection* section.
D8	INB1	Single-Ended Line Input B1. Also negative differential line input B.
D9	INA2/ EXTMICN	Single-Ended Line Input A2. Also positive differential line input A or negative differential external microphone input.

Stereo Audio CODEC with FlexSound Technology

Pin Description (continued)

PIN	NAME	FUNCTION
E1	DVDDS1	S1 Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.
E2	MCLK	Master Clock Input. Acceptable input frequency range is 10MHz to 60MHz.
E4	SDOUTS1	S1 Digital Audio Serial-Data ADC Output. The output voltage is referenced to DVDDS1.
E5	$\overline{IRQ}$	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to pull low when bits in status register 0x00 change state. Read status register 0x00 to clear $\overline{IRQ}$ once set. Repeat faults have no effect on $\overline{IRQ}$ until it is cleared by reading the I²C status register 0x00. Connect a 10kΩ pullup resistor to DVDD for full output swing.
E8	MIC1P/ DIGMICDATA	Positive Differential Microphone 1 Input. AC-couple a microphone with a series 1µF capacitor. Can be retasked as a digital microphone data input.
E9	INA1/ EXTMICP	Single-Ended Line Input A1. Also negative differential line input A or positive differential external microphone input.
F1	DGND	Digital Ground
F2	BCLKS2	S2 Digital Audio Bit Clock Input/Output. BCLKS2 is an input when the IC is in slave mode and an output when in master mode. The input/output voltage is referenced to DVDDS2.
F3	LRCLKS2	S2 Digital Audio Left-Right Clock Input/Output. LRCLKS2 is the audio sample rate clock and determines whether audio data on S2 is routed to the left or right channel. In TDM mode, LRCLKS2 is a frame sync pulse. LRCLKS2 is an input when the IC is in slave mode and an output when in master mode. The input/output voltage is referenced to DVDDS2.
F4	SDA	I²C Serial-Data Input/Output. Connect a pullup resistor to DVDD for full output swing.
F5	SCL	I²C Serial-Clock Input
F6	REG	Common-Mode Voltage Reference. Bypass to AGND with a 1µF capacitor.
F7	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor.
F8	MIC1N/ DIGMICCLK	Negative Differential Microphone 1 Input. AC-couple a microphone with a series 1µF capacitor. Can be retasked as a digital microphone clock output.
F9	MIC2P	Positive Differential Microphone 2 Input. AC-couple a microphone with a series 1µF capacitor.
G1	SDOUTS2	S2 Digital Audio Serial-Data ADC Output. The output voltage is referenced to DVDDS2.
G2	DVDDS2	S2 Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.
G3	SDINS2	S2 Digital Audio Serial-Data DAC Input. The input voltage is referenced to DVDDS2.
G4	DVDD	Digital Power Supply. Supply for the digital core and I²C interface. Bypass to DGND with a 1µF capacitor.
G5	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
G6	PREG	Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor.
G7	AGND	Analog Ground
G8	MICBIAS	Low-Noise Bias Voltage. Outputs a 2.2V microphone bias. An external resistor in the 2.2kΩ to 1kΩ range should be used to set the microphone current.
G9	MIC2N	Negative Differential Microphone 2 Input. AC-couple a microphone with a series 1µF capacitor.

Detailed Description

The MAX9888 is a fully integrated stereo audio codec with FlexSound technology and integrated amplifiers.

Two differential microphone amplifiers can accept signals from three analog inputs. One input can be retasked to support two digital microphones. Any combination of two microphones (analog or digital) can be recorded simultaneously. The analog signals are amplified up to 50dB and recorded by the stereo ADC. The digital record path supports voice filtering with selectable preset highpass filters and high stopband attenuation at $f_S/2$. An automatic gain control (AGC) circuit monitors the digitized signal and automatically adjusts the analog microphone gain to make best use of the ADC's dynamic range. A noise gate attenuates signals below the user-defined threshold to minimize the noise output by the ADC.

The IC includes two analog line inputs. One of the line inputs can be optionally retasked as a third analog microphone input. Both line inputs support either stereo single-ended input signals or mono differential signals. The line inputs are preamplified and then routed either to the ADC for recording or to the output amplifiers for playback.

Integrated analog switches allow two differential microphone signals to be routed out the third microphone input to an external device. This eliminates the need for an external analog switch in systems that have two devices recording signals from the same microphone.

Through two digital audio interfaces, the device can transmit one stereo audio signal and receive two stereo audio signals in a wide range of formats including I^2S, PCM, and up to four mono slots in TDM. Each interface can be connected to either of two audio ports (S1 and S2) for communication with external devices. Both audio interfaces support 8kHz to 96kHz sample rates. Each input signal is independently equalized using 5-band parametric equalizers. A multiband automatic level control (ALC) boosts signals by up to 12dB. One signal path additionally supports the same voiceband filtering as the ADC path.

The IC includes a differential receiver amplifier, stereo Class D speaker amplifiers, and DirectDrive true ground stereo headphone amplifiers.

When the receiver amplifier is disabled, analog switches allow RECP/RXINP and RECN/RXINN to be reused for signal routing. In systems where a single transducer is used for both the loudspeaker and receiver, an external receiver amplifier can be routed to the left speaker through RECP/RXINP and RECN/RXINN, bypassing the Class D amplifier, to connect to the loudspeaker. If the internal receiver amplifier is used, then leave RECP/RXINP and RECN/RXINN unconnected. In systems where an external amplifier drives both the receiver and the MAX9888's input, one of the differential signals can be disconnected from the receiver when not needed by passing it through the analog switch that connects RECP/RXINP to RECN/RXINN.

The stereo Class D amplifier provides efficient amplification for two speakers. The amplifier includes active emissions limiting to minimize the radiated emissions (EMI) traditionally associated with Class D. In most systems, no output filtering is required to meet standard EMI limits.

To optimize speaker sound quality, the IC includes an excursion limiter, a distortion limiter, and a power limiter. The excursion limiter is a dynamic highpass filter with variable corner frequency that increases in response to high signal levels. Low-frequency energy typically causes more distortion than useful sound at high signal levels, so attenuating low frequencies allows the speaker to play louder without distortion or damage. At lower signal levels, the filter corner frequency reduces to pass more low frequency energy when the speaker can handle it. The distortion limiter reduces the volume when the output signal exceeds a preset distortion level. This ensures that regardless of input signal and battery voltage, excessive distortion is never heard by the user. The power limiter monitors the continuous power into the loudspeaker and lowers the signal level if the speaker is at risk of overheating.

The stereo DirectDrive headphone amplifier uses an inverting charge pump to generate a ground-referenced output signal. This eliminates the need for DC-blocking capacitors or a midrail bias for the headphone jack ground return. Ground sense reduces output noise caused by ground return current.

The IC integrates jack detection allowing the detection of insertion and removal of accessories as well as button presses.

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I²C Slave Address

Configure the MAX9888 using the I²C control bus. The IC uses a slave address of 0x20 or 00100000 for write operations and 0x21 or 00100001 for read operations. See the *I²C Serial Interface* section for a complete interface description.

Registers

Table 1 lists all of the registers, their addresses, and power-on-reset states. Registers 0x00 to 0x03 and 0xFF are read-only while all of the other registers are read/write. Write zeros to all unused bits in the register table when updating the register, unless otherwise noted.

Table 1. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
STATUS												
Status	CLD	SLD	ULK	—	—	—	JDET	—	0x00	—	R	103
Microphone AGC/NG	NG			AGC					0x01	—	R	65
Jack Status	JKSNS		—	—	—	—	—	—	0x02	—	R	101
Battery Voltage	—	—	—	VBAT					0x03	—	R/W	102
Interrupt Enable	ICLD	ISLD	IULK	0	0	0	IJDET	0	0x0F	0x00	R/W	103
MASTER CLOCK CONTROL												
Master Clock	0	0	PSCLK		0	0	0	0	0x10	0x00	R/W	76
DAI1 CLOCK CONTROL												
Clock Mode	SR1				FREQ1				0x11	0x00	R/W	76
Any Clock Control	PLL1	NI1[14:8]							0x12	0x00	R/W	77
	NI1[7:1]							NI1[0]	0x13	0x00	R/W	77
DAI1 CONFIGURATION												
Format	MAS1	WCI1	BCI1	DLY1	0	TDM1	FSW1	WS1	0x14	0x00	R/W	71
Clock	OSR1		0	0	0	BSEL1			0x15	0x00	R/W	72
I/O Configuration	SEL1		LTEN1	LBEN1	DMONO1	HIZOFF1	SDOEN1	SDIEN1	0x16	0x00	R/W	72
Time-Division Multiplex	SLOTL1		SLOTR1		SLOTDLY1				0x17	0x00	R/W	73
Filters	MODE1	AVFLT1			DHF1	DVFLT1			0x18	0x00	R/W	79
DAI2 CLOCK CONTROL												
Clock Mode	SR2				0	0	0	0	0x19	0x00	R/W	76
Any Clock Control	PLL2	NI2[14:8]							0x1A	0x00	R/W	77
	NI2[7:1]							NI2[0]	0x1B	0x00	R/W	77
DAI2 CONFIGURATION												
Format	MAS2	WCI2	BCI2	DLY2	0	TDM2	FSW2	WS2	0x1C	0x00	R/W	71
Clock	0	0	0	0	0	BSEL2			0x1D	0x00	R/W	72
I/O Configuration	SEL2		0	LBEN2	DMONO2	HIZOFF2	SDOEN2	SDIEN2	0x1E	0x00	R/W	72

Table 1. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
Time-Division Multiplex	SLOTL2		SLOTR2		SLOTDLY2				0x1F	0x00	R/W	73
Filters	0	0	0	0	DHF2	0	0	DCB2	0x20	0x00	R/W	79
MIXERS												
DAC Mixer	MIXDAL				MIXDAR				0x21	0x00	R/W	85
Left ADC Mixer	MIXADL								0x22	0x00	R/W	64
Right ADC Mixer	MIXADR								0x23	0x00	R/W	64
Preoutput 1 Mixer	0	0	0	0	MIXOUT1				0x24	0x00	R/W	86
Preoutput 2 Mixer	0	0	0	0	MIXOUT2				0x25	0x00	R/W	86
Preoutput 3 Mixer	0	0	0	0	MIXOUT3				0x26	0x00	R/W	86
Headphone Amplifier Mixer	MIXHPL				MIXHPR				0x27	0x00	R/W	97
Receiver Amplifier Mixer	0	0	0	0	MIXREC				0x28	0x00	R/W	88
Speaker Amplifier Mixer	MIXSPL				MIXSPR				0x29	0x00	R/W	90
LEVEL CONTROL												
Sidetone	DSTS		0		DVST				0x2A	0x00	R/W	69
DAI1 Playback Level	DV1M	0	DV1G		DV1				0x2B	0x00	R/W	84
DAI1 Playback Level	0	0	0	$\overline{\text{EQCLP1}}$	DVEQ1				0x2C	0x00	R/W	83
DAI2 Playback Level	DV2M	0	0	0	DV2				0x2D	0x00	R/W	84
DAI2 Playback Level	0	0	0	$\overline{\text{EQCLP2}}$	DVEQ2				0x2E	0x00	R/W	83
Left ADC Level	0	0	AVLG		AVL				0x2F	0x00	R/W	68
Right ADC Level	0	0	AVRG		AVR				0x30	0x00	R/W	68
Microphone 1 Input Level	0	PA1EN			PGAM1				0x31	0x00	R/W	61

Table 1. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
Microphone 2 Input Level	0	PA2EN		PGAM2					0x32	0x00	R/W	61
INA Input Level	0	INAEXT	0	0	0	PGAINA			0x33	0x00	R/W	63
INB Input Level	0	INBEXT	0	0	0	PGAINB			0x34	0x00	R/W	63
Preoutput 1 Level	0	0	0	0	PGAOUT1				0x35	0x00	R/W	87
Preoutput 2 Level	0	0	0	0	PGAOUT2				0x36	0x00	R/W	87
Preoutput 3 Level	0	0	0	0	PGAOUT3				0x37	0x00	R/W	87
Left Headphone Amplifier Volume Control	HPLM	0	0	HPVOLL					0x38	0x00	R/W	97
Right Headphone Amplifier Volume Control	HPRM	0	0	HPVOLR					0x39	0x00	R/W	97
Receiver Amplifier Volume Control	RECM	0	0	RECVOL					0x3A	0x00	R/W	88
Left Speaker Amplifier Volume Control	SPLM	0	0	SPVOLL					0x3B	0x00	R/W	90
Right Speaker Amplifier Volume Control	SPRM	0	0	SPVOLR					0x3C	0x00	R/W	90
MICROPHONE AGC												
Configuration	AGCSRC	AGCRLS			AGCATK		AGCHLD		0x3D	0x00	R/W	65
Threshold	ANTH				AGCTH				0x3E	0x00	R/W	66
SPEAKER SIGNAL PROCESSING												
Excursion Limiter Filter	0	DHPUCF			0	0	DHPLCF		0x3F	0x00	R/W	92
Excursion Limiter Threshold	0	0	0	0	0	DHPTH			0x40	0x00	R/W	92
ALC	ALCEN	ALCRLS			ALCMB	ALCTH			0x41	0x00	R/W	82

Table 1. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
Power Limiter	PWRTH				0	PWRK			0x42	0x00	R/W	93
Power Limiter	PWRT2				PWRT1				0x43	0x00	R/W	94
Distortion Limiter	THDCLP				0	THDT1			0x44	0x00	R/W	95
CONFIGURATION												
Audio Input	INADIFF	INBDIFF	0	0	0	0	0	0	0x45	0x00	R/W	63
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	EXTMIC		0x46	0x00	R/W	61
Level Control	$\overline{VS2EN}$	$\overline{VSEN}$	$\overline{ZDEN}$	0	0	0	EQ2EN	EQ1EN	0x47	0x00	R/W	99, 83
Bypass Switches	INABYP	0	0	MIC2BYP	0	0	RECBYP	SPKBYP	0x48	0x00	R/W	62, 98
Jack Detection	JDETEN	0	0	0	0	0	JDEB		0x49	0x00	R/W	101
POWER MANAGEMENT												
Input Enable	INAEN	INBEN	0	0	MBEN	0	ADLEN	ADREN	0x4A	0x00	R/W	59
Output Enable	HPLEN	HPREN	SPLEN	SPREN	RECEN	0	DALEN	DAREN	0x4B	0x00	R/W	59
System Enable	$\overline{SHDN}$	VBATEN	0	0	0	0	JDWK	0	0x4C	0x00	R/W	59
DSP COEFFICIENTS												
EQ Band 1 (DAI1/DAI2)	K_1[15:8]								0x50/0x82	0xXX	R/W	82
	K_1[7:0]								0x51/0x83	0xXX	R/W	82
	K1_1[15:8]								0x52/0x84	0xXX	R/W	82
	K1_1[7:0]								0x53/0x85	0xXX	R/W	82
	K2_1[15:8]								0x54/0x86	0xXX	R/W	82
	K2_1[7:0]								0x55/0x87	0xXX	R/W	82
	c1_1[15:8]								0x56/0x88	0xXX	R/W	82
	c1_1[7:0]								0x57/0x89	0xXX	R/W	82
	c2_1[15:8]								0x58/0x8A	0xXX	R/W	82
	c2_1[7:0]								0x59/0x8B	0xXX	R/W	82
EQ Band 2 (DAI1/DAI2)	K_2[15:8]								0x5A/0x8C	0xXX	R/W	82
	K_2[7:0]								0x5B/0x8D	0xXX	R/W	82
	K1_2[15:8]								0x5C/0x8E	0xXX	R/W	82
	K1_2[7:0]								0x5D/0x8F	0xXX	R/W	82
	K2_2[15:8]								0x5E/0x90	0xXX	R/W	82
	K2_2[7:0]								0x5F/0x91	0xXX	R/W	82
	c1_2[15:8]								0x60/0x92	0xXX	R/W	82
	c1_2[7:0]								0x61/0x93	0xXX	R/W	82
	c2_2[15:8]								0x62/0x94	0xXX	R/W	82
	c2_2[7:0]								0x63/0x95	0xXX	R/W	82

Table 1. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W	PAGE
EQ Band 3 (DAI1/DAI2)	K_3[15:8]								0x64/0x96	0xXX	R/W	82
	K_3[7:0]								0x65/0x97	0xXX	R/W	82
	K1_3[15:8]								0x66/0x98	0xXX	R/W	82
	K1_3[7:0]								0x67/0x99	0xXX	R/W	82
	K2_3[15:8]								0x68/0x9A	0xXX	R/W	82
	K2_3[7:0]								0x69/0x9B	0xXX	R/W	82
	c1_3[15:8]								0x6A/0x9C	0xXX	R/W	82
	c1_3[7:0]								0x6B/0x9D	0xXX	R/W	82
	c2_3[15:8]								0x6C/0x9E	0xXX	R/W	82
	c2_3[7:0]								0x6D/0x9F	0xXX	R/W	82
EQ Band 4 (DAI1/DAI2)	K_4[15:8]								0x6E/0xA0	0xXX	R/W	82
	K_4[7:0]								0x6F/0xA1	0xXX	R/W	82
	K1_4[15:8]								0x70/0xA2	0xXX	R/W	82
	K1_4[7:0]								0x71/0xA3	0xXX	R/W	82
	K2_4[15:8]								0x72/0xA4	0xXX	R/W	82
	K2_4[7:0]								0x73/0xA5	0xXX	R/W	82
	c1_4[15:8]								0x74/0xA6	0xXX	R/W	82
	c1_4[7:0]								0x75/0xA7	0xXX	R/W	82
	c2_4[15:8]								0x76/0xA8	0xXX	R/W	82
	c2_4[7:0]								0x77/0xA9	0xXX	R/W	82
EQ Band 5 (DAI1/DAI2)	K_5[15:8]								0x78/0xAA	0xXX	R/W	82
	K_5[7:0]								0x79/0xAB	0xXX	R/W	82
	K1_5[15:8]								0x7A/0xAC	0xXX	R/W	82
	K1_5[7:0]								0x7B/0xAD	0xXX	R/W	82
	K2_5[15:8]								0x7C/0xAE	0xXX	R/W	82
	K2_5[7:0]								0x7D/0xAF	0xXX	R/W	82
	c1_5[15:8]								0x7E/0xB0	0xXX	R/W	82
	c1_5[7:0]								0x7F/0xB1	0xXX	R/W	82
	c2_5[15:8]								0x80/0xB2	0xXX	R/W	82
	c2_5[7:0]								0x81/0xB3	0xXX	R/W	82
Excursion Limiter Biquad (DAI1/DAI2)	a1[15:8]								0xB4/0xBE	0xXX	R/W	91
	a1[7:0]								0xB5/0xBF	0xXX	R/W	91
	a2[15:8]								0xB6/0xC0	0xXX	R/W	91
	a2[7:0]								0xB7/0xC1	0xXX	R/W	91
	b0[15:8]								0xB8/0xC2	0xXX	R/W	91
	b0[7:0]								0xB9/0xC3	0xXX	R/W	91
	b1[15:8]								0xBA/0xC4	0xXX	R/W	91
	b1[7:0]								0xBB/0xC5	0xXX	R/W	91
	b2[15:8]								0xBC/0xC6	0xXX	R/W	91
	b2[7:0]								0xBD/0xC7	0xXX	R/W	91
REVISION ID												
Rev ID	REV								0xFF	0x43	R	104

Power Management

The IC includes comprehensive power management to allow the disabling of all unused circuits, minimizing supply current.

Table 2. Power Management Registers

REGISTER	BIT	NAME	DESCRIPTION
0x4C	7	$\overline{SHDN}$	**Global Shutdown** Disables everything except the headset detection circuitry, which is controlled separately. 0 = Device shutdown 1 = Device enabled
	6	VBATEN	See the *Battery Measurement* section.
	1	JDWK	See the *Headset Detection* section.
0x4A	7	INAEN	**Line Input A Enable** 0 = Disabled 1 = Enabled
	6	INBEN	**Line Input B Enable** 0 = Disabled 1 = Enabled
	3	MBEN	**Microphone Bias Enable** 0 = Disabled 1 = Enabled
	1	ADLEN	**Left ADC Enable** 0 = Disabled 1 = Enabled
	0	ADREN	**Right ADC Enable** 0 = Disabled 1 = Enabled
0x4B	7	HPLEN	**Left Headphone Enable** 0 = Disabled 1 = Enabled
	6	HPREN	**Right Headphone Enable** 0 = Disabled 1 = Enabled
	5	SPLEN	**Left Speaker Enable** 0 = Disabled 1 = Enabled
	4	SPREN	**Right Speaker Enable** 0 = Disabled 1 = Enabled
	3	RECEN	**Receiver Enable** 0 = Disabled 1 = Enabled
	1	DALEN	**Left DAC Enable** 0 = Disabled 1 = Enabled
	0	DAREN	**Right DAC Enable** 0 = Disabled 1 = Enabled

Stereo Audio CODEC with FlexSound Technology

Microphone Inputs

The device includes three differential microphone inputs and a low-noise microphone bias for powering the microphones (Figure 6). One microphone input can also be configured as a digital microphone input accepting signals from up to two digital microphones. Two microphones, analog or digital, can be recorded simultaneously.

In the typical application, one microphone input is used for the handset microphone and the other is used as an accessory microphone. In systems using a background noise microphone, INA can be retasked as another microphone input.

In systems where the codec is not the only device recording microphone signals, connect microphones to MIC2P/MIC2N and EXTMICP/EXTMICN. MIC1P/MIC1N then become outputs that route the microphone signals to an external device as needed. Two devices can then record microphone signals without needing external analog switches.

Analog microphone signals are amplified by two stages of gain and then routed to the ADCs. The first stage offers selectable 0dB, 20dB, or 30dB settings. The second stage is a programmable-gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps. To maximize the signal-to-noise ratio, use the gain in the first stage whenever possible. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes.

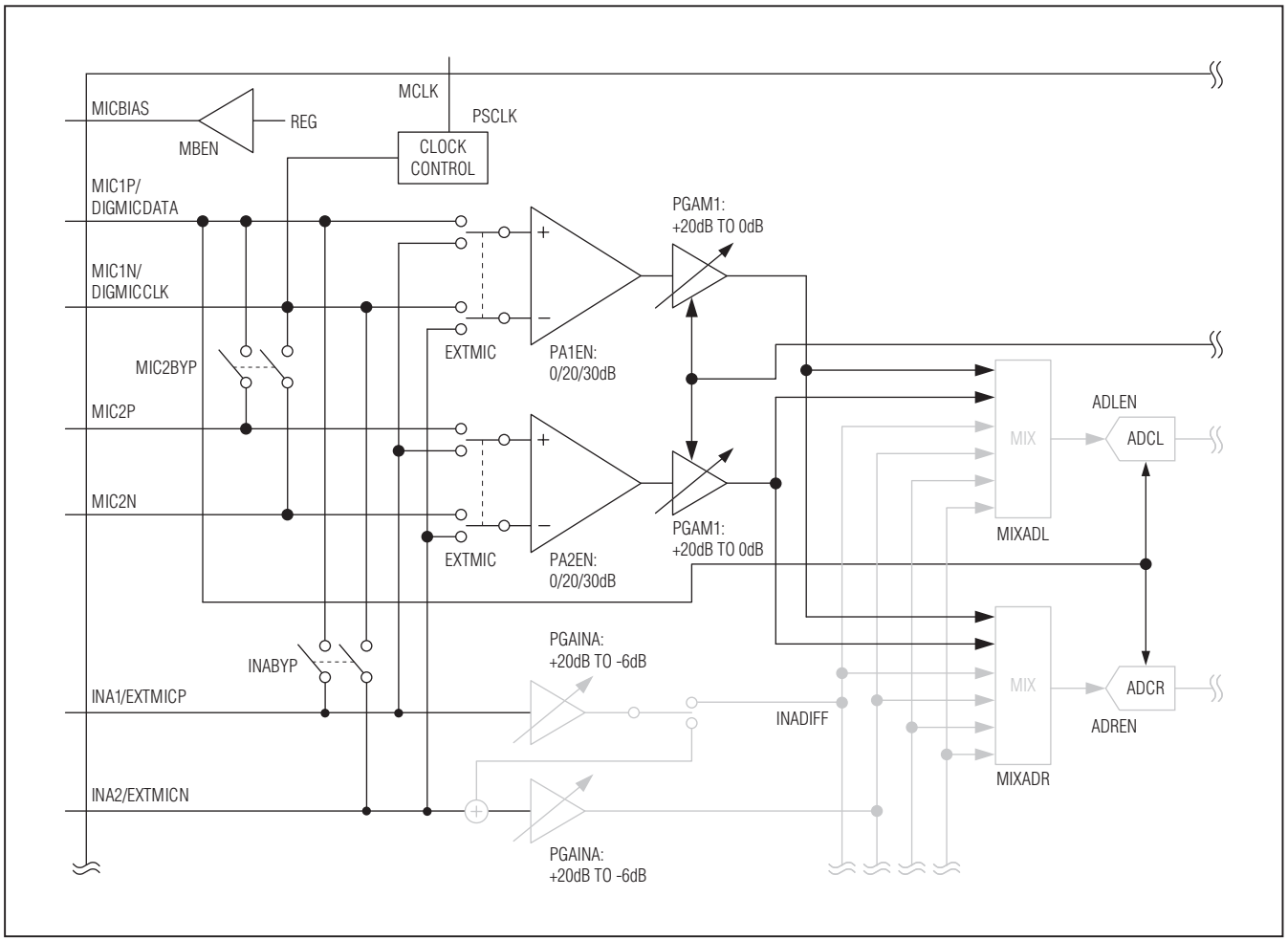


Figure 6. Microphone Input Block Diagram

Table 3. Microphone Input Registers

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="15">0x31/0x32</td><td>6</td><td rowspan="2">PA1EN/PA2EN</td><td colspan="4">MIC1/MIC2 Preamplifier Gain
Course microphone gain adjustment.
00 = Preamplifier disabled
01 = 0dB
10 = 20dB
11 = 30dB</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td rowspan="13">PGAM1/PGAM2</td><td colspan="4">MIC1/MIC2 PGA
Fine microphone gain adjustment.</td></tr>
<tr><td rowspan="3">3</td><td>VALUE</td><td>GAIN (dB)</td><td>VALUE</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+20</td><td>0x0B</td><td>+9</td></tr>
<tr><td>0x01</td><td>+19</td><td>0x0C</td><td>+8</td></tr>
<tr><td rowspan="3">2</td><td>0x02</td><td>+18</td><td>0x0D</td><td>+7</td></tr>
<tr><td>0x03</td><td>+17</td><td>0x0E</td><td>+6</td></tr>
<tr><td>0x04</td><td>+16</td><td>0x0F</td><td>+5</td></tr>
<tr><td rowspan="3">1</td><td>0x05</td><td>+15</td><td>0x10</td><td>+4</td></tr>
<tr><td>0x06</td><td>+14</td><td>0x11</td><td>+3</td></tr>
<tr><td>0x07</td><td>+13</td><td>0x12</td><td>+2</td></tr>
<tr><td rowspan="3">0</td><td>0x08</td><td>+12</td><td>0x13</td><td>+1</td></tr>
<tr><td>0x09</td><td>+11</td><td>0x14 to 0x1F</td><td>0</td></tr>
<tr><td>0x0A</td><td>+10</td><td colspan="2"></td></tr>
<tr><td rowspan="6">0x46</td><td>7</td><td rowspan="2">MICCLK</td><td colspan="4">Digital Microphone Clock Frequency
Select a frequency that is within the digital microphone’s clock frequency range.
Set OSR1 = 1 when using a digital microphone.
00 = PCLK/8
01 = PCLK/6
10 = 64 x LRCLK
11 = Reserved</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td><td>DIGMICL</td><td colspan="4">Left Digital Microphone Enable
Set PAL1EN = 00 for proper operation.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>4</td><td>DIGMICR</td><td colspan="4">Right Digital Microphone Enable
Set PAR1EN = 00 for proper operation.
0 = Disabled
1 = Enabled</td></tr>
<tr><td>1</td><td rowspan="2">EXTMIC</td><td colspan="4">External Microphone Connection
Routes INA_/EXTMIC_ to the microphone preamplifiers. Set INAEN = 0 when using INA_/EXTMIC_ as a microphone input.
00 = Disabled
01 = MIC1 input
10 = MIC2 input
11 = Reserved</td></tr>
<tr><td>0</td></tr>
</table>

Table 3. Microphone Input Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
0x48	7	INABYP	**INA_/EXTMIC_ to MIC1_ Bypass Switch** 0 = Disabled 1 = Enabled
	4	MIC2BYP	**MIC1_ to MIC2_ Bypass Switch** 0 = Disabled 1 = Enabled
	1	RECBYP	See the *Output Bypass Switches* section.
	0	SPKBYP	

Line Inputs

The device includes two sets of line inputs (Figure 7). Each set can be configured as a stereo single-ended input or as a mono differential input. Each input includes adjustable gain to match a wide range of input signal levels. If a custom gain is needed, the external gain mode provides a trimmed feedback resistor. Set the gain by choosing the appropriate input resistor and using the following formula:

$$AV_{PGAIN} = 20 \times \log (20K/RIN)$$

The external gain mode also allows summing multiple signals into a single input, by connecting multiple input resistors as show in Figure 8, and inputting signals larger than $1V_{P-P}$.

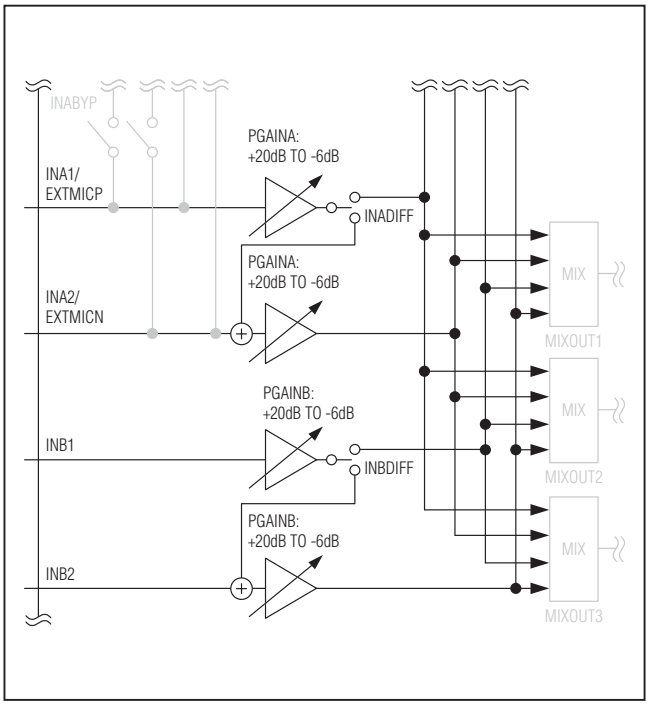


Figure 7. Line Input Block Diagram

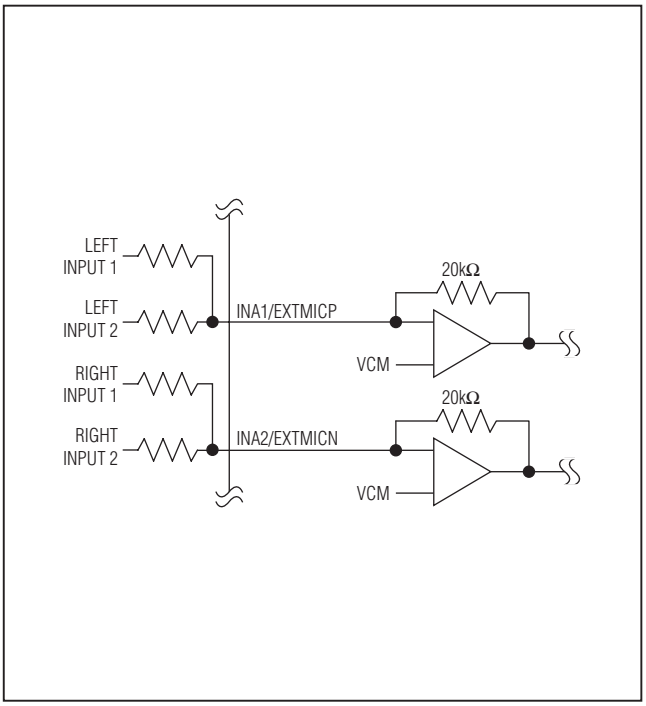


Figure 8. Summing Multiple Input Signals into INA/INB

Table 4. Line Input Registers

REGISTER	BIT	NAME	DESCRIPTION
0x33/0x34	6	INAEXT/INBEXT	**Line Input A/B External Gain** Switches out the internal input resistor and selects a trimmed 20kΩ feedback resistor. Use an external input resistor to set the gain of the line input. 0 = Disabled 1 = Enabled
	2 1 0	PGAINA/PGAINB	**Line Input A/B Internal Gain Settings** 000 = +20dB 001 = +14dB 010 = +3dB 011 = 0dB 100 = -3dB 101 = -6dB 110 = -6dB 111 = -6dB
0x45	7	INADIFF	**Line Input A Differential Enable** 0 = Stereo single-ended input 1 = Mono differential input
	6	INBDIFF	**Line Input B Differential Enable** 0 = Stereo single-ended input 1 = Mono differential input

ADC Input Mixers

The device's stereo ADC accepts input from the microphone amplifiers and line inputs. The ADC mixer routes any combination of the six audio inputs to the left and right ADCs (Figure 9).

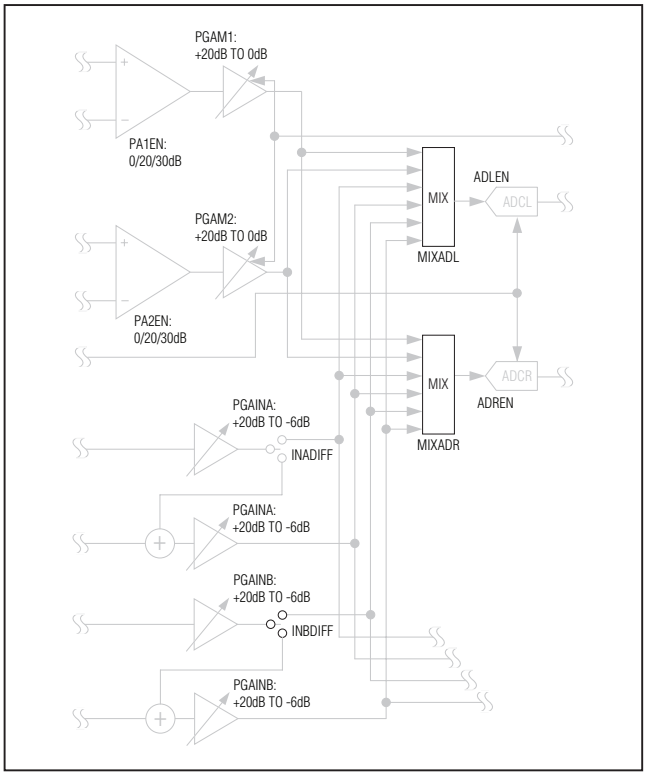


Figure 9. ADC Input Mixer Block Diagram

Table 5. ADC Input Mixer Register

REGISTER	BIT	NAME	DESCRIPTION
0x22/0x23	7	MIXADL/MIXADR	**Left/Right ADC Input Mixer** Selects which analog inputs are recorded by the left/right ADC. 1xxxxxxx = MIC1 x1xxxxxx = MIC2 xx1xxxxx = Reserved xxx1xxxx = Reserved xxxx1xxx = INA1 xxxxx1xx = INA2 (INADIFF = 0) or INA2 - INA1 (INADIFF = 1) xxxxxx1x = INB1 xxxxxxx1 = INB2 (INBDIFF = 0) or INB2 - INB1 (INBDIFF = 1)
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Record Path Signal Processing

The device's record signal path includes both automatic gain control (AGC) for the microphone inputs and a digital noise gate at the output of the ADC (Figure 10).

Microphone AGC

The IC's AGC monitors the signal level at the output of the ADC and then adjusts the MIC1 and MIC2 analog PGA settings automatically. When the signal level is below the predefined threshold, the gain is increased up to its maximum (20dB). If the signal exceeds the threshold, the gain is reduced to prevent the output signal level exceeding the threshold. When AGC is enabled, the microphone PGA is not user programmable. The AGC provides a more constant signal level and improves the available ADC dynamic range.

Noise Gate

Since the AGC increases the levels of all signals below a user-defined threshold, the noise floor is effectively increased by 20dB. To counteract this, the noise gate reduces the gain at low signal levels. Unlike typical noise gates that completely silence the output below a defined level, the noise gate in the IC applies downward expansion. The noise gate attenuates the output at a rate of 1dB for each 2dB the signal is below the threshold.

The noise gate can be used in conjunction with the AGC or on its own. When the AGC is enabled, the noise gate reduces the output level only when the AGC has set the gain to the maximum setting. Figure 11 shows the gain response resulting from using the AGC and noise gate.

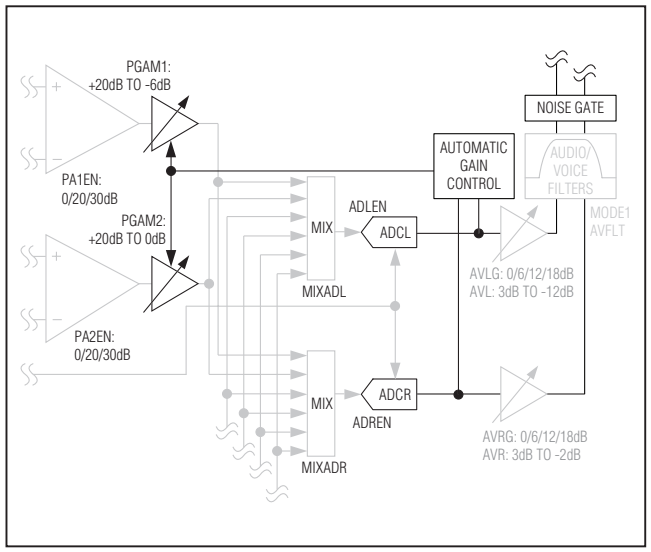


Figure 10. Record Path Signal Processing Block Diagram

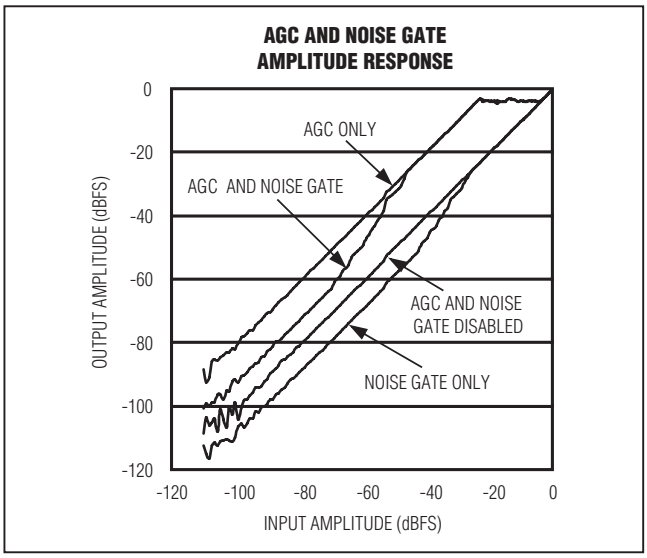


Figure 11. AGC and Noise Gate Input vs. Output Gain

Table 6. Record Path Signal Processing Registers

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="15">0x01</td><td>7</td><td rowspan="3">NG</td><td colspan="4">Noise Gate Attenuation
Reports the current noise gate attenuation.
000 = 0dB
001 = 1dB
010 = 2dB
011 = 3dB to 5dB
100 = 6dB to 7dB
101 = 8dB to 9dB
110 = 10dB to 11dB
111 = 12dB</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td rowspan="12">AGC</td><td colspan="4">AGC Gain
Reports the current AGC gain setting.</td></tr>
<tr><td rowspan="11">3
2
1
0</td><td>VALUE</td><td>GAIN (dB)</td><td>VALUE</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+20</td><td>0x0B</td><td>+9</td></tr>
<tr><td>0x01</td><td>+19</td><td>0x0C</td><td>+8</td></tr>
<tr><td>0x02</td><td>+18</td><td>0x0D</td><td>+7</td></tr>
<tr><td>0x03</td><td>+17</td><td>0x0E</td><td>+6</td></tr>
<tr><td>0x04</td><td>+16</td><td>0x0F</td><td>+5</td></tr>
<tr><td>0x05</td><td>+15</td><td>0x10</td><td>+4</td></tr>
<tr><td>0x06</td><td>+14</td><td>0x11</td><td>+3</td></tr>
<tr><td>0x07</td><td>+13</td><td>0x12</td><td>+2</td></tr>
<tr><td>0x08</td><td>+12</td><td>0x13</td><td>+1</td></tr>
<tr><td>0x09</td><td>+11</td><td>0x14 to 0x1F</td><td>0</td></tr>
<tr><td>0x0A</td><td>+10</td><td colspan="2"></td></tr>
<tr><td rowspan="4">0x3D</td><td>7</td><td>AGCSRC</td><td colspan="4">AGC/Noise Gate Signal Source
Determines which ADC channel the AGC and noise gates analyze. Gain is adjusted on both channels regardless of the AGCSRC setting.
0 = Left ADC output
1 = Maximum of either the left or right ADC output</td></tr>
<tr><td>6</td><td rowspan="3">AGCRLS</td><td colspan="4">AGC Release Time
Defined as the duration from start to finish of gain increase in the region shown in Figure 12. Release times are longer for low AGC threshold levels.
000 = 78ms
001 = 156ms
010 = 312ms
011 = 625ms
100 = 1.25s
101 = 2.5s
110 = 5s
111 = 10s</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
</table>

Table 6. Record Path Signal Processing Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
0x3D	3	AGCATK	**AGC Attack Time** Defined as the time required to reduce gain by 63% of the total gain reduction (one time constant of the exponential response). Attack times are longer for low AGC threshold levels. See Figure 12 for details. 00 = 2ms 01 = 7.2ms 10 = 31ms 11 = 123ms
	2		
	1	AGCHLD	**AGC Hold Time** The delay before the AGC release begins. The hold time counter starts whenever the signal drops below the AGC threshold and is reset by any signal that exceeds the threshold. Set AGCHLD to enable the AGC circuit. See Figure 12 for details. 00 = AGC disabled 01 = 50ms 10 = 100ms 11 = 400ms
	0		
0x3E	7	ANTH	**Noise Gate Threshold** Gain is reduced for signals below the threshold to quiet noise. The thresholds are relative to the ADC's full-scale output voltage.

VALUE	THRESHOLD (dBFS)	VALUE	THRESHOLD (dBFS)
0x0	Noise gate disabled	0x8	-45
0x1	Reserved	0x9	-41
0x2	Reserved	0xA	-38
0x3	-64	0xB	-34
0x4	-62	0xC	-30
0x5	-58	0xD	-27
0x6	-53	0xE	-22
0x7	-50	0xF	-16

0x3E	3	AGCTH	**AGC Threshold** Gain is reduced when signals exceed the threshold to prevent clipping. The thresholds are relative to the ADC's full-scale voltage.

VALUE	THRESHOLD (dBFS)	VALUE	THRESHOLD (dBFS)
0x0	-3	0x8	-11
0x1	-4	0x9	-12
0x2	-5	0xA	-13
0x3	-6	0xB	-14
0x4	-7	0xC	-15
0x5	-8	0xD	-16
0x6	-9	0xE	-17
0x7	-10	0xF	-18

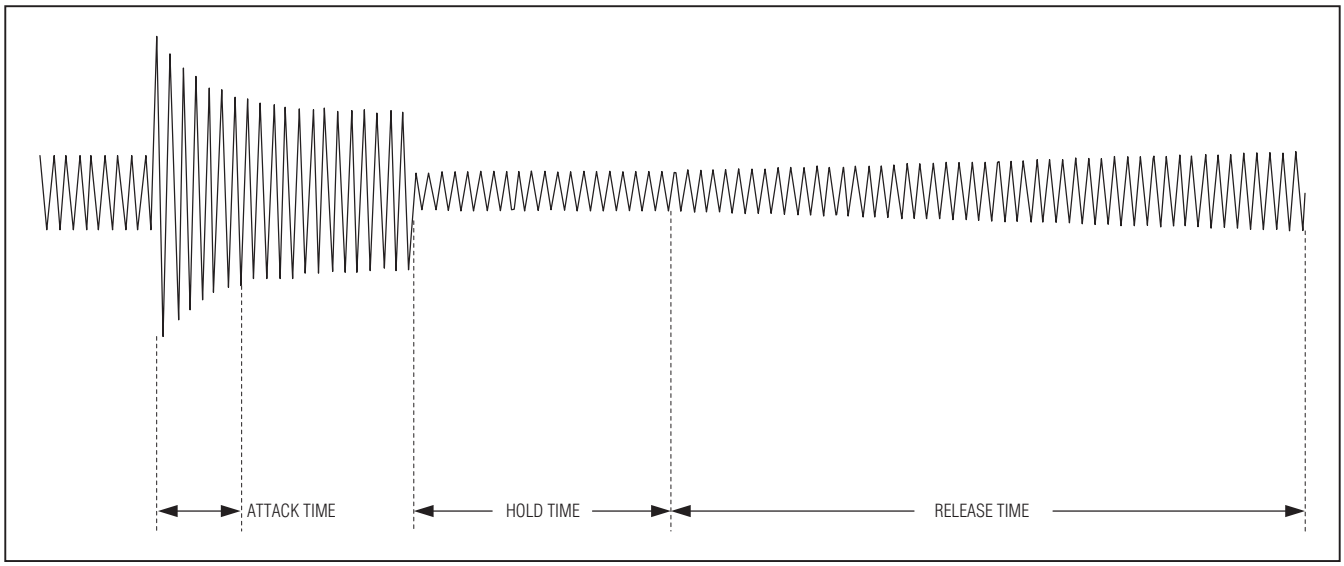


Figure 12. AGC Timing

ADC Record Level Control

The IC includes separate digital level control for the left and right ADC outputs (Figure 13). To optimize dynamic range, use analog gain to adjust the signal level and set the digital level control to 0dB whenever possible. Digital level control is primarily used when adjusting the record level for digital microphones.

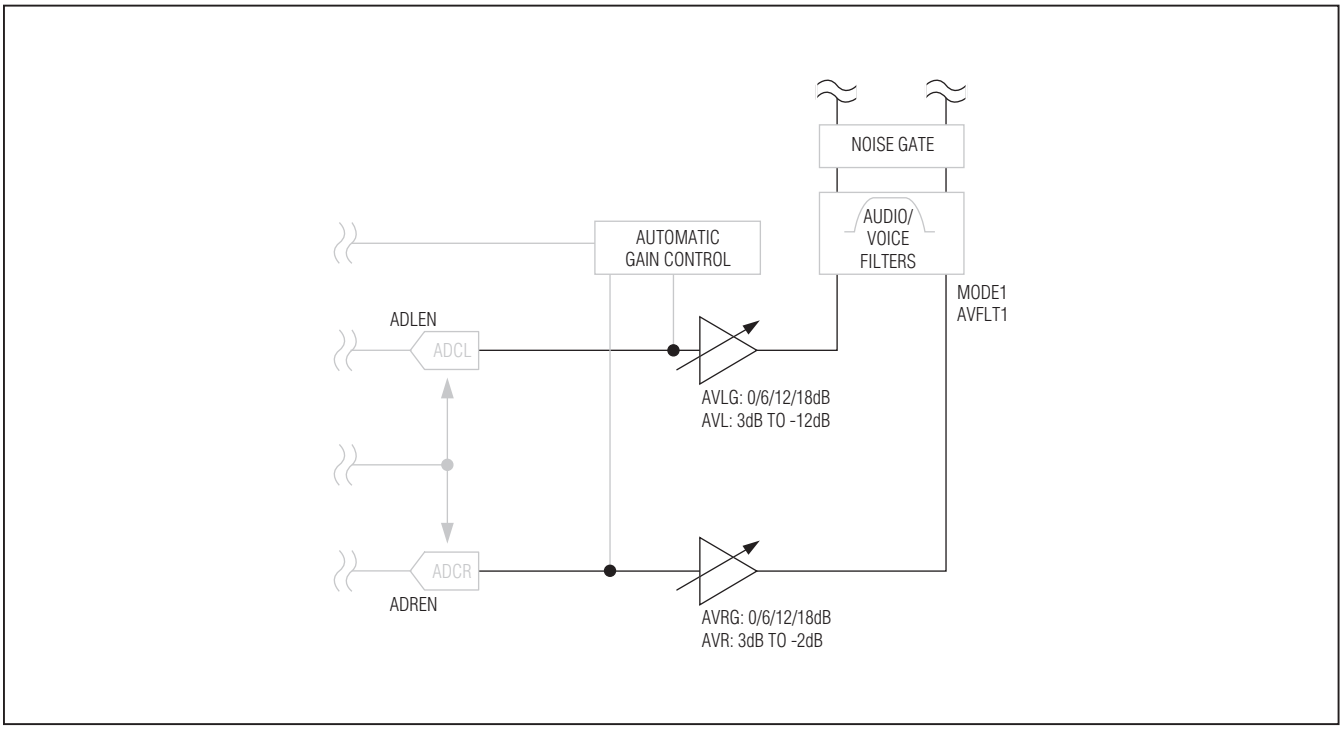


Figure 13. ADC Record Level Control Block Diagram

Table 7. ADC Record Level Control Register

REGISTER	BIT	NAME	DESCRIPTION			
0x2F/0x30	5	AVLG/AVRG	**Left/Right ADC Gain** 00 = 0dB 01 = 6dB 10 = 12dB 11 = 18dB			
	4					
	3	AVL/AVR	**Left/Right ADC Level**			
			VALUE	**GAIN (dB)**	**VALUE**	**GAIN (dB)**
	2		0x0	+3	0x8	-5
			0x1	+2	0x9	-6
	1		0x2	+1	0xA	-7
			0x3	0	0xB	-8
			0x4	-1	0xC	-9
	0		0x5	-2	0xD	-10
			0x6	-3	0xE	-11
			0x7	-4	0xF	-12

Sidetone

Enable sidetone during full-duplex operation to add a low-level copy of the recorded audio signal to the playback audio signal (Figure 14). Sidetone is commonly used in telephony to allow the speaker to hear himself speak, providing a more natural user experience. The IC implements sidetone digitally. Doing so helps prevent unwanted feedback into the playback signal path and better matches the playback audio signal.

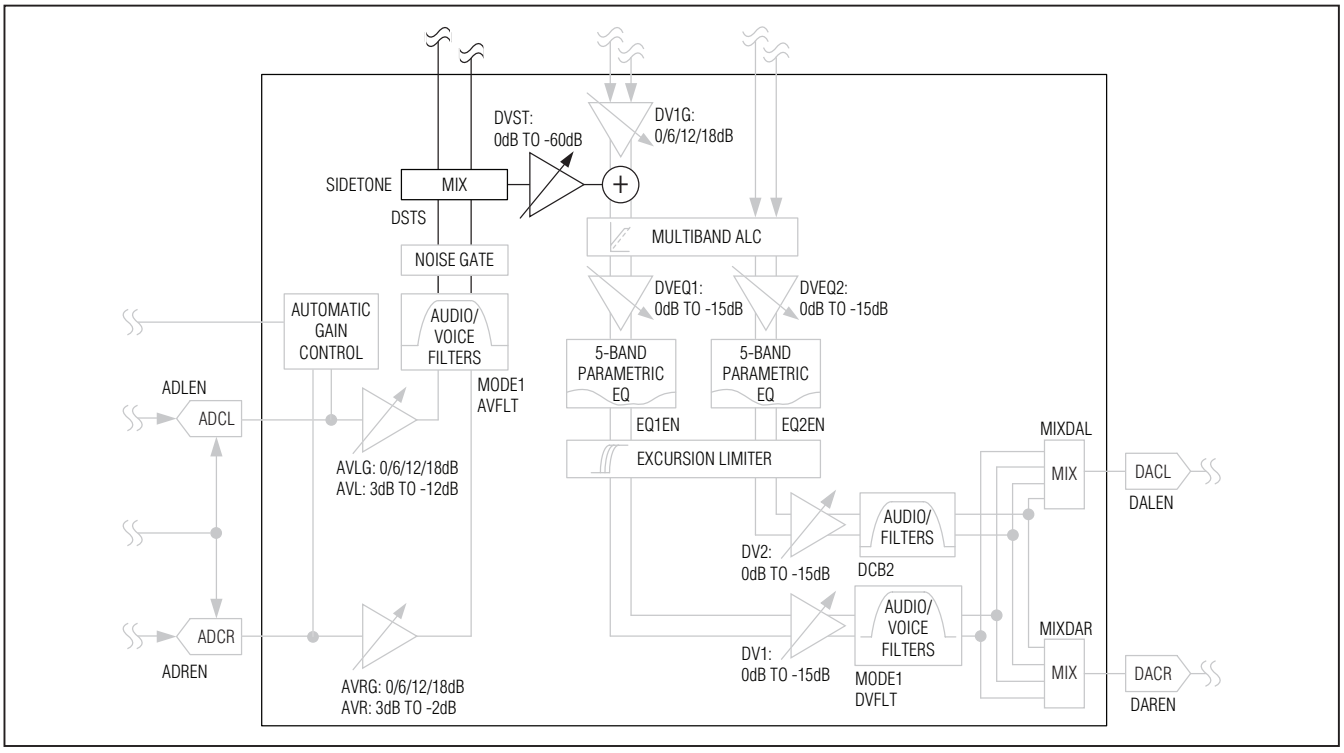


Figure 14. Sidetone Block Diagram

Table 8. Sidetone Register

REGISTER	BIT	NAME	DESCRIPTION			
0x2A	7	DSTS	**Sidetone Source** Selects which ADC output is fed back as sidetone. When mixing the left and right ADC outputs, each is attenuated by 6dB to prevent full-scale signals from clipping. 00 = Sidetone disabled 01 = Left ADC 10 = Right ADC 11 = Left + Right ADC			
	6					
	4	DVST	**Sidetone Level** Adjusts the sidetone signal level. All levels are referenced to the ADC's full-scale output.			
			VALUE	**LEVEL (dB)**	**VALUE**	**LEVEL (dB)**
	3		0x00	Sidetone disabled	0x10	-30.5
			0x01	-0.5	0x11	-32.5
			0x02	-2.5	0x12	-34.5
			0x03	-4.5	0x13	-36.5
	2		0x04	-6.5	0x14	-38.5
			0x05	-8.5	0x15	-40.5
			0x06	-10.5	0x16	-42.5
			0x07	-12.5	0x17	-44.5
	1		0x08	-14.5	0x18	-46.5
			0x09	-16.5	0x19	-48.5
			0x0A	-18.5	0x1A	-50.5
			0x0B	-20.5	0x1B	-52.5
	0		0x0C	-22.5	0x1C	-54.5
			0x0D	-24.5	0x1D	-56.6
			0x0E	-26.5	0x1E	-58.5
			0x0F	-28.5	0x1F	-60.5

Digital Audio Interfaces

The IC includes two separate playback signal paths and one record signal path. Digital audio interface 1 (DAI1) is used to transmit the recorded stereo audio signal and receive a stereo audio signal for playback. Digital audio interface 2 (DAI2) is used to receive a second stereo audio signal. Use DAI1 for all full-duplex operations and for all voice signals. Use DAI2 for music and to mix two playback audio signals. The digital audio interfaces are separate from the audio ports to enable either interface to communicate with any external device connected to the audio ports.

Each audio interface can be configured in a variety of formats including left justified, I²S, PCM, and time division multiplexed (TDM). TDM mode supports up to 4 mono audio slots in each frame. The IC can use up to 2 mono slots per interface, leaving the remaining two slots available for another device. Table 9 shows how to configure the device for common digital audio formats. Figures 16 and 17 show examples of common audio formats. By default, SDOUTS1 and SDOUTS2 are set high impedance when the IC is not outputting data to facilitate sharing the bus. Configure the interface in TDM mode using only slot 1 to transmit and receive mono PCM voice data.

The IC's digital audio interfaces support both ADC to DAC loop-through and digital loopback. Loop-through allows the signal converted by the ADC to be routed to the DAC for playback. The signal is routed from the record path to the playback path in the digital audio interface to allow the IC's full complement of digital signal processing to be used. Loopback allows digital

data input to either SDINS1 or SDINS2 to be routed from one interface to the other for output on SDOUTS2 or SDOUTS1. Both interfaces must be configured for the same sample rate, but the interface format need not be the same. This allows the IC to route audio data from one device to another, converting the data format as needed. Figure 15 shows the available digital signal routing options.

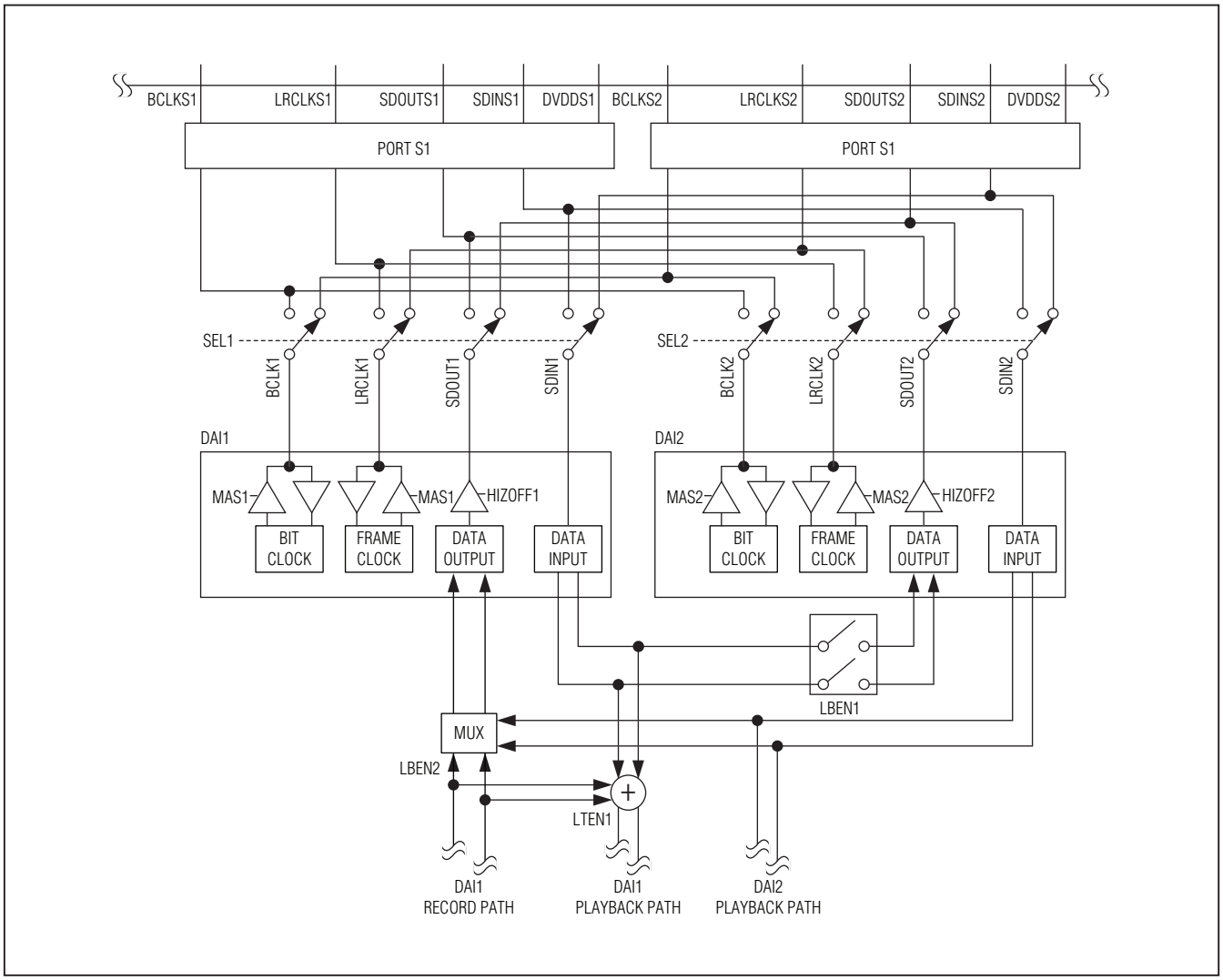


Figure 15. Digital Audio Signal Routing

Table 9. Common Digital Audio Formats

MODE	WCI1/WCI2	BCI1/BCI2	DLY1/DLY2	TDM1/TDM2	SLOTL1/SLOTL2	SLOTR1/SLOTR2
Left Justified	Set as desired	Set as desired	0	0	X	X
I²S	1	0	1	0	X	X
PCM	X	1	X	1	0	0
TDM	X	1	X	1	Set as desired	

X = Don't care.

Table 10. Digital Audio Interface Registers

REGISTER	BIT	NAME	DESCRIPTION
0x14/0x1C	7	MAS1/MAS2	**DAI1/DAI2 Master Mode** In master mode, DAI1/DAI2 outputs LRCLK and BCLK. In slave mode, DAI1/DAI2 accept LRCLK and BCLK as inputs. 0 = Slave mode 1 = Master mode
	6	WCI1/WCI2	**DAI1/DAI2 Word Clock Invert** TDM1/TDM2 = 0: 0 = Left-channel data is transmitted while LRCLK is low. 1 = Right-channel data is transmitted while LRCLK is low. TDM1/TDM2 = 1: Always set WCI = 0.
	5	BCI1/BCI2	**DAI1/DAI2 Bit Clock Invert** BCI1/BCI2 must be set to 1 when TDM1/TDM2 = 1. 0 = SDIN is accepted on the rising edge of BCLK. SDOUT is valid on the rising edge of BCLK. 1 = SDIN is accepted on the falling edge of BCLK. SDOUT is valid on the falling edge of BCLK. Master Mode: 0 = LRCLK transitions on the falling edge of BCLK. 1 = LRCLK transitions on the rising edge of BCLK.
	4	DLY1/DLY2	**DAI1/DAI2 Data Delay** DLY1/DLY2 has no effect when TDM1/TDM2 = 1. 0 = The most significant data bit is clocked on the first active BCLK edge after an LRCLK transition. 1 = The most significant data bit is clocked on the second active BCLK edge after an LRCLK transition.
	2	TDM1/TDM2	**DAI1/DAI2 Time-Division Multiplex Mode (TDM Mode)** Set TDM1/TDM2 when communicating with devices that use a frame synchronization pulse on LRCLK instead of a square wave. 0 = Disabled 1 = Enabled (BCI1/BCI2 must be set to 1)
	1	FSW1/FSW2	**DAI1/DAI2 Wide Frame Sync Pulse** Increases the width of the frame sync pulse to the full data width when TDM1/TDM2 = 1. FSW1/FSW2 has no effect when TDM1/TDM2 = 0. 0 = Disabled 1 = Enabled
	0	WS1/WS2	**DAI1/DAI2 Audio Data Bit Depth** Determines the maximum bit depth of audio being transmitted and received. Data is always 16 bit when TDM1/TMD2 = 0. 0 = 16 bits 1 = 24 bits

Table 10. Digital Audio Interface Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
0x15/0x1D	7	OSR1	**ADC Oversampling Ratio** Use the higher setting for maximum performance. Use the lower setting for reduced power consumption at the expense of performance. 00 = 96x 01 = 64x 10 = Reserved 11 = Reserved
	6		
	2	BSEL1/ BSEL2	**DAI1/DAI2 BCLK Output Frequency** When operating in master mode, BSEL1/BSEL2 set the frequency of BCLK. When operating in slave mode, BSEL1/BSEL2 have no effect. Select the lowest BCLK frequency that clocks all data input to the DAC and output by the ADC. 000 = BCLK disabled 001 = 64 x LRCLK 010 = 48 x LRCLK 011 = 128 x LRCLK (invalid for DHF1/DHF2 = 1) 100 = PCLK/2 101 = PCLK/4 110 = PCLK/8 111 = PCLK/16
	1		
	0		
0x16/0x1E	7	SEL1/SEL2	**DAI1/DAI2 Audio Port Selector** Selects which port is used by DAI1/DAI2. 00 = None 01 = Port S1 10 = Port S2 11 = Reserved
	6		
	5	LTEN1	**DAI1 Digital Loopthrough** Connects the output of the record signal path to the input of the playback path. Data input to DAI1 from an external device is mixed with the recorded audio signal. 0 = Disabled 1 = Enabled
	4	LBEN1/ LBEN2	**DAI1/DAI2 Digital Audio Interface Loopback** LBEN1 routes the digital audio input to DAI1 back out on DAI2. LBEN2 routes the digital audio input to DAI2 back out on DAI1. Selecting LBEN2 disables the ADC output data. 0 = Disabled 1 = Enabled
	3	DMONO1/ DMONO2	**DAI1/DAI2 DAC Mono Mix** Mixes the left and right digital input to mono and routes the combined signal to the left and right playback paths. The left and right input data is attenuated by 6dB prior to the mono mix. 0 = Disabled 1 = Enabled

Table 10. Digital Audio Interface Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
0x16/0x1E	2	HIZOFF1/ HIZOFF2	**Disable DA1/DAI2 Output High-Impedance Mode** Normally SDOUT is set high impedance between data words. Set HIZOFF1/HIZOFF2 to force a level on SDOUT at all times. 0 = Disabled 1 = Enabled
	1	SDOEN1/ SDOEN2	**DAI1/DAI2 Record Path Output Enable** DAI2 outputs data only if LBEN1 = 1. 0 = Disabled 1 = Enabled
	0	SDIEN1/ SDIEN2	**DAI1/DAI2 Playback Path Input Enable** 0 = Disabled 1 = Enabled
0x17/0x1F	7 6	SLOTL1/ SLOTL2	**TDM Left Time Slot** Selects which of the four slots is used for left data on DAI1/DAI2. If the same slot is selected for left and right audio, left audio is placed in the slot. 00 = Slot 1 01 = Slot 2 10 = Slot 3 11 = Slot 4
	5 4	SLOTR1/ SLOTR2	**TDM Right Time Slot** Selects which of the four slots is used for right data on DAI1/DAI2. If the same slot is selected for left and right audio, left audio is placed in the slot. 00 = Slot 1 01 = Slot 2 10 = Slot 3 11 = Slot 4
	3 2 1 0	SLOTDLY1/ SLOTDLY2	**TDM Slot Delay** Adds 1 BCLK cycle delay to the data in the specified TDM slot. 1xxx = Slot 4 delayed x1xx = Slot 3 delayed xx1x = Slot 2 delayed xxx1 = Slot 1 delayed

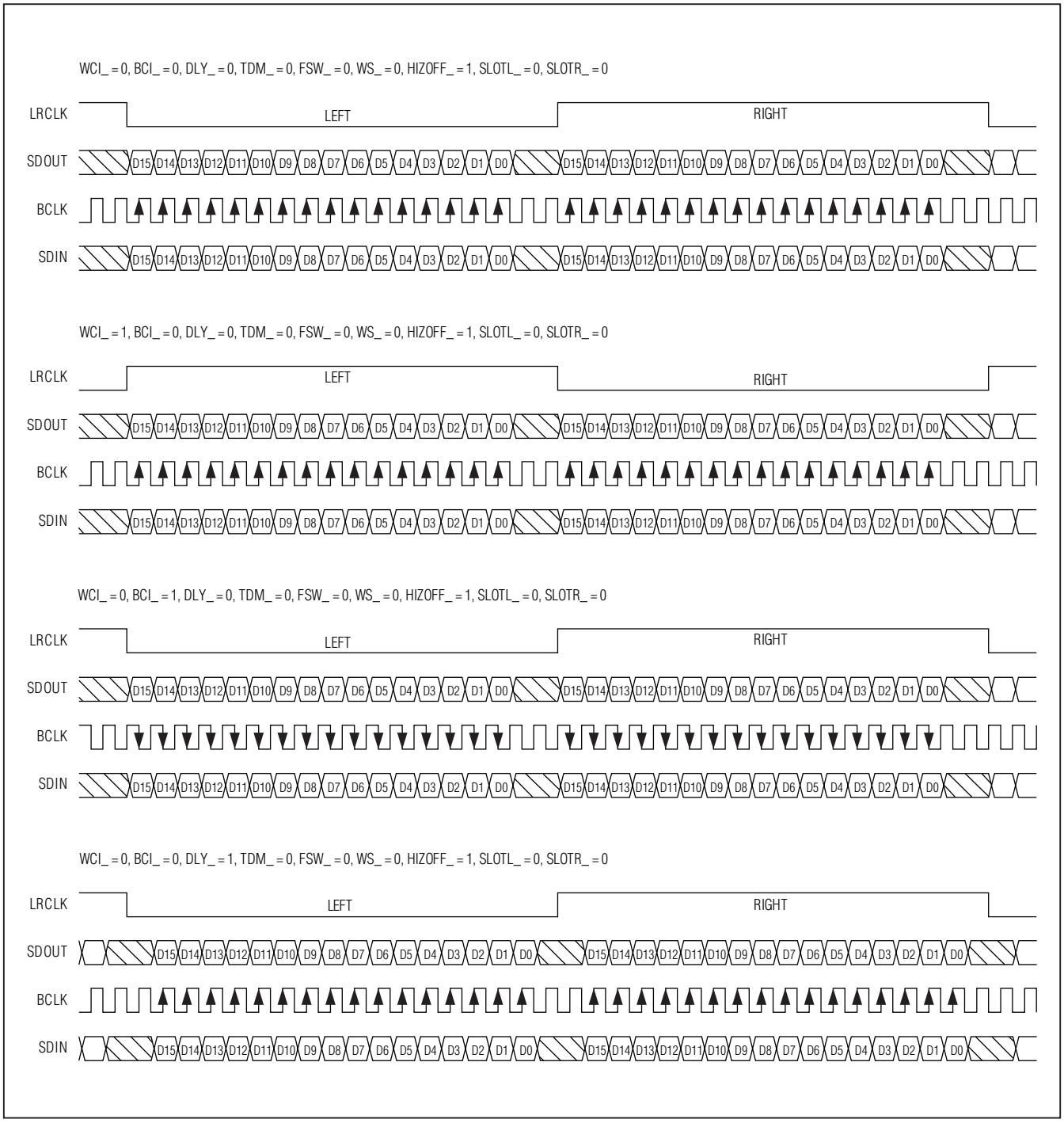


Figure 16. Non-TDM Data Format Examples

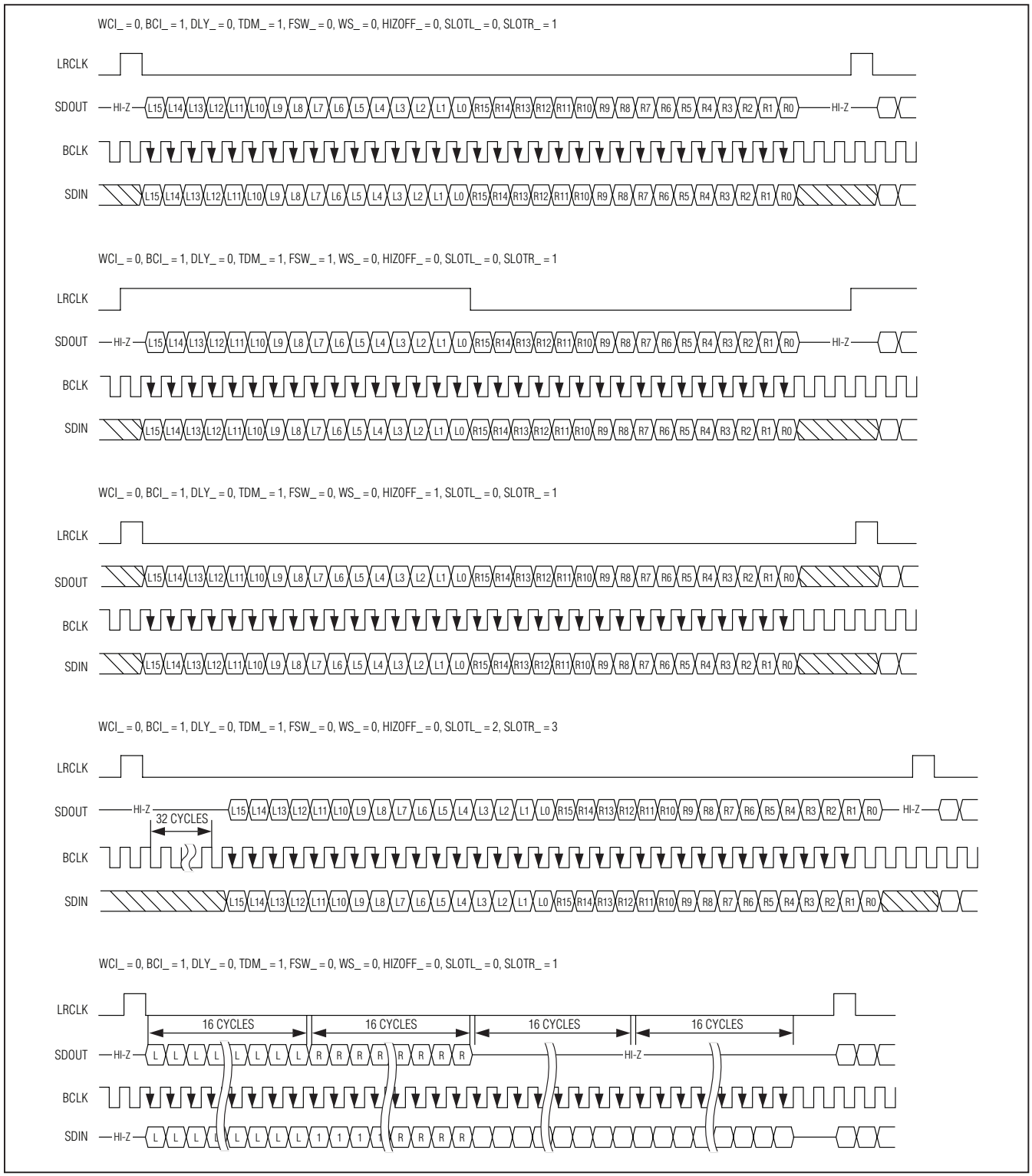


Figure 17. TDM Mode Data Format Examples

Stereo Audio CODEC with FlexSound Technology

Clock Control

The digital signal paths in the IC require a master clock (MCLK) between 10MHz and 60MHz to function. Internally, the MAX9888 requires a clock between 10MHz and 20MHz. A prescaler divides MCLK by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the IC.

The MAX9888 includes two digital audio signal paths, both capable of supporting any sample rate from 8kHz to 96kHz. Each path is independently configured to allow different sample rates. To accommodate a wide range of system architectures, three main clocking modes are supported:

- **PLL Mode:** When operating in slave mode, enable the PLL to lock onto any LRCLK input. This mode requires the least configuration, but provides the lowest performance. Use this mode to simplify initial setup or when normal mode and exact integer mode cannot be used.
- **Normal Mode:** This mode uses a 15-bit clock divider to set the sample rate relative to PCLK. This allows high flexibility in both the PCLK and LRCLK frequencies and can be used in either master or slave mode.
- **Exact Integer Mode (DAI1 only):** In both master and slave modes, common MCLK frequencies (12MHz, 13MHz, 16MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ1 bits instead of the NI, and PLL control bits.

Table 11. Clock Control Registers

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="2">0x10</td><td>5</td><td rowspan="2">PSCLK</td><td colspan="4">MCLK Prescaler
Generates PCLK, which is used by all internal circuitry.
00 = PCLK disabled
01 = 10MHz ≤ MCLK ≤ 20MHz (PCLK = MCLK)
10 = 20MHz ≤ MCLK ≤ 40MHz (PCLK = MCLK/2)
11 = 40MHz ≤ MCLK ≤ 60MHz (PCLK = MCLK/4)</td></tr>
<tr><td>4</td></tr>
<tr><td rowspan="11">0x11/0x19</td><td>7</td><td rowspan="11">SR1/SR2</td><td colspan="4">DAI1/DAI2 Sample Rate
Used by the ALC to correctly set the dual-band crossover frequency and the excursion limiter to set the predefined corner frequencies.</td></tr>
<tr><td>6</td><td>VALUE</td><td>SAMPLE RATE (kHz)</td><td>VALUE</td><td>SAMPLE RATE (kHz)</td></tr>
<tr><td rowspan="4">5</td><td>0x0</td><td>Reserved</td><td>0x8</td><td>48</td></tr>
<tr><td>0x1</td><td>8</td><td>0x9</td><td>88.2</td></tr>
<tr><td>0x2</td><td>11.025</td><td>0xA</td><td>96</td></tr>
<tr><td>0x3</td><td>16</td><td>0xB</td><td>Reserved</td></tr>
<tr><td rowspan="4">4</td><td>0x4</td><td>22.05</td><td>0xC</td><td>Reserved</td></tr>
<tr><td>0x5</td><td>24</td><td>0xD</td><td>Reserved</td></tr>
<tr><td>0x6</td><td>32</td><td>0xE</td><td>Reserved</td></tr>
<tr><td>0x7</td><td>44.1</td><td>0xF</td><td>Reserved</td></tr>
</table>

Table 11. Clock Control Registers (continued)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="11">0x11</td><td rowspan="3">3</td><td rowspan="11">FREQ1</td><td colspan="4">Exact Integer Mode
Overrides PLL1 and NI1 and configures a specific PCLK to LRCLK ratio.</td></tr>
<tr><td>VALUE</td><td>SAMPLE RATE</td><td>VALUE</td><td>SAMPLE RATE</td></tr>
<tr><td>0x0</td><td>Disabled</td><td>0x8</td><td>PCLK = 12MHz,
LRCLK = 8kHz</td></tr>
<tr><td rowspan="4">2</td><td>0x1</td><td>Reserved</td><td>0x9</td><td>PCLK = 12MHz,
LRCLK = 16kHz</td></tr>
<tr><td>0x2</td><td>Reserved</td><td>0xA</td><td>PCLK = 13MHz,
LRCLK = 8kHz</td></tr>
<tr><td>0x3</td><td>Reserved</td><td>0xB</td><td>PCLK = 13MHz,
LRCLK = 16kHz</td></tr>
<tr><td>0x4</td><td>Reserved</td><td>0xC</td><td>PCLK = 16MHz,
LRCLK = 8kHz</td></tr>
<tr><td rowspan="3">1</td><td>0x5</td><td>Reserved</td><td>0xD</td><td>PCLK = 16MHz,
LRCLK = 16kHz</td></tr>
<tr><td>0x6</td><td>Reserved</td><td>0xE</td><td>PCLK = 19.2MHz,
LRCLK = 8kHz</td></tr>
<tr><td>0x7</td><td>Reserved</td><td>0xF</td><td>PCLK = 19.2MHz,
LRCLK = 16kHz</td></tr>
<tr><td rowspan="9">0x12/0x1A</td><td>7</td><td>PLL1/PLL2</td><td colspan="4">PLL Mode Enable (Slave Mode Only)
PLL1/PLL2 enables a digital PLL that locks on to the externally supplied LRCLK frequency and automatically sets the LRCLK divider (NI1/NI2).
0 = Disabled
1 = Enabled</td></tr>
<tr><td>6</td><td rowspan="10">NI1/
NI2</td><td colspan="4" rowspan="2">Normal Mode LRCLK Divider
When PLL1/PLL2 = 0, the frequency of LRCLK is determined by NI1/NI2. See Table 12 for common NI values.</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td>SAMPLE RATE</td><td colspan="2">DHF1/DHF2</td><td>NI1/NI2 FORMULA</td></tr>
<tr><td>3</td><td rowspan="2">8kHz ≤ LRCLK ≤ 48kHz</td><td colspan="2" rowspan="2">0</td><td rowspan="2">$NI = \frac{65536 \times 96 \times f_{LRCLK}}{f_{PCLK}}$</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td><td rowspan="6">48kHz < LRCLK ≤ 96kHz</td><td colspan="2" rowspan="6">1</td><td rowspan="6">$NI = \frac{65536 \times 48 \times f_{LRCLK}}{f_{PCLK}}$</td></tr>
<tr><td>0</td></tr>
<tr><td rowspan="5">0x13/0x1B</td><td>7</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
<tr><td>3</td><td colspan="4">f_{LRCLK} = LRCLK frequency
f_{PCLK} = Prescaled MCLK frequency (PCLK)</td></tr>
<tr><td></td><td>2</td><td></td><td colspan="4"></td></tr>
<tr><td></td><td>1</td><td></td><td colspan="4"></td></tr>
<tr><td></td><td>0</td><td>NI1[0]/NI2[0]</td><td colspan="4">Rapid Lock Mode
Program NI1/NI2 to the nearest valid ratio and set NI1[0]/NI2[0] when PLL1/PLL2 = 1 to enable rapid lock mode. Normally, the PLL automatically calculates and dynamically adjusts NI1/NI2. When rapid lock mode is properly configured, the PLL starting point is much closer to the correct value, thus speeding up lock time. Wait one LRCLK period after programming NI1/NI2 before setting PLL1/PLL2 = 1.</td></tr>
</table>

Table 12. Common NI1/NI2 Values

PCLK (MHz)	LRCLK (kHz)											
	DHF1/2 = 0									DHF1/2 = 1		
	8	11.025	12	16	22.05	24	32	44.1	48	64	88.2	96
10	13A9	1B18	1D7E	2752	3631	3AFB	4EA5	6C61	75F7	4EA5	6C61	75F7
11	11E0	18A2	1ACF	23BF	3144	359F	477E	6287	6B3E	477E	6287	6B3E
11.2896	116A	**1800**	1A1F	22D4	**3000**	343F	45A9	**6000**	687D	45A9	**6000**	687D
12	1062	1694	1893	20C5	2D29	3127	4189	5A51	624E	4189	5A51	624E
12.288	**1000**	160D	**1800**	**2000**	2C1A	**3000**	**4000**	5833	**6000**	**4000**	5833	**6000**
13	0F20	14D8	16AF	1E3F	29AF	2D5F	3C7F	535F	5ABE	3C7F	535F	5ABE
16	0C4A	10EF	126F	1893	21DE	24DD	3127	43BD	49BA	3127	43BD	49BA
16.9344	0B9C	**1000**	116A	1738	**2000**	22D4	2E71	**4000**	45A9	2E71	**4000**	45A9
18.432	0AAB	0EB3	**1000**	1555	1D66	**2000**	2AAB	3ACD	**4000**	2AAB	3ACD	**4000**
20	09D5	0D8C	0EBF	13A9	1B18	1D7E	2752	3631	3AFB	2752	3631	3AFB

Note: *Values in bold are exact integers that provide maximum full-scale performance.*

Passband Filtering

Each digital signal path in the IC includes options for defining the path bandwidth (Figure 18). The playback and record paths connected to DAI1 support both voice and music filtering while the playback path connected to DAI2 supports music filtering only.

The voice IIR filters provide greater than 70dB stopband attenuation at frequencies above $f_S/2$ to reduce aliasing. Three selectable highpass filters eliminate unwanted low-frequency signals.

Use music mode when processing high-fidelity audio content. The music FIR filters reduce power consumption and are linear phase to maintain stereo imaging. An optional DC-blocking filter is available to eliminate unwanted DC offset.

In music mode, a second set of FIR filters are available to support sample rates greater than 50kHz. The filters can be independently selected for DAI1 and DAI2 and support both the playback and record audio paths.

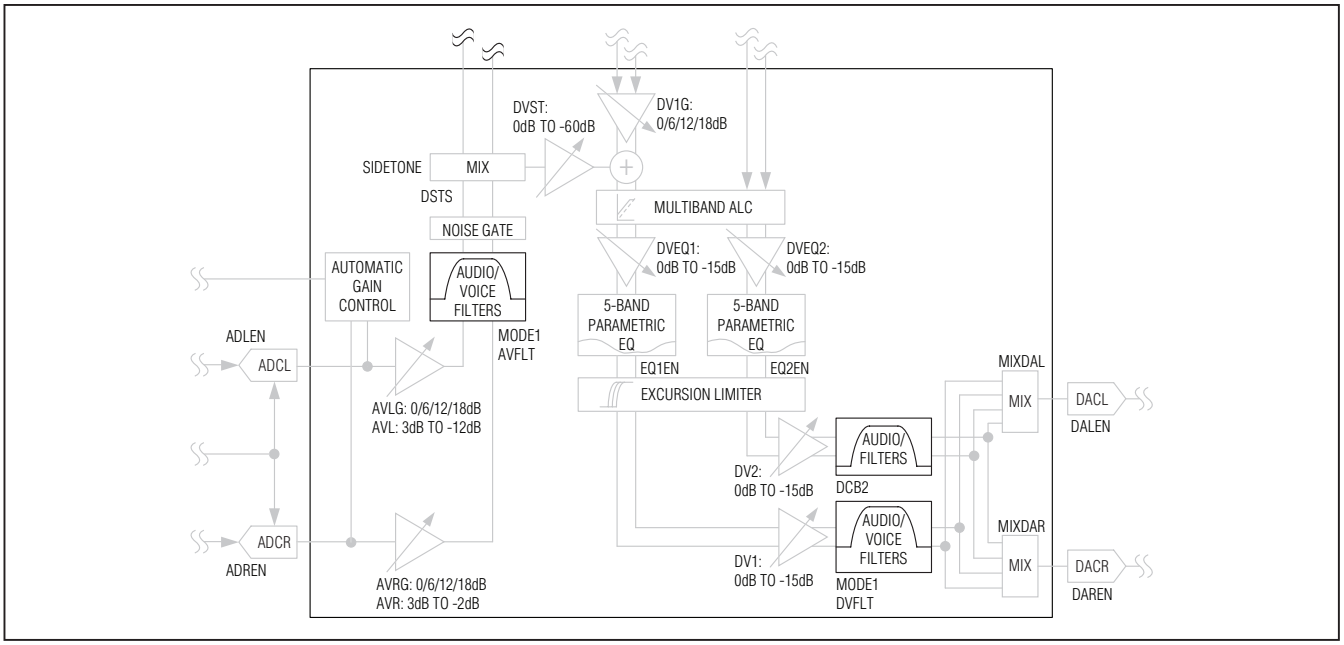
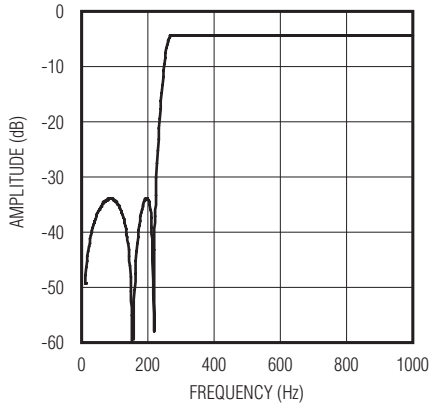
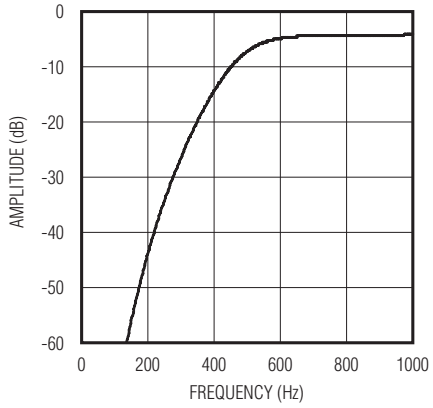
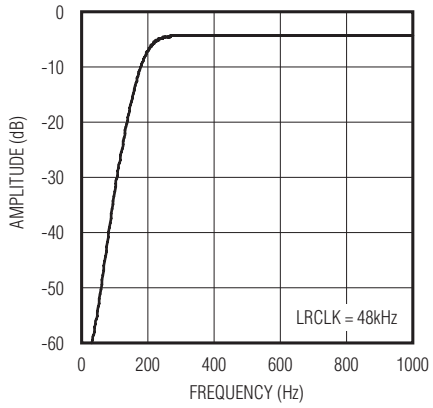


Figure 18. Digital Passband Filtering Block Diagram

Table 13. Passband Filtering Registers

REGISTER	BIT	NAME	DESCRIPTION	
0x18	7	MODE1	**DAI1 Passband Filtering Mode** 0 = Voice filters 1 = Music filters (recommended for f_S > 24kHz)	
	6	AVFLT1	**DAI1 ADC Highpass Filter Mode**	
	5		**MODE1**	**AVFLT1**
	4		0	See Table 14
			1	Select a nonzero value to enable the DC-blocking filter
	3	DHF1	**DAI1 High Sample Rate Mode** Selects the sample rate range. 0 = 8kHz ≤ LRCLK ≤ 48kHz 1 = 48kHz ≤ LRCLK < 96kHz	
	2	DVFLT1	**DAI1 DAC Highpass Filter Mode**	
	1		**MODE1**	**DVFLT1**
	0		0	See Table 14
			1	Select a nonzero value to enable the DC-blocking filter
0x20	3	DHF2	**DAI2 High Sample Rate Mode** Selects the sample rate range. 0 = 8kHz ≤ LRCLK ≤ 48kHz 1 = 48kHz < LRCLK ≤ 96kHz	
	0	DCB2	**DAI2 DC Blocking Filter** Enables a DC-blocking filter on the DAI2 playback audio path. 0 = Disabled 1 = Enabled	

Table 14. Voice Highpass Filters

AVFTL/DVFLT VALUE	INTENDED SAMPLE RATE	FILTER RESPONSE
000	N/A	Disabled
001/011	16kHz/8kHz	
010/100	16kHz/8kHz	
101	8kHz to 48kHz	
110/111	N/A	Reserved

Playback Path Signal Processing

The IC playback signal path includes automatic level control (ALC) and a 5-band parametric equalizer (EQ) (Figure 19). The DAI1 and DAI2 playback paths include separate ALCs controlled by a single set of registers. Two completely separate parametric EQs are included for the DAI1 and DAI2 playback paths.

Automatic Level Control

The automatic level control (ALC) circuit ensures maximum signal amplitude without producing audible clipping. This is accomplished by a variable gain stage that works on a sample by sample basis to increase the gain up to 12dB. A look-ahead circuit determines if the next sample exceeds full scale and reduces the gain so that the sample is exactly full scale.

A programmable low signal threshold determines the minimum signal amplitude that is amplified. Select a threshold that prevents the amplification of background noise. When the signal level drops below the low signal threshold, the ALC reduces the gain to 0dB until the signal increases above the threshold. Figure 20 shows an example of ALC input vs. output curves.

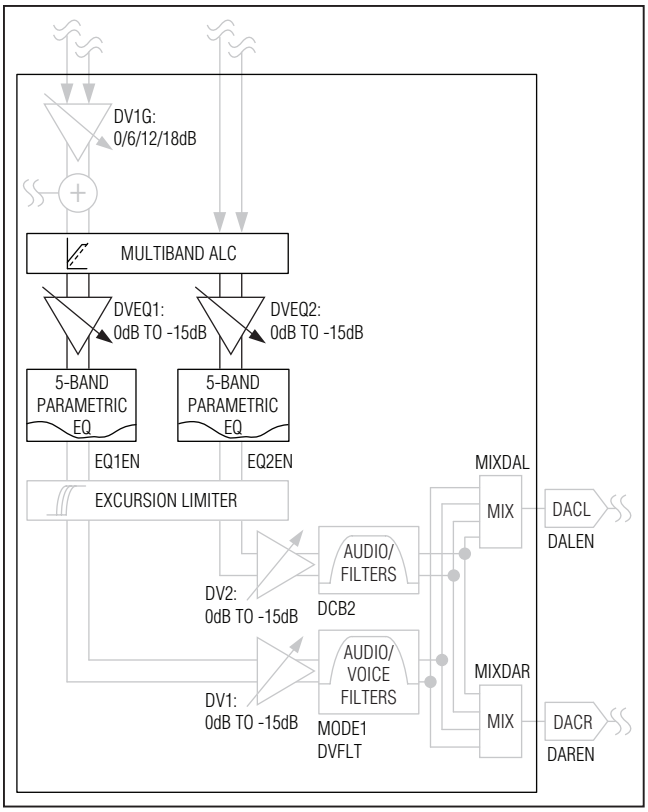


Figure 19. Playback Path Signal Processing Block Diagram

The ALC can optionally be configured in dual-band mode. In this mode, the input signal is filtered into two bands with a 5kHz center frequency. Each band is routed through independent ALCs and then summed together. In multiband mode, both bands use the same parameters.

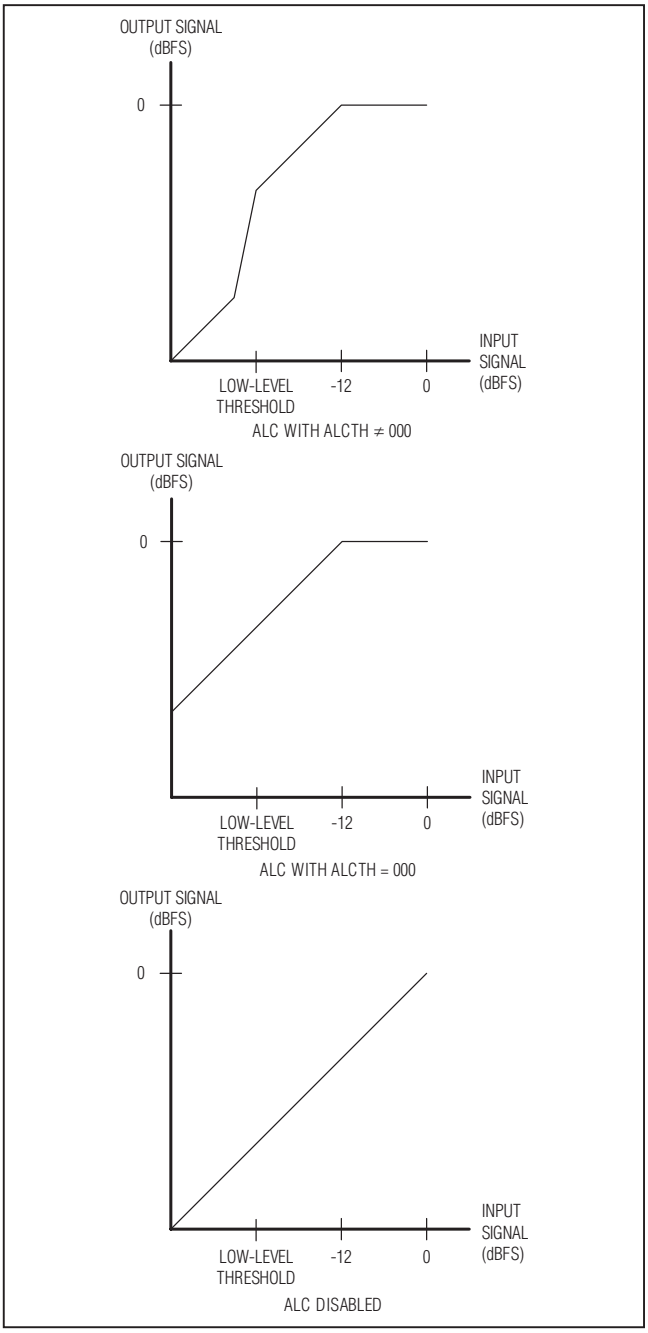


Figure 20. ALC Input vs. Output Examples

Table 15. Automatic Level Control Registers

REGISTER	BIT	NAME	DESCRIPTION
0x41	7	ALCEN	**ALC Enable** Enables ALC on both the DAI1 and DAI2 playback paths. 0 = Disabled 1 = Enabled
	6, 5, 4	ALCRLS	**ALC and Excursion Limiter Release Time** Sets the release time for both the ALC and Excursion Limiter. See the *Excursion Limiter* section for Excursion Limiter release times. ALC release time is defined as the time required to adjust the gain from 12dB to 0dB.
			VALUE / **ALC RELEASE TIME (s)** 000 = 8 001 = 4 010 = 2 011 = 1 100 = 0.5 101 = 0.25 110 = Reserved 111 = Reserved
	3	ALCMB	**Multiband Enable** Enables dual-band processing with a 5kHz center frequency. SR1 and SR2 must be configured properly to achieve the correct center frequency for each playback path. 0 = Single-band ALC 1 = Dual-band ALC
	2, 1, 0	ALCTH	**Low Signal Threshold** Selects the minimum signal level to be boosted by the ALC. 000 = -∞dB (low-signal threshold disabled) 001 = -12dB 010 = -18dB 011 = -24dB 100 = -30dB 101 = -36dB 110 = -42dB 111 = -48dB

Parametric Equalizer

The parametric EQ contains five independent biquad filters with programmable gain, center frequency, and bandwidth. Each biquad filter has a gain range of ±12dB and a center frequency range from 20Hz to 20kHz. Use a filter Q less than that shown in Figure 21 to achieve ideal frequency responses. Setting a higher Q results in non-ideal frequency response. The biquad filters are series connected, allowing a total gain of ±60dB.

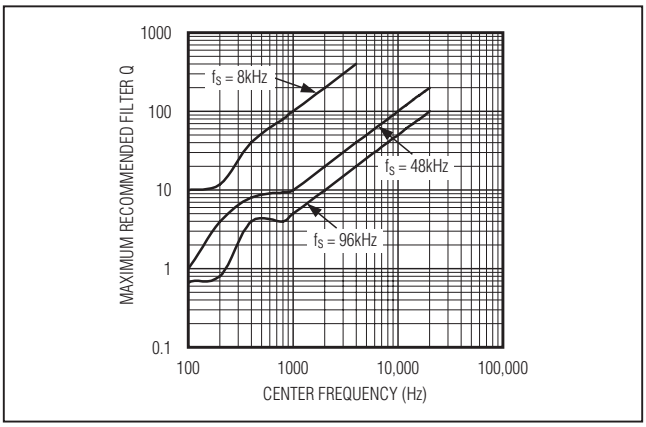


Figure 21. Maximum Recommended Filter Q vs. Frequency

Use the attenuator at the EQ's input to avoid clipping the signal. The attenuator can be programmed for fixed attenuation or dynamic attenuation based on signal level. If the dynamic EQ clip detection is enabled, the signal level from the EQ is fed back to the attenuator circuit to determine the amount of gain reduction necessary to avoid clipping.

The MAX9888 EV kit software includes a graphic interface for generating the EQ coefficients. The coefficients are sample rate dependent and stored in registers 0x50 through 0xB3.

Table 16. EQ Registers

REGISTER	BIT	NAME	DESCRIPTION			
0x2C/0x2E	4	$\overline{\text{EQCLP1}}$/$\overline{\text{EQCLP2}}$	**DAI1/DAI2 EQ Clip Detection** Automatically controls the EQ attenuator to prevent clipping in the EQ. 0 = Enabled 1 = Disabled			
	3	DVEQ1/DVEQ2	**DAI1/DAI2 EQ Attenuator** Provides attenuation to prevent clipping in the EQ when full-scale signals are boosted. DVEQ1/DVEQ2 operates only when EQ1EN/EQ2EN = 1 and $\overline{\text{EQCLP1}}$/$\overline{\text{EQCLP2}}$ = 1.			
	2		**VALUE**	**GAIN (dB)**	**VALUE**	**GAIN (dB)**
			0x0	0	0x8	-8
			0x1	-1	0x9	-9
	1		0x2	-2	0xA	-10
			0x3	-3	0xB	-11
			0x4	-4	0xC	-12
	0		0x5	-5	0xD	-13
			0x6	-6	0xE	-14
			0x7	-7	0xF	-15
0x47	7	$\overline{\text{VS2EN}}$	See the *Click-and-Pop Reduction* section.			
	6	$\overline{\text{VSEN}}$				
	5	$\overline{\text{ZDEN}}$				
	1	EQ2EN	**DAI2 EQ Enable** 0 = Disabled 1 = Enabled			
	0	EQ1EN	**DAI1 EQ Enable** 0 = Disabled 1 = Enabled			

Stereo Audio CODEC with FlexSound Technology

Playback Level Control

The IC includes separate digital level control for the DAI1 and DAI2 playback audio paths. The DAI1 signal path allows boost when MODE1 = 0 and attenuation in any mode. The DAI2 signal path allows attenuation only.

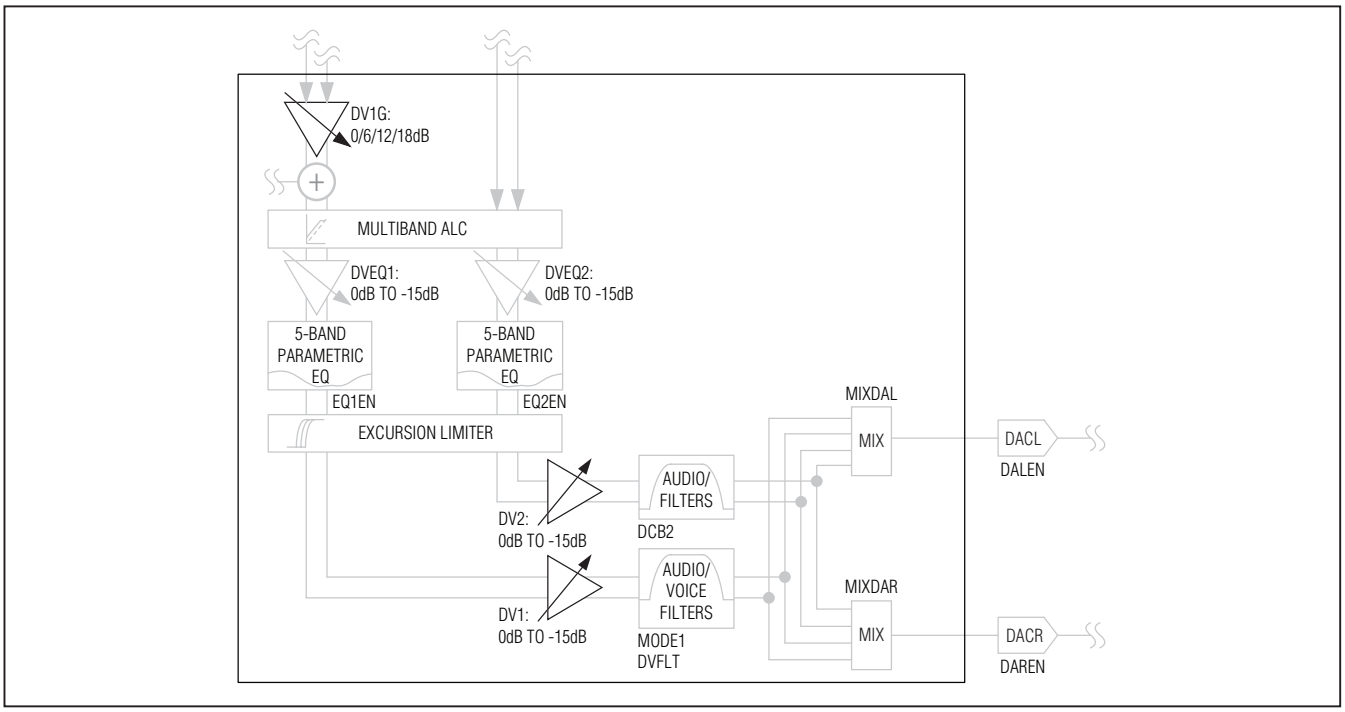


Figure 22. Playback Level Control Block Diagram

Table 17. DAC Playback Level Control Register

REGISTER	BIT	NAME	DESCRIPTION			
0x2B/0x2D	7	DV1M/DV2M	**DAI1/DAI2 Mute** 0 = Disabled 1 = Enabled			
	5	DV1G	**DAI1 Voice Mode Gain** DV1G only applies when MODE1 = 0. 00 = 0dB 01 = 6dB 10 = 12dB 11 = 18dB			
	4					
	3	DV1/DV2	**DAI1/DAI2 Attenuation**			
			VALUE	**GAIN (dB)**	**VALUE**	**GAIN (dB)**
	2		0x0	0	0x8	-8
			0x1	-1	0x9	-9
			0x2	-2	0xA	-10
	1		0x3	-3	0xB	-11
			0x4	-4	0xC	-12
			0x5	-5	0xD	-13
	0		0x6	-6	0xE	-14
			0x7	-7	0xF	-15

DAC Input Mixers

The IC's stereo DAC accepts input from two digital audio paths. The DAC mixer routes any audio path to the left and right DACs (Figure 23).

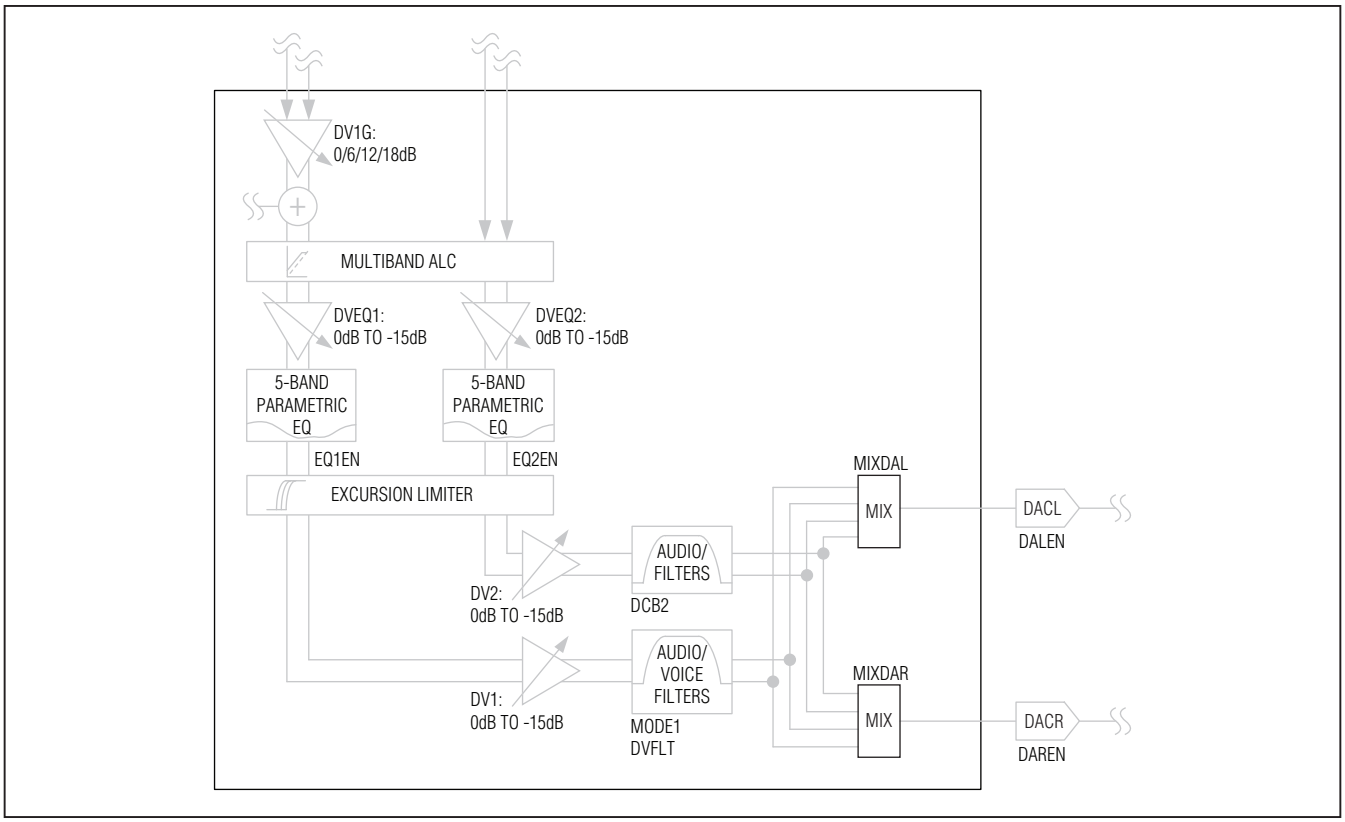


Figure 23. DAC Input Mixer Block Diagram

Table 18. DAC Input Mixer Register

REGISTER	BIT	NAME	DESCRIPTION
0x21	7	MIXDAL	**Left DAC Input Mixer** 1xxx = DAI1 left channel x1xx = DAI1 right channel xx1x = DAI2 left channel xxx1 = DAI2 right channel
	6		
	5		
	4		
	3	MIXDAR	**Right DAC Input Mixer** 1xxx = DAI1 left channel x1xx = DAI1 right channel xx1x = DAI2 left channel xxx1 = DAI2 right channel
	2		
	1		
	0		

Stereo Audio CODEC with FlexSound Technology

Preoutput Signal Path

The IC's preoutput mixer stage provides mixing and level adjustment for line input signals routed to the output amplifiers. Figure 24 shows a block diagram of the preoutput signal path. 9dB is added between the line input amplifiers and the output amplifiers to boost the 1V_{P-P} maximum line input signal level to the 1V_{RMS} maximum DAC signal level.

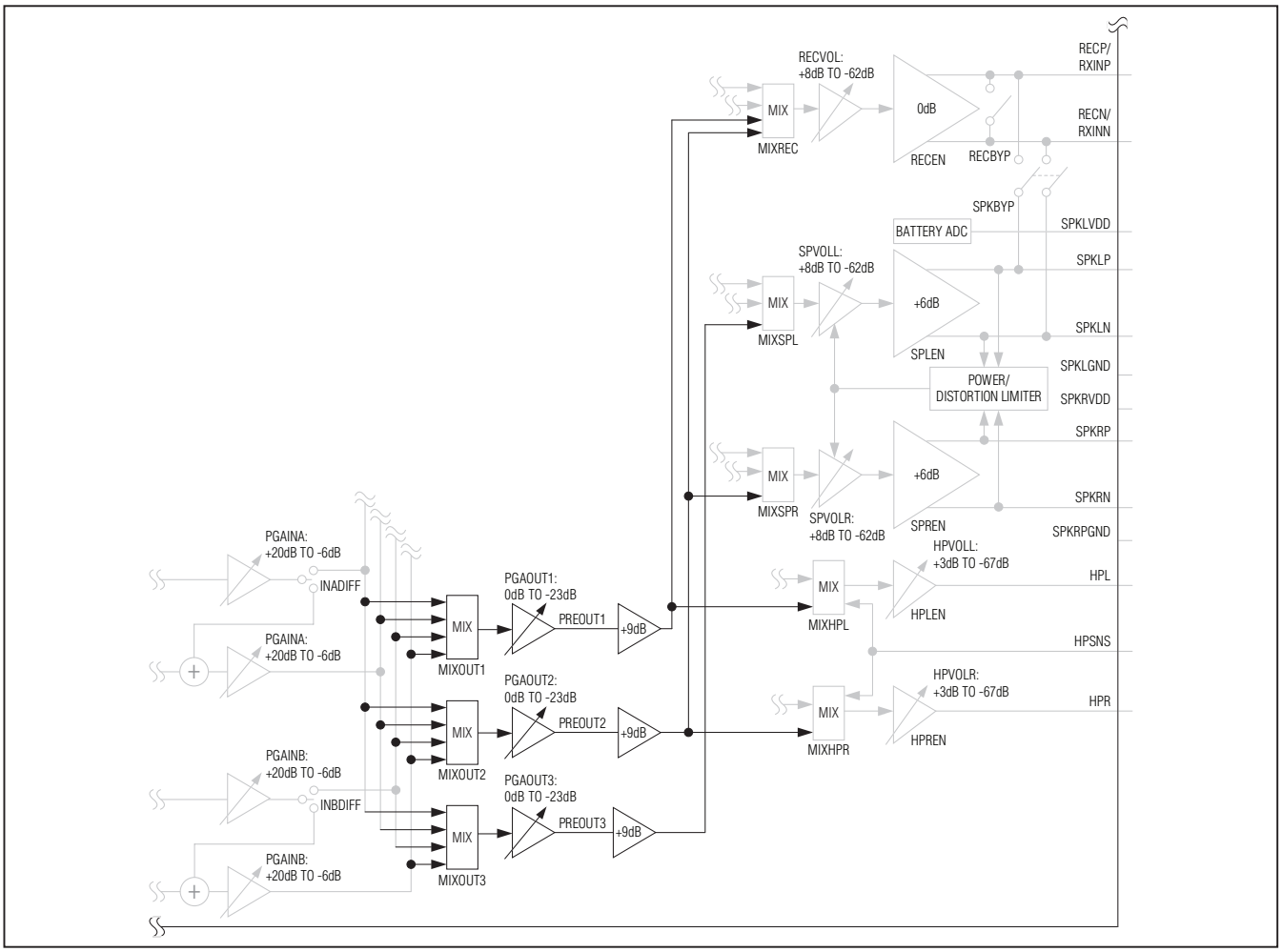


Figure 24. Preoutput Signal Path Block Diagram

Preoutput Mixer

The IC's output amplifiers each accept input from one of the three preoutput mixers. Configure each preoutput mixer to mix any combination of the four line input signals.

Table 19. Preoutput Mixer Registers

REGISTER	BIT	NAME	DESCRIPTION
0x24/0x25/ 0x26	3	MIXOUT1/ MIXOUT2/ MIXOUT3	**Preoutput Mixer 1** 1xxx = INA1 x1xx = INA2 (INADIFF = 0) or INA2 - INA1 (INADIFF = 1) xx1x = INB1 xxx1 = INB2 (INBDIFF = 0) or INB2 - INB1 (INBDIFF = 1)
	2		
	1		
	0		

Preoutput PGA

The IC's preoutput PGAs allow line input signals to be attenuated to match DAC output signal levels. Use the 0dB setting for maximum performance.

Table 20. Preoutput PGA Registers

REGISTER	BIT	NAME	DESCRIPTION			
0x35/0x36/ 0x37	3	PGAOUT1/ PGAOUT2/ PGAOUT3	Preoutput PGA Level			
			VALUE	GAIN (dB)	VALUE	GAIN (dB)
	2		0x0	0	0x8	-15
			0x1	-1	0x9	-17
	1		0x2	-3	0xA	-19
			0x3	-5	0xB	-21
			0x4	-7	0xC	-23
	0		0x5	-9	0xD	Mute
			0x6	-11	0xE	Mute
			0x7	-13	0xF	Mute

Receiver Amplifier

The IC includes a single differential receiver amplifier. The receiver amplifier is designed to drive 32Ω receivers. In cases where a single transducer is used for the loudspeaker and receiver, use the SPKBYP switch to route the receiver amplifier output to the left speaker outputs.

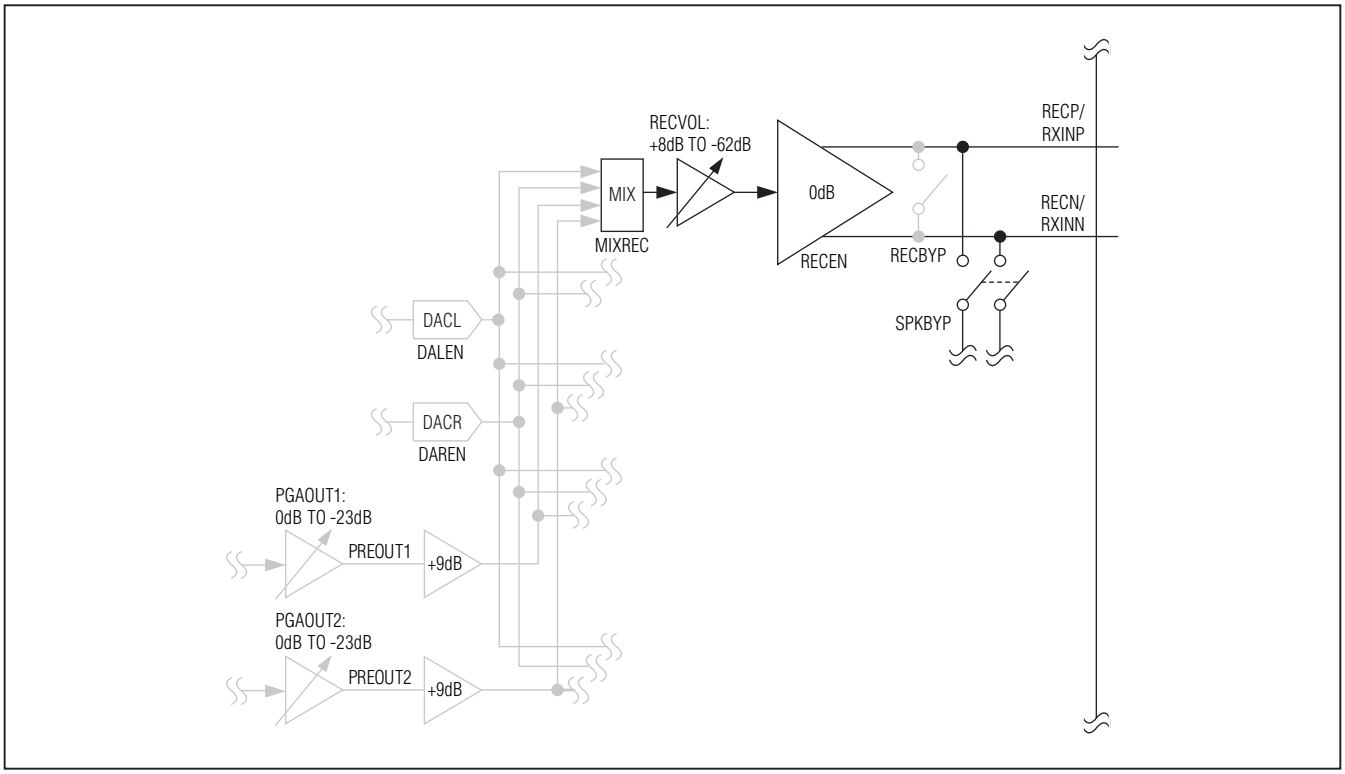


Figure 25. Receiver Amplifier Block Diagram

Receiver Output Mixer

The IC's receiver amplifier accepts input from the stereo DAC and the line inputs. Configure the mixer to mix any combination of the available sources. When more than one signal is selected, the mixed signal is attenuated by 6dB for 2 signals, 9.5dB for 3 signals, or 12dB for 4 signals.

Table 21. Receiver Output Mixer Register

REGISTER	BIT	NAME	DESCRIPTION
0x28	3	MIXREC	**Receiver Output Mixer** 1xxx = Left DAC x1xx = Right DAC xx1x = Preoutput mixer 1 xxx1 = Preoutput mixer 2
	2		
	1		
	0		

Receiver Output Volume

Table 22. Receiver Output Level Register

REGISTER	BIT	NAME	DESCRIPTION			
0x3A	7	RECM	**Receiver Output Mute** 0 = Disabled 1 = Enabled			
	4	RECVOL	**Receiver Output Volume Level**			
	3		**VALUE**	**VOLUME (dB)**	**VALUE**	**VOLUME (dB)**
			0x00	-62	0x10	-10
			0x01	-58	0x11	-8
			0x02	-54	0x12	-6
			0x03	-50	0x13	-4
	2		0x04	-46	0x14	-2
			0x05	-42	0x15	0
			0x06	-38	0x16	+1
			0x07	-35	0x17	+2
	1		0x08	-32	0x18	+3
			0x09	-29	0x19	+4
			0x0A	-26	0x1A	+5
			0x0B	-23	0x1B	+6
	0		0x0C	-20	0x1C	+6.5
			0x0D	-17	0x1D	+7
			0x0E	-14	0x1E	+7.5
			0x0F	-12	0x1F	+8

Speaker Amplifiers

The IC integrates a stereo filterless Class D amplifier that offers much higher efficiency than Class AB without the typical disadvantages.

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%, however, that efficiency is only exhibited at peak output power. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the IC's Class D amplifier still exhibits 80% efficiency under the same conditions.

Traditional Class D amplifiers require the use of external LC filters or shielding to meet EN55022B and FCC electromagnetic-interference (EMI) regulation standards. Maxim's patented active emissions limiting edge-rate control circuitry reduces EMI emissions (Figure 26).

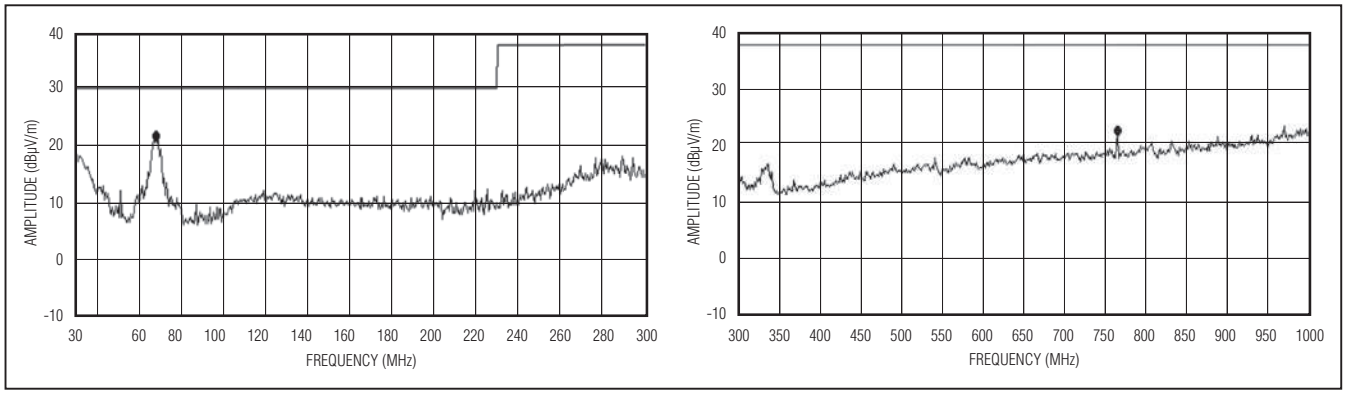


Figure 26. EMI with 15cm of Speaker Cable

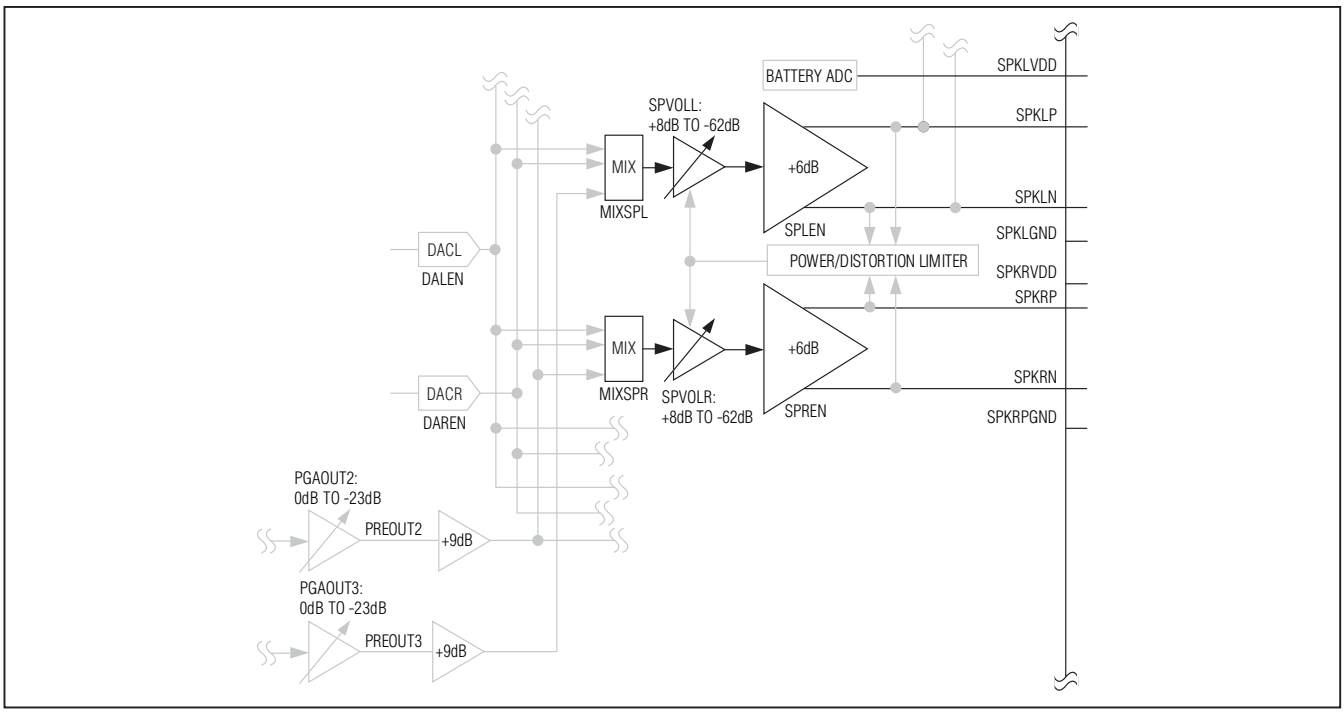


Figure 27. Speaker Amplifier Path Block Diagram

Stereo Audio CODEC with FlexSound Technology

Speaker Output Mixers

The IC's speaker amplifiers accept input from the stereo DAC and the line inputs. Configure the mixer to mix any combination of the available sources. When more than one signal is selected, the mixed signal is attenuated by 6dB for 2 signals, 9.5dB for 3 signals, or 12dB for four signals.

Table 23. Speaker Output Mixer Register

REGISTER	BIT	NAME	DESCRIPTION
0x29	7	MIXSPL	**Left Speaker Output Mixer** 1xxx = Left DAC x1xx = Right DAC xx1x = Reserved xxx1 = Preoutput mixer 3
	6		
	5		
	4		
	3	MIXSPR	**Right Speaker Output Mixer** 1xxx = Left DAC x1xx = Right DAC xx1x = Reserved xxx1 = Preoutput mixer 2
	2		
	1		
	0		

Speaker Output Volume

Table 24. Speaker Output Mixer Register

REGISTER	BIT	NAME	DESCRIPTION			
0x3B/0x3C	7	SPLM/SPRM	**Left/Right Speaker Output Mute** 0 = Disabled 1 = Enabled			
	4 3 2 1 0	SPVOLL/SPVOLR	**Left/Right Speaker Output Volume Level**			
			VALUE	**VOLUME (dB)**	**VALUE**	**VOLUME (dB)**
			0x00	-64	0x10	-10
			0x01	-59	0x11	-8
			0x02	-55	0x12	-6
			0x03	-50	0x13	-4
			0x04	-46	0x14	-2
			0x05	-42	0x15	0
			0x06	-38	0x16	+1
			0x07	-35	0x17	+2
			0x08	-32	0x18	+3
			0x09	-29	0x19	+4
			0x0A	-26	0x1A	+5
			0x0B	-23	0x1B	+6
			0x0C	-20	0x1C	+6.5
			0x0D	-17	0x1D	+7
			0x0E	-14	0x1E	+7.5
			0x0F	-12	0x1F	+8

Speaker Amplifier Signal Processing

The IC includes signal processing to improve the sound quality of the speaker output and protect transducers from damage. An excursion limiter dynamically adjusts the highpass corner frequency, while a power limiter and distortion limiter prevent the amplifier from outputting too much distortion or power. The excursion limiter is located in the DSP while the distortion limiter and power limiter control the analog volume control (Figure 28). All three limiters analyze the speaker amplifier's output signal to determine when to take action.

Excursion Limiter

The excursion limiter is a dynamic highpass filter that monitors the speaker outputs and increases the highpass corner frequency when the speaker amplifier's output exceeds a predefined threshold. The filter smoothly transitions between the high and low corner frequency to prevent unwanted artifacts. The filter can operate in four different modes:

- **Fixed Frequency Preset Mode.** The highpass corner frequency is fixed at the upper corner frequency and does not change with signal level.
- **Fixed Frequency Programmable Mode.** The highpass corner frequency is fixed to that specified by the programmable biquad filter.
- **Preset Dynamic Mode.** The highpass filter automatically slides between a preset upper and lower corner frequency based on output signal level.
- **User Programmable Dynamic Mode.** The highpass filter slides between a user-programmed biquad filter on the low side to a predefined corner frequency on the high side.

The transfer function for the user-programmable biquad is:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

The coefficients b_0, b_1, b_2, a_1, and a_2 are sample rate dependent and stored in registers 0xB4 through 0xC7. Store b_0, b_1, and b_2 as positive numbers. Store a_1 and a_2 as negated two's complement numbers. Separate filters can be stored for the DAI1 and DAI2 playback paths.

The MAX9888 EV kit software includes a graphic interface for generating the user-programmable biquad coefficients.

Note: Only change the excursion limiter settings when the signal path is disabled to prevent undesired artifacts.

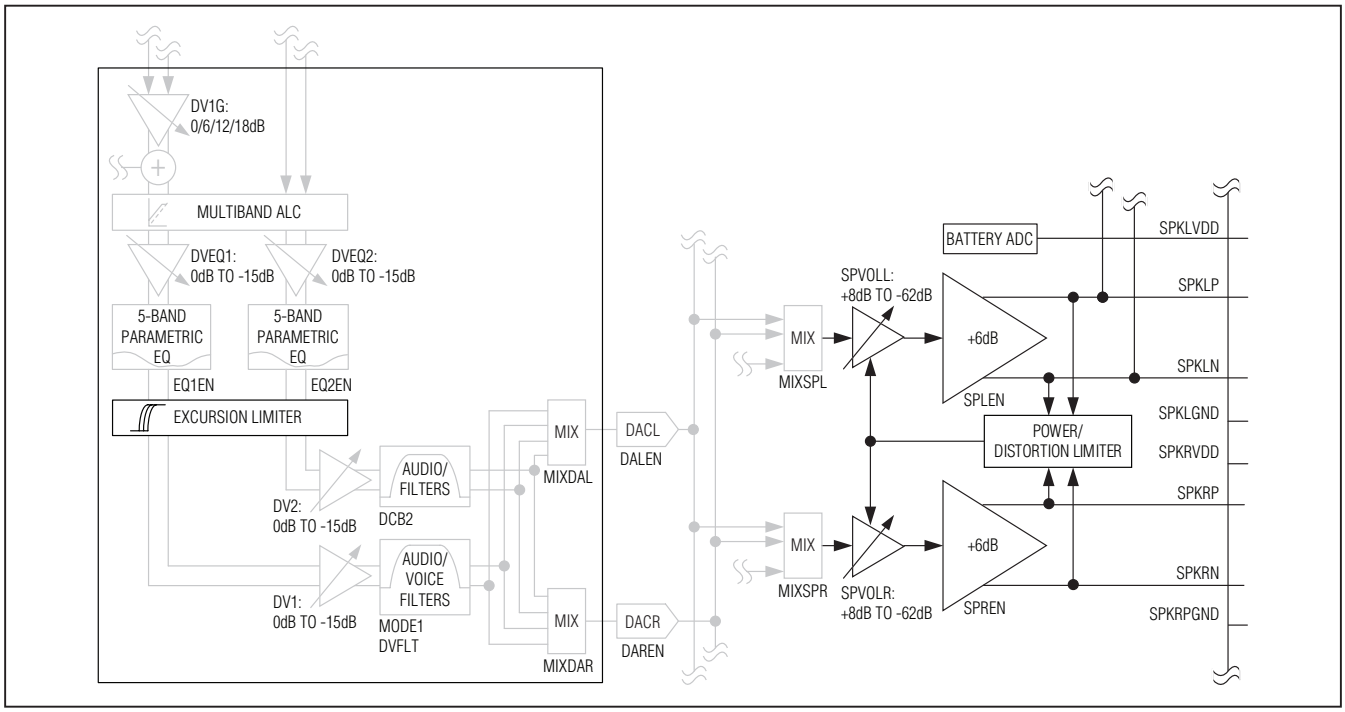


Figure 28. Speaker Amplifier Signal Processing Block Diagram

Table 25. Excursion Limiter Registers

REGISTER	BIT	NAME	DESCRIPTION				
0x3F	6	DHPUCF	**Excursion Limiter Corner Frequency** The excursion limiter has limited sliding range and minimum corner frequencies. Listed below are all the valid filter combinations.				
	5		**LOWER CORNER FREQUENCY**	**UPPER CORNER FREQUENCY**	**MINIMUM BIQUAD CORNER FREQUENCY**	**DHPUCF**	**DHPLCF**
			Excursion limiter disabled		—	000	00
	4		400Hz		—	001	00
			600Hz		—	010	00
			800Hz		—	011	00
			1kHz		—	100	00
	1	DHPLCF	Programmable using biquad		100Hz	000	11
			200Hz	400Hz	—	001	01
			400Hz	600Hz	—	010	10
			400Hz	800Hz	—	011	10
			Programmable using biquad	400Hz	200Hz	001	11
	0		Programmable using biquad	600Hz	300Hz	010	11
			Programmable using biquad	800Hz	400Hz	011	11
			Programmable using biquad	1kHz	500Hz	100	11
0x41	6	ALCRLS	**ALC and Excursion Limiter Release Time** Sets the release time for both the ALC and Excursion Limiter. See the *Automatic Level Control* section for ALC release times. Excursion limiter release time is defined as the time required to slide from the high corner frequency to the low corner frequency.				
	5		**VALUE**		**EXCURSION LIMITER RELEASE TIME (s)**		
			000		4		
			001		2		
			010		1		
			011		0.5		
	4		100		0.25		
			101		0.25		
			110		Reserved		
			111		Reserved		
0x40	3	DHPTH	**Excursion Limiter Threshold** Measured at the Class D speaker amplifier outputs. Signals above the threshold use the upper corner frequency. Signals below the threshold use the lower corner frequency. **V_{BAT} must correctly reflect the voltage of SPKLVDD to achieve accurate thresholds.** 000 = 0.34V_P 001 = 0.71V_P 010 = 1.30V_P 011 = 1.77V_P 100 = 2.33V_P 101 = 3.25V_P 110 = 4.25V_P 111 = 4.95V_P				
	2						
	1						
	0						

Power Limiter

The IC's power limiter tracks the RMS power delivered to the loudspeaker and briefly mutes the speaker amplifier output if the speaker is at risk of sustaining permanent damage.

Loudspeakers are typically damaged when the voice coil overheats due to extended operation above the rated power. During normal operation, heat generated in the voice coil is transferred to the speaker's magnet, which transfers heat to the surrounding air. For the voice coil to overheat, both the voice coil and the magnet must overheat. The result is that a loudspeaker can operate above its rated power for a significant time before it heats sufficiently to cause damage.

The IC's power limiter includes user-programmable time constants and power thresholds to match a wide range of loudspeakers. Program the power limiter's threshold to match the loudspeaker's rated power handling. This can be determined through measurement or the loudspeaker's specification. Program time constant 1 to match the voice coil's thermal time constant. Program time constant 2 to match the magnet's thermal time constant. The time constants can be determined by plotting the voice coil's resistance vs. time as power is applied to the speaker.

Table 26. Power Limiter Registers

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="20">0x42</td><td>7</td><td rowspan="10">PWRTH</td><td colspan="4">Power Limiter Threshold
If the RMS output power from the speaker amplifiers exceeds this threshold, the output is briefly muted to protect the speaker. The threshold is measured in watts assuming an 8Ω load. VBAT must correctly reflect the voltage of SPKLVDD/SPKRVDD to achieve accurate thresholds.</td></tr>
<tr><td rowspan="2">6</td><td>VALUE</td><td>THRESHOLD (W)</td><td>VALUE</td><td>THRESHOLD (W)</td></tr>
<tr><td>0x0</td><td>Power limiter disabled</td><td>0x8</td><td>0.27</td></tr>
<tr><td rowspan="4">5</td><td>0x1</td><td>0.05</td><td>0x9</td><td>0.35</td></tr>
<tr><td>0x2</td><td>0.06</td><td>0xA</td><td>0.48</td></tr>
<tr><td>0x3</td><td>0.09</td><td>0xB</td><td>0.72</td></tr>
<tr><td>0x4</td><td>0.11</td><td>0xC</td><td>1.00</td></tr>
<tr><td rowspan="4">4</td><td>0x5</td><td>0.13</td><td>0xD</td><td>1.43</td></tr>
<tr><td>0x6</td><td>0.18</td><td>0xE</td><td>1.57</td></tr>
<tr><td>0x7</td><td>0.22</td><td>0xF</td><td>1.80</td></tr>
<tr><td>2</td><td rowspan="10">PWRK</td><td colspan="4">Power Limiter Weighting Factor
Determines the balance between time constant 1 and 2 to match the dominance of each time constant in the loudspeaker.</td></tr>
<tr><td rowspan="4">1</td><td>VALUE</td><td colspan="2">T1 (%)</td><td>T2 (%)</td></tr>
<tr><td>000</td><td colspan="2">50</td><td>50</td></tr>
<tr><td>001</td><td colspan="2">62.5</td><td>37.5</td></tr>
<tr><td>010</td><td colspan="2">75</td><td>25</td></tr>
<tr><td>011</td><td colspan="2">87.5</td><td>12.5</td></tr>
<tr><td rowspan="4">0</td><td>100</td><td colspan="2">100</td><td>0</td></tr>
<tr><td>101</td><td colspan="2">12.5</td><td>87.5</td></tr>
<tr><td>110</td><td colspan="2">25</td><td>75</td></tr>
<tr><td>111</td><td colspan="2">37.5</td><td>62.5</td></tr>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
</table>

Table 26. Power Limiter Registers (continued)

0x43	7	PWRT2	**Power Limiter Time Constant 2** Select a value that matches the thermal time constant of the loudspeaker's magnet.			
	6		**VALUE**	**TIME CONSTANT (min)**	**VALUE**	**TIME CONSTANT (min)**
			0x0	Disabled	0x8	3.75
			0x1	0.50	0x9	5.00
	5		0x2	0.67	0xA	6.66
			0x3	0.89	0xB	8.88
			0x4	1.19	0xC	Reserved
	4		0x5	1.58	0xD	Reserved
			0x6	2.11	0xE	Reserved
			0x7	2.81	0xF	Reserved
	3	PWRT1	**Power Limiter Time Constant 1** Select a value that matches the thermal time constant of the loudspeaker's voice coil.			
	2		**VALUE**	**TIME CONSTANT (s)**	**VALUE**	**TIME CONSTANT (s)**
			0x0	Disabled	0x8	3.75
			0x1	0.50	0x9	5.00
	1		0x2	0.67	0xA	6.66
			0x3	0.89	0xB	8.88
			0x4	1.19	0xC	Reserved
	0		0x5	1.58	0xD	Reserved
			0x6	2.11	0xE	Reserved
			0x7	2.81	0xF	Reserved

Distortion Limiter

The IC's distortion limiter ensures that the speaker amplifier's output does not exceed the programmed THD+N limit. The distortion limiter analyzes the Class D output duty cycle to determine the percentage of the waveform that is clipped. If the distortion exceeds the programmed threshold, the output gain is reduced.

Table 27. Distortion Limiter Registers

REGISTER	BIT	NAME	DESCRIPTION			
0x44	7	THDCLP	**Distortion Limit** Measured in % THD+N.			
	6		**VALUE**	**THD+N LIMIT (%)**	**VALUE**	**THD+N LIMIT (%)**
	5		0x0	Limiter disabled	0x8	12
			0x1	< 1	0x9	14
			0x2	1	0xA	16
			0x3	2	0xB	18
	4		0x4	4	0xC	20
			0x5	6	0xD	21
			0x6	8	0xE	22
			0x7	10	0xF	24
	2	THDT1	**Distortion Limiter Release Time Constant** Duration of time required for the speaker amplifier's output gain to adjust back to the nominal level after a large signal has passed. 000 = 6.2s 001 = 3.1s 010 = 1.6s 011 = 815ms 100 = 419ms 101 = 223ms 110 = 116ms 111 = 76ms			
	1					
	0					

Headphone Amplifier

The IC's headphone amplifier integrates Maxim's DirectDrive architecture to eliminate the need for large DC-blocking capacitors. Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and headphone amplifier.

The DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the IC's headphone outputs to be biased at GND while operating from a single supply (Figure 29). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) capacitors, the IC charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the offset of the IC is typically ±0.2mV, which, when combined with a 32Ω load, results in less than 6µA of DC current flow to the headphones.

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. The DC-blocking capacitor not only blocks DC, but also low-frequency audio. Improving the low-frequency response of a conventional headphone amplifier requires increasing the capacitor size, further adding to the cost and size of the solution. Due to the voltage coefficient of the capacitors used for DC blocking, they introduce significant distortion near the corner frequency of the highpass filter they create. This distortion further degrades the low-frequency audio quality.

Stereo Audio CODEC with FlexSound Technology

Alternative approaches to eliminating the output-coupling capacitors involve biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises some issues:

- The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
- During an ESD strike, the amplifier's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full energy from an ESD strike.
- When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

The IC features a low-noise charge pump to generate a negative supply for the headphone amplifier. The nominal switching frequency is well beyond the audio range, and thus does not interfere with audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic trace inductance is minimized. The charge pump is active only in headphone modes.

To reduce audible noise at the outputs, the IC's headphone amplifier includes headphone ground sensing. Connect the sense line (HPSNS) to the ground terminal of the device's headphone jack. Any noise present at the headphone ground is then added to the headphone output. The result is elimination of this noise from the audible output. If ground sensing is not required, connect HPSNS directly to ground. Figure 30 shows a block diagram of the headphone output section including the headphone sense function.

Headphone Output Mixers

The IC's headphone amplifier accepts input from the stereo DAC and the line inputs. The output of the left and right DAC cannot be mixed at the headphone mixer. Use MIXDAL/MIXDAR to mix the left and right audio channels before conversion.

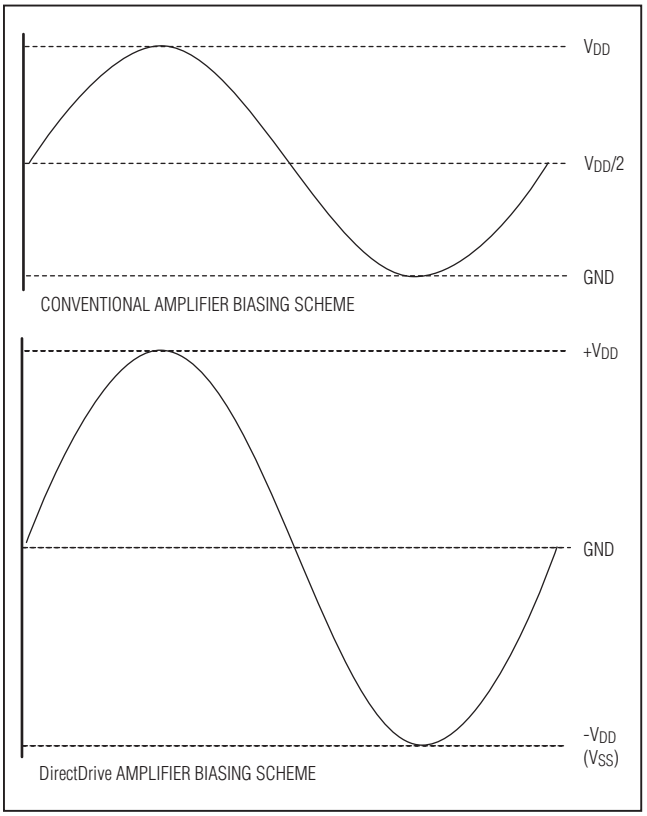


Figure 29. Traditional Amplifier Output vs. DirectDrive Output

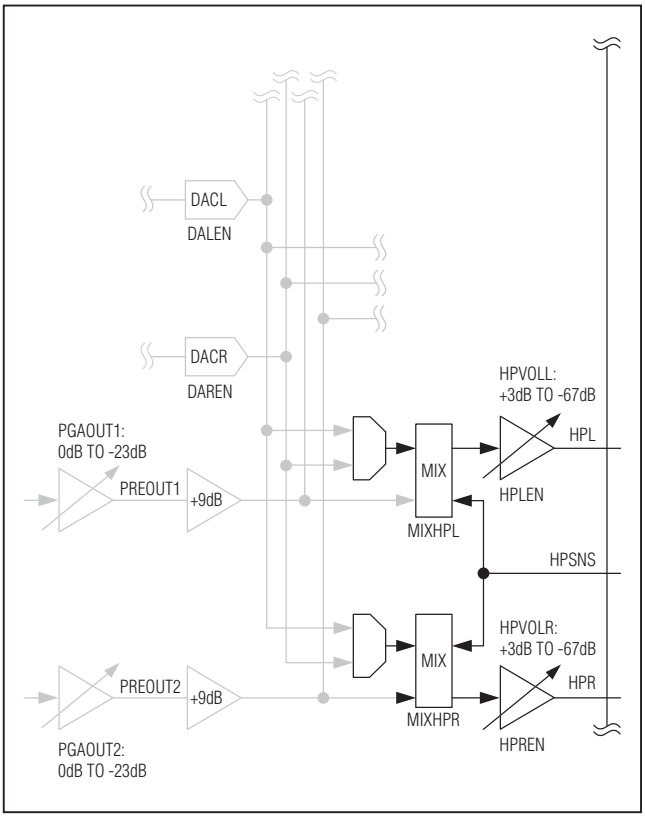


Figure 30. Headphone Amplifier Block Diagram

Table 28. Headphone Output Mixer Register

REGISTER	BIT	NAME	DESCRIPTION
0x27	7	MIXHPL	**Left Headphone Output Mixer** 10xx = Left DAC 01xx = Right DAC (requires DALEN = 0 for proper operation) 11xx = Left DAC xx1x = Reserved xxx1 = Preoutput mixer 1
	6		
	5		
	4		
	3	MIXHPR	**Right Headphone Output Mixer** 10xx = Left DAC (requires DAREN = 0 for proper operation) 01xx = Right DAC 11xx = Right DAC xx1x = Reserved xxx1 = Preoutput mixer 2
	2		
	1		
	0		

Headphone Output Volume

Table 29. Headphone Output Level Register

REGISTER	BIT	NAME	DESCRIPTION			
0x38/0x39	7	HPLM/HPRM	**Headphone Output Mute** 0 = Disabled 1 = Enabled			
	4 3 2 1 0	HPVOLL/HPVOLR	**Left/Right Headphone Output Volume Level**			
			VALUE	**VOLUME (dB)**	**VALUE**	**VOLUME (dB)**
			0x00	-67	0x10	-15
			0x01	-63	0x11	-13
			0x02	-59	0x12	-11
			0x03	-55	0x13	-9
			0x04	-51	0x14	-7
			0x05	-47	0x15	-5
			0x06	-43	0x16	-4
			0x07	-40	0x17	-3
			0x08	-37	0x18	-2
			0x09	-34	0x19	-1
			0x0A	-31	0x1A	0
			0x0B	-28	0x1B	+1
			0x0C	-25	0x1C	+1.5
			0x0D	-22	0x1D	+2
			0x0E	-19	0x1E	+2.5
			0x0F	-17	0x1F	+3

Stereo Audio CODEC with FlexSound Technology

Output Bypass Switches

The IC includes two output bypass switches that solve common applications problems. When a single transducer is used for the loudspeaker and receiver, the need exists for two amplifiers to power the same transducer. Bypass switches connect the IC's receiver amplifier output to the speaker amplifier's output, allowing either amplifier to power the same transducer. In systems where an external receiver amplifier is used, route its output to the left speaker through RECP/RXINP and RECN/RXINN, bypassing the Class D amplifier. In systems where an external amplifier drives both the receiver and the IC's line input, one of the differential signals can be disconnected from the receiver when not needed by passing it through the analog switch that connects RECP/RXINP to RECN/RXINN.

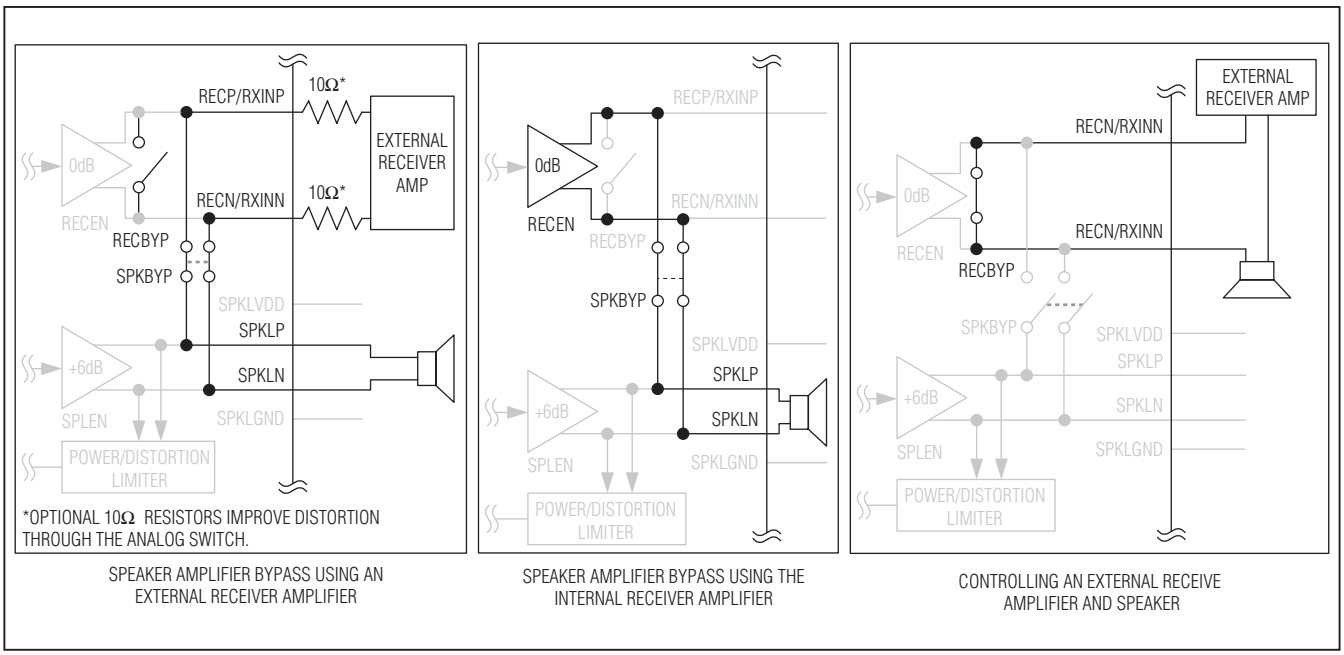


Figure 31. Output Bypass Switch Block Diagrams

Table 30. Output Bypass Switches Register

REGISTER	BIT	NAME	DESCRIPTION
0x48	7	INABYP	See the *Microphone Inputs* section.
	4	MIC2BYP	
	1	RECBYP	**RXINP to RXINN Bypass Switch** Shorts RXINP to RXINN allowing a signal to pass through the MAX9888. Disable the receiver amplifier when RECBYP = 1. 0 = Disabled 1 = Enabled
	0	SPKBYP	**RXIN to SPKL Bypass Switch** Shorts RXINP/RXINN to SPKLP/SPKLN allowing either the internal or an external receiver amplifier to power the left speaker. Disable the left speaker amplifier when SPKBYP = 1. 0 = Disabled 1 = Enabled

Click-and-Pop Reduction

The IC includes extensive click-and-pop reduction circuitry. The circuitry minimizes clicks and pops at turn-on, turn-off, and during volume changes.

Zero-crossing detection is implemented on all analog PGAs and volume controls to prevent large glitches when volume changes are made. Instead of making a volume change immediately, the change is made when the audio signal crosses the midpoint. If no zero-crossing occurs within the timeout window, the change is forced.

Volume slewing breaks up large volume changes into the smallest available step size and the steps through each step between the initial and final volume setting. When enabled, volume slewing also occurs at device turn-on and turn-off. During turn-on the volume is set to mute before the output is enabled. Once the output is on, the volume ramps to the desired level. At turn-off the volume is ramped to mute before the outputs are disabled.

When there is no audio signal zero-crossing detection can prevent volume slewing from occurring. Enable enhanced volume slewing to prevent the volume controller from requesting another volume level until the previous one has been set. Each step in the volume ramp then occurs after a zero crossing has occurred in the audio signal or the timeout window has expired. During turn-off, enhance volume slewing is always disabled.

Table 31. Click-and-Pop Reduction Register

REGISTER	BIT	NAME	DESCRIPTION
0x49	7	$\overline{VS2EN}$	**Enhanced Volume Smoothing** During volume slewing, the controller waits for each step in the ramp to be applied before sending the next step. When zero-crossing detection is enabled this prevents large steps in the output volume when no zero crossings are detected. 0 = Enabled 1 = Disabled Applies to volume changes in HPVOLL, HPVOLR, RECVOL, SPVOLL, and SPVOLR.
	6	$\overline{VSEN}$	**Volume Adjustment Smoothing** Volume changes are smoothed by stepping through intermediate steps. Also ramps the volume from minimum to the programmed value at turn-on and back to minimum at turn-off. 0 = Enabled 1 = Disabled Applies to volume changes in HPVOLL, HPVOLR, RECVOL, SPVOLL, and SPVOLR.
	5	$\overline{ZDEN}$	**Zero-Crossing Detection** Holds volume changes until there is a zero crossing in the audio signal. This reduces click and pop during volume changes (zipper noise). If no zero crossing is detected within 100ms, the volume change is forced. 0 = Enabled 1 = Disabled Applies to volume changes in PGAM1, PGAM2, PGAOUTA, PGAOUTB, PGAOUTC, HPVOLL, HPVOLR, RECVOL, SPVOLL, and SPVOLR.
	1	EQ2EN	See the *5-Band Parametric EQ* section.
	0	EQ1EN	

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Jack Detection

The IC features jack detection that can detect the insertion and removal of a jack as well as the load type. When a jack is detected, an interrupt on $\overline{IRQ}$ can be triggered to alert the microcontroller of the event. Figure 32 shows the typical configuration for jack detection.

Jack Insertion

To detect a jack insertion, the IC must have a power supply and MICBIAS should be disabled. Set JDETEN to enable jack detection circuitry and apply a pullup current to JACKSNS. Set JDWK to minimize supply current. Clear JDWK to differentiate between headsets with a microphone and headphones without a microphone. The voltage on JACKSNS is equal to SPKLVDD as long as no load is applied to JACKSNS. Table 32 shows the change in JKSNS that occurs when a jack is inserted.

Accessory Button Detection

After jack insertion, the MAX9888 can detect button presses on accessories that include a microphone and a switch that shorts the microphone signal to ground. Set JDETEN to enable jack detection circuitry. A pullup current is automatically applied to JACKSNS if MICBIAS is disabled. Clear JDWK to allow differentiation between the microphone load and a short to ground. Button presses can be detected both when MICBIAS is enabled and disabled. Table 33 shows the change in JKSNS that occurs when the accessory button is pressed.

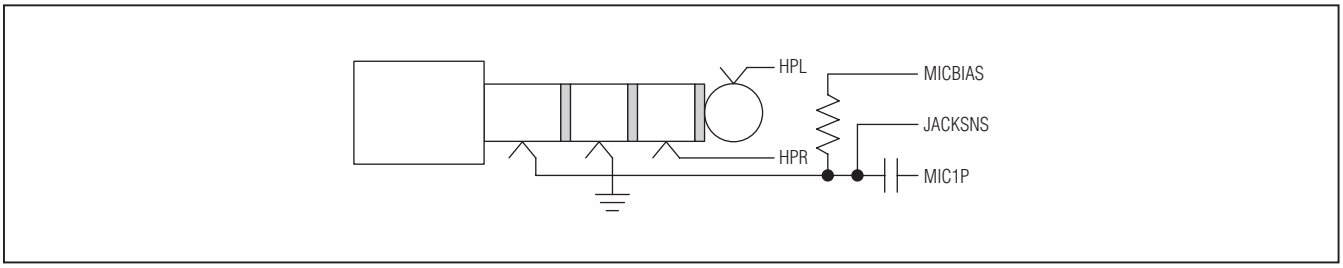


Figure 32. Typical Configuration for Jack Detection

Table 32. Change in JKSNS Upon Jack Insertion

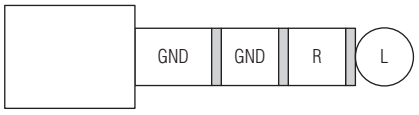
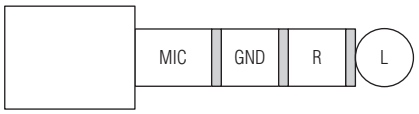
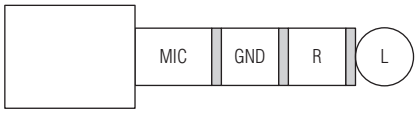
JACK TYPE	JDWK = 1	JDWK = 0
	JKSNS: 11 → 00	JKSNS: 11 → 00
	JKSNS: 11 → 00	JKSNS: 11 → 01

Table 33. Change in JKSNS Upon Button Press

JACK TYPE	MICBIAS ENABLED OR DISABLED
	JKSNS: 01 → 00

Jack Removal

The IC detects jack removal by monitoring JACKSNS for transitions to the 11 state. Set JDETEN to enable jack detection circuitry. A pullup current is automatically applied to JACKSNS if MICBIAS is disabled. Set JDWK to minimize supply current if button detection is not required. Table 34 shows the change in JKSNS that occurs when a jack is removed.

Table 34. Change in JKSNS Upon Jack Removal

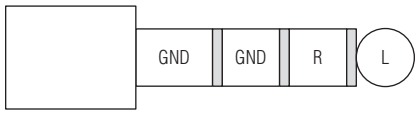
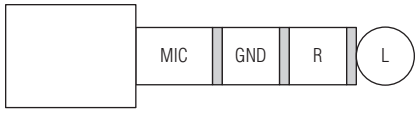
JACK TYPE	JDWK = 1 AND MICBIAS DISABLED	JDWK = 0 OR MICBIAS ENABLED
	JKSNS: 00 ➔ 11	JKSNS: 00 ➔ 11
	JKSNS: 00 ➔ 11	JKSNS: 01 ➔ 11

Table 35. Jack Detection Registers

REGISTER	BIT	NAME	DESCRIPTION
0x02 (Read Only)	7, 6	JKSNS	**JACKSNS State** Reports the status of JACKSNS when JDETEN = 1.

VALUE	MODE	DESCRIPTION
00	MBEN = 1	$\mathbf{V_{JACKSNS}}$ < 0.1 x $V_{MICBIAS}$
	MBEN = 0	$\mathbf{V_{JACKSNS}}$ < 0.1 x $V_{SPKLVDD}$
01	MBEN = 1	0.1 x $V_{MICBIAS}$ < $\mathbf{V_{JACKSNS}}$ < 0.95 x $V_{MICBIAS}$
	MBEN = 0	0.1 x $V_{SPKLVDD}$ < $\mathbf{V_{JACKSNS}}$ < 0.95 x $V_{SPKLVDD}$
10	MBEN = 1	Reserved
	MBEN = 0	Reserved
11	MBEN = 1	0.95 x $V_{MICBIAS}$ < $\mathbf{V_{JACKSNS}}$
	MBEN = 0	0.95 x $V_{SPKLVDD}$ < $\mathbf{V_{JACKSNS}}$

REGISTER	BIT	NAME	DESCRIPTION
0x49	7	JDETEN	**Jack Detection Enable** 0 = Disabled 1 = Enabled
	1, 0	JDEB	**Jack Detection Debounce** Configures the debounce time for setting JDET. 00 = 25ms 01 = 50ms 10 = 100ms 11 = 200ms
0x4C	7	$\overline{SHDN}$	See the *Power Management* section.
	6	VBATEN	See the *Battery Measurement* section.
	1	JDWK	**JACKSNS Pullup** When JDWK = 1 JACKSNS is slow to increase in voltage. Set JDWK = 0 before setting JDETEN = 1 to prevent false detection. Valid when MBIAS = 0 or $\overline{SHDN}$ = 0. 0 = 2.4kΩ to SPKLVDD (allows microphone detection) 1 = 5µA to SPKLVDD (minimizes supply current)

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Battery Measurement

The IC measures the voltage applied to SPKLVDD (typically the battery voltage) and reports the value in register 0x03. This value is also used by the speaker limiter circuitry to set accurate thresholds. When the battery measurement function is disabled, the battery voltage is user programmable.

Table 36. Battery Measurement Registers

REGISTER	BIT	NAME	DESCRIPTION
0x03	4	VBAT	**Battery Voltage** Read VBAT when V_{BATEN} = 1 to determine $V_{SPKLVDD}$. Program VBAT when V_{BATEN} = 0 to allow proper speaker amplifier signal processing. Calculate the battery voltage using the following formula: $V_{BATTERY}$ = 2.55V + [VBAT/10]
	3		
	2		
	1		
	0		
0x4C	7	$\overline{SHDN}$	See the *Power Management* section.
	6	VBATEN	**Battery Measurement Enable** Enables an internal ADC to measure $V_{SPKLVDD}$. 0 = Disabled (register 0x03 readable and writeable) 1 = Enabled (register 0x03 read only)
	1	JDWK	See the *Headset Detection* section.

Device Status

The IC uses register 0x00 and $\overline{IRQ}$ to report the status of various device functions. The status register bits are set when their respective events occur, and cleared upon reading the register. Device status can be determined either by poling register 0x00 or configuring the $\overline{IRQ}$ to pull low when specific events occur. $\overline{IRQ}$ is an open-drain output that requires a pullup resistor for proper operation. Register 0x0F determines which bits in the status register trigger $\overline{IRQ}$ to pull low.

Table 37. Status and Interrupt Registers

REGISTER	BIT	NAME	DESCRIPTION
0x00 (Read Only)	7	CLD	**Full Scale** 0 = All digital signals are less than full scale. 1 = The DAC or ADC signal path has reached or exceeded full scale. This typically indicates clipping.
	6	SLD	**Volume Slew Complete** SLD reports that any of the programmable-gain arrays or volume controllers has completed slewing from a previous setting to a new programmed setting. If multiple gain arrays or volume controllers are changed at the same time, the SLD flag is set after the last volume slew completes. SLD also reports when the digital audio interface soft-start or soft-stop process has completed. MCLK is required for proper SLD operation. 0 = No volume slewing sequences have completed since the status register was last read. 1 = Volume slewing complete.
	5	ULK	**Digital Audio Interface Unlocked** 0 = Both digital audio interfaces are operating normally. 1 = Either digital audio interface is configured incorrectly or receiving invalid data.
	1	JDET	**Jack Configuration Change** JDET reports changes to any bit in the Jack Status register (0x02). Changes to the Jack Status bits are debounced before setting JDET. The debounce period is programmable using the JDEB bits. JDET is always set the first time JDETEN or $\overline{SHDN}$ is set the first time power is applied to the IC. Read the status register following such an event to clear JDET and allow for proper jack detection. 0 = No change in jack configuration. 1 = Jack configuration has changed.
0x0F	7	ICLD	**Full-Scale Interrupt Enable** 0 = Disabled 1 = Enabled
	6	ISLD	**Volume Slew Complete Interrupt Enable** 0 = Disabled 1 = Enabled
	5	IULK	**Digital Audio Interface Unlocked Interrupt Enable** 0 = Disabled 1 = Enabled
	1	IJDET	**Jack Configuration Change Interrupt Enable** 0 = Disabled 1 = Enabled

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Device Revision

Table 38. Device Revision Register

REGISTER	BIT	NAME	DESCRIPTION
0xFF (Read Only)	7	REV	**Device Revision Code** REV is always set to 0x43.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

I²C Serial Interface

The IC features an I²C/SMBus™-compatible, 2-wire serial interface comprising a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. Figure 5 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 33). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

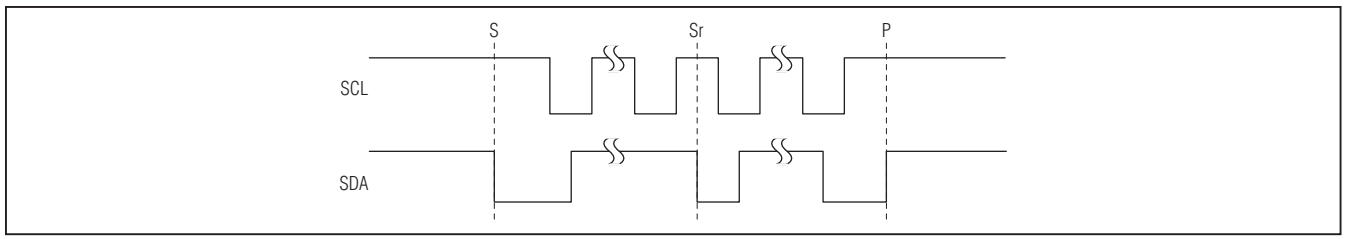

Figure 33. START, STOP, and REPEATED START Conditions

SMBus is a trademark of Intel Corp.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the IC, the seven most significant bits are 0010000. Setting the read/write bit to 1 (slave address = 0x21) configures the IC for read mode. Setting the read/write bit to 0 (slave address = 0x20) configures the IC for write mode. The address is the first byte of information sent to the IC after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt each byte of data when in write mode (Figure 34). The IC pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 35 illustrates the proper frame format for writing one byte of data to the IC. Figure 35 illustrates the frame format for writing n-bytes of data to the IC.

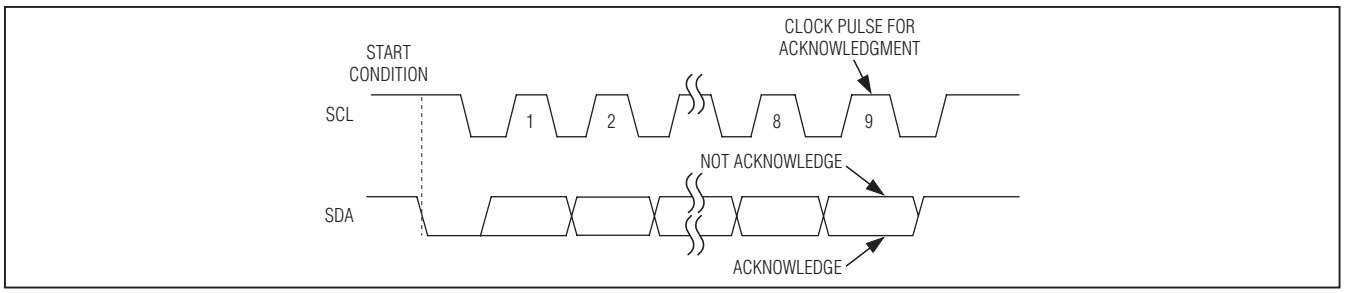

Figure 34. Acknowledge

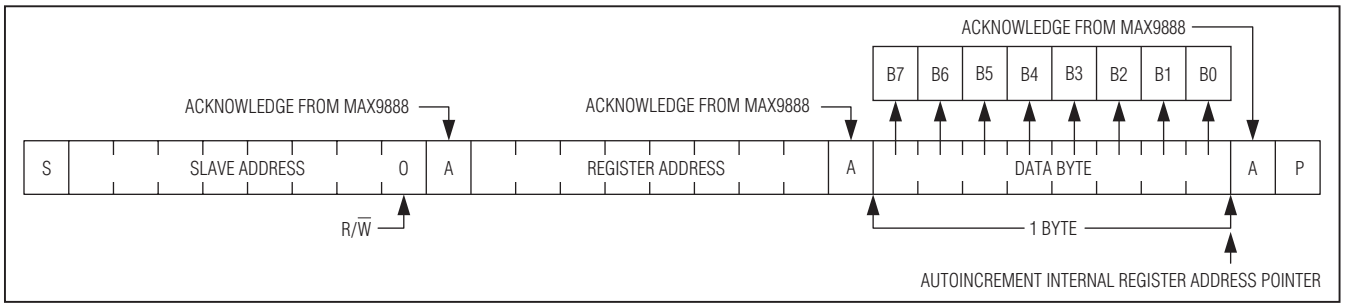

Figure 35. Writing One Byte of Data to the IC

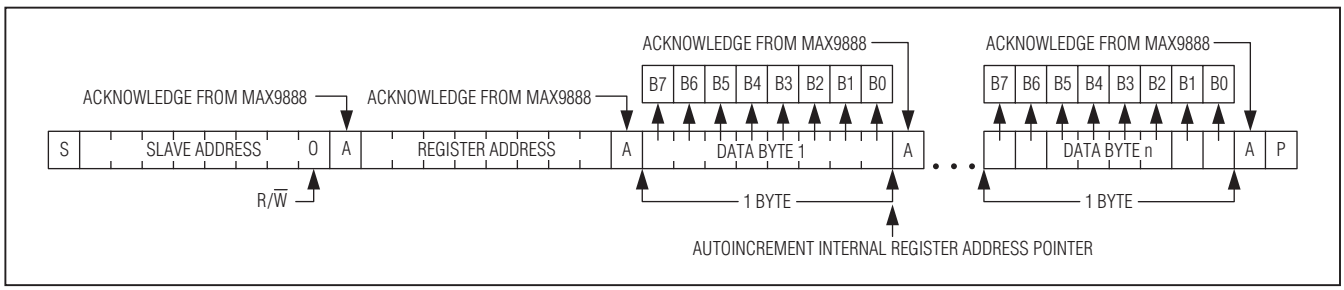

Figure 36. Writing n-Bytes of Data to the IC

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The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0xC7 are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the IC is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the IC's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The IC then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 37 illustrates the frame format for reading one byte from the IC. Figure 38 illustrates the frame format for reading multiple bytes from the IC.

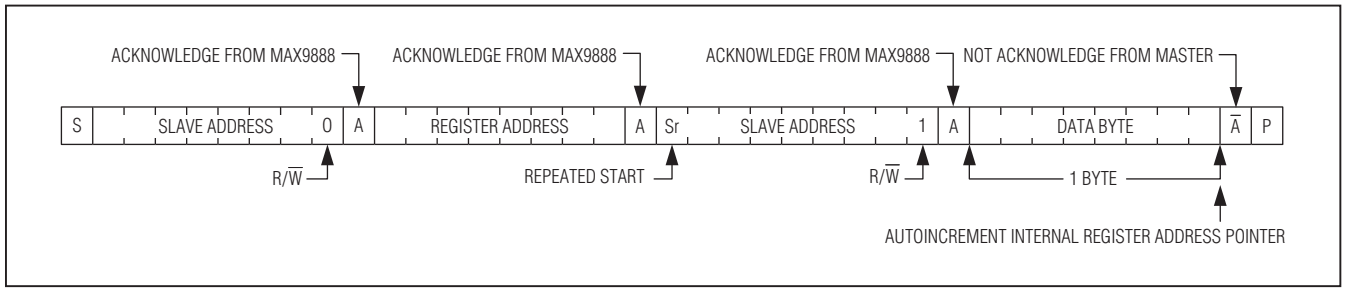

Figure 37. Reading One Byte of Data from the IC

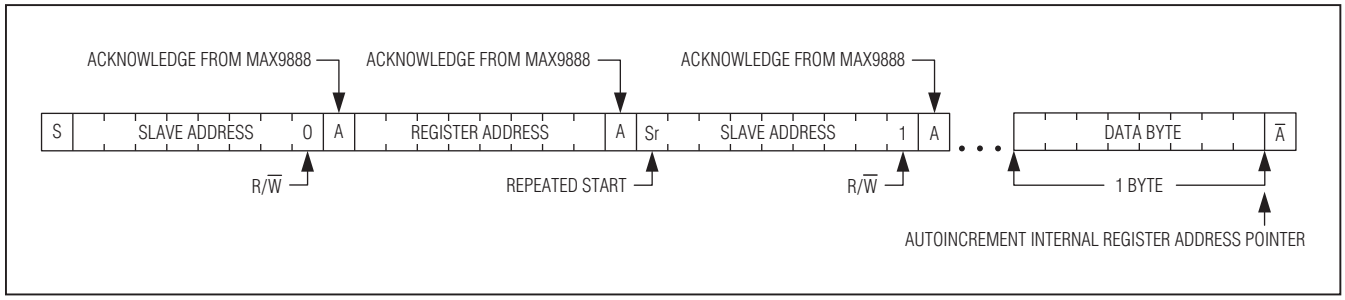

Figure 38. Reading n Bytes of Data from the IC

Applications Information

Typical Operating Circuits

Figures 39 and 40 provide example operating circuits for the IC. The external components shown are the minimum required for the IC to operate. Additional components may be required by the application.

Analog Microphones and Bypass Switch

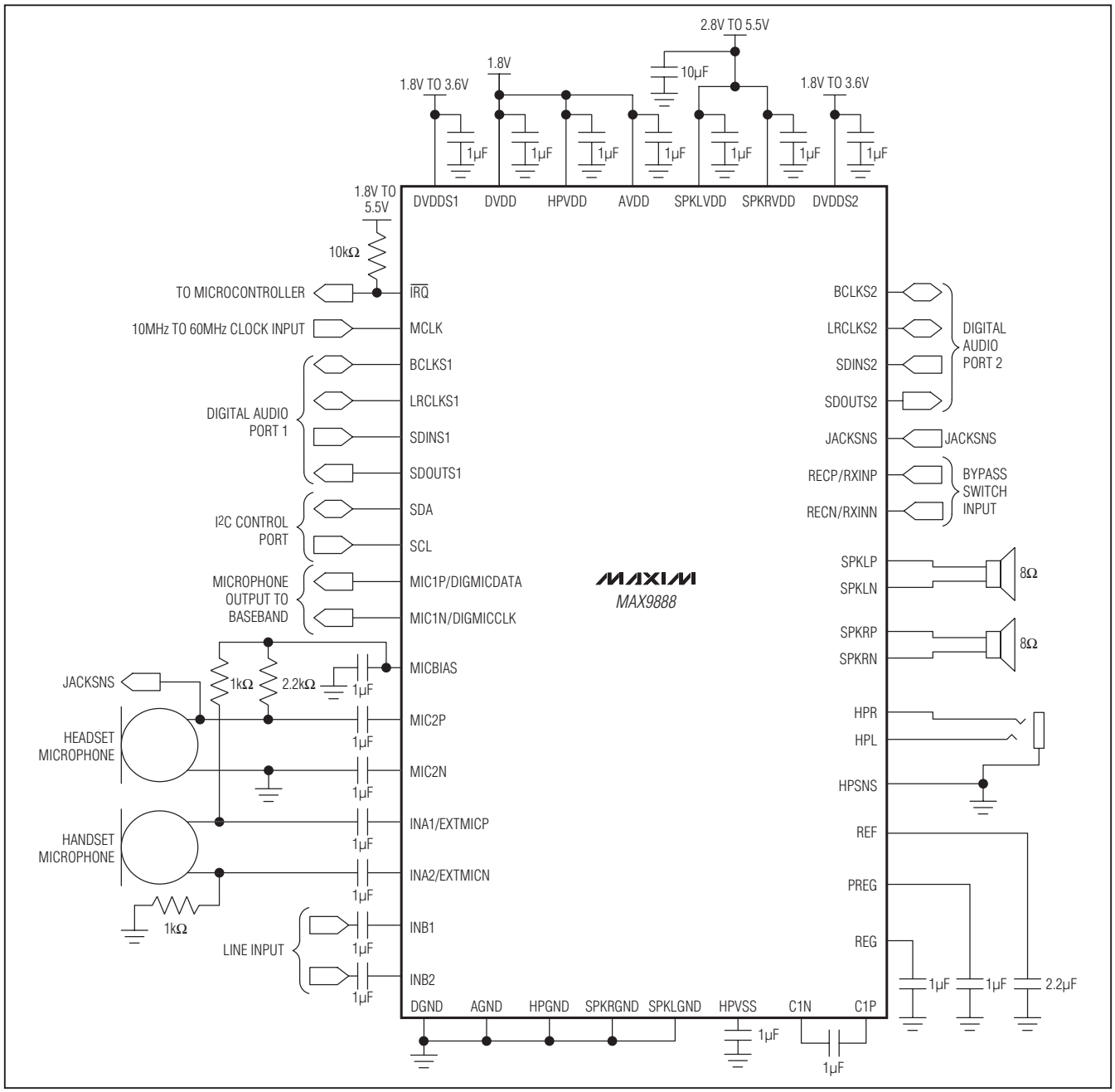

Figure 39. Typical Application Circuit Using Analog Microphone Inputs and the Bypass Switch

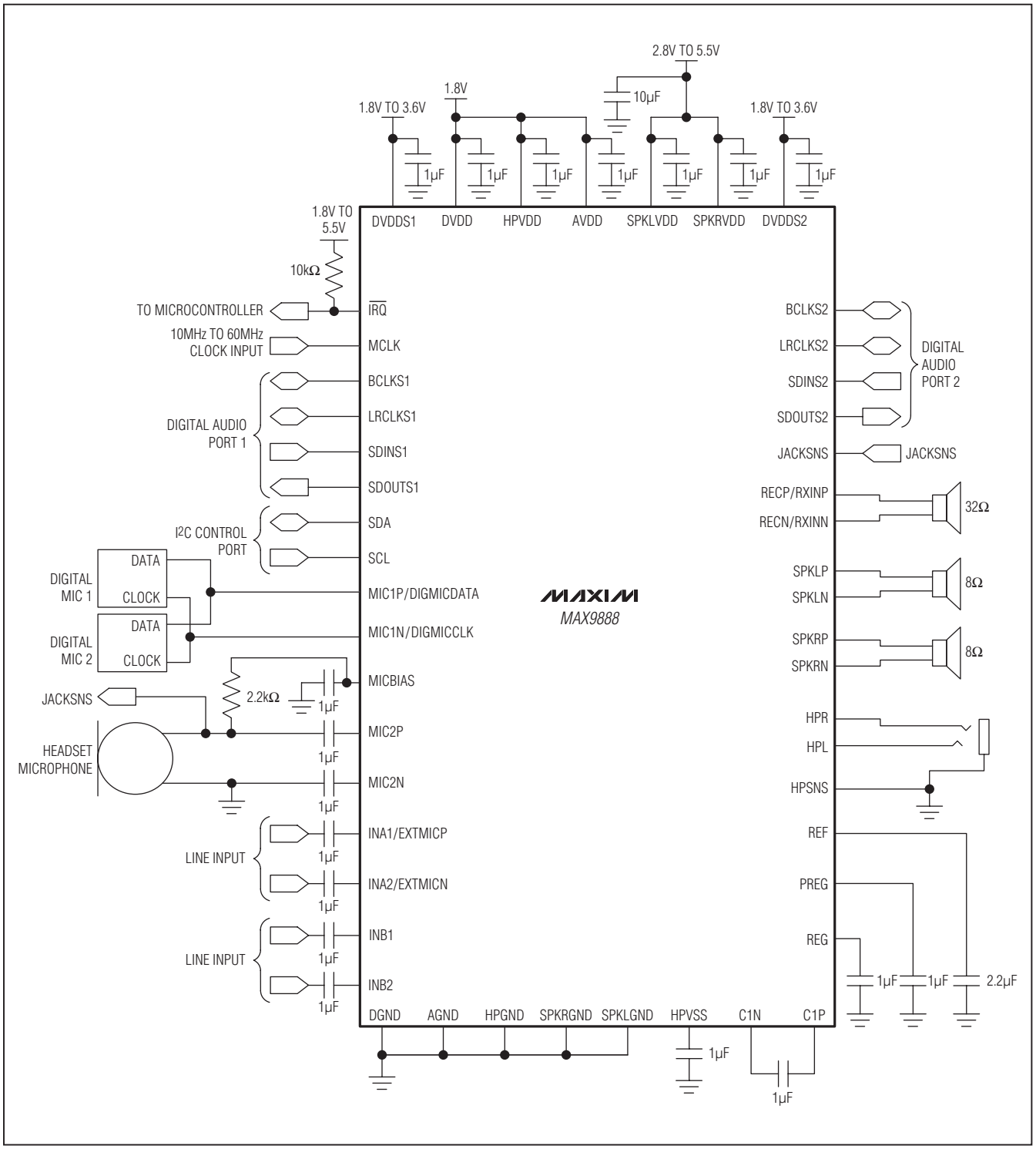

Figure 40. Typical Application Circuit Using the Digital Microphone Input and Receiver Amplifier

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (2 x V_{DD} peak to peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The IC does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Because the frequency of the IC output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers. The IC is designed specifically to reject RF signals; however, PCB layout has a large impact on the susceptibility of the end product.

In RF applications, improvements to both layout and component selection decrease the IC's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Trace lengths should be kept below 1/4 of the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the IC. The wavelength (λ) in meters is given by: $\lambda = c/f$ where $c = 3 \times 10^8$ m/s, and f = the RF frequency of interest.

Route audio signals on middle layers of the PCB to allow ground planes above and below to shield them from RF interference. Ideally, the top and bottom layers of the PCB should primarily be ground planes to create effective shielding.

Additional RF immunity can also be obtained by relying on the self-resonant frequency of capacitors as it exhibits a frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at the RF frequencies of interest. These capacitors, when placed at the input pins, can effectively shunt the RF noise to ground. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Avoid using microvias to connect to the ground plane whenever possible as these vias do not conduct well at RF frequencies.

Startup/Shutdown Sequencing

To ensure proper device initialization and minimal click-and-pop, program the IC's $\overline{SHDN}$ = 1 after configuring all registers. Table 39 lists an example startup sequence for the device. To shut down the IC, simply set $\overline{SHDN}$ = 0.

Table 39. Example Startup Sequence

SEQUENCE	DESCRIPTION	REGISTERS
1	Ensure $\overline{SHDN}$ = 0	0x4C
2	Configure clocks	0x10 to 0x13, 0x19 to 0x1B
3	Configure digital audio interface	0x14 to 0x17, 0x1C to 0x1F
4	Configure digital signal processing	0x18, 0x20, 0x3D to 0x44
5	Load coefficients	0x50 to 0xC7
6	Configure mixers	0x21 to 0x29
7	Configure gain and volume controls	0x2A to 0x3C
8	Configure miscellaneous functions	0x45 to 0x49
9	Enable desired functions	0x4A, 0x4B
10	Set $\overline{SHDN}$ = 1	0x4C

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While many configuration options in the IC can be made while the device is operating, some registers should only be adjusted when the corresponding audio path is disabled. Table 40 lists the registers that are sensitive during operation. Either disable the corresponding audio path or set $\overline{SHDN}$ = 0 while changing these registers.

Component Selection

Optional Ferrite Bead Filter

In applications where speaker leads exceed 20mm, additional EMI suppression can be achieved by using a filter constructed from a ferrite bead and a capacitor to ground (Figure 41). Use a ferrite bead with low DC resistance, high-frequency (> 600MHz) impedance between 100Ω and 600Ω, and rated for at least 1A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF based on EMI performance.

Input Capacitor

An input capacitor, C_{IN}, in conjunction with the input impedance of the IC line inputs forms a highpass filter that removes the DC bias from an incoming analog signal. The AC coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. For best audio quality use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface-mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Table 40. Registers That Are Sensitive to Changes During Operation

REGISTER	DESCRIPTION
0x10 to 0x13, 0x19 to 0x1B	Clock Control Registers
0x14 to 0x17, 0x1C to 0x1F	Digital Audio Interface Configuration
0x18, 0x20	Digital Passband Filters
0x24 to 0x29	Analog Mixers
0x50 to 0xC7	Digital Signal Processing Coefficients

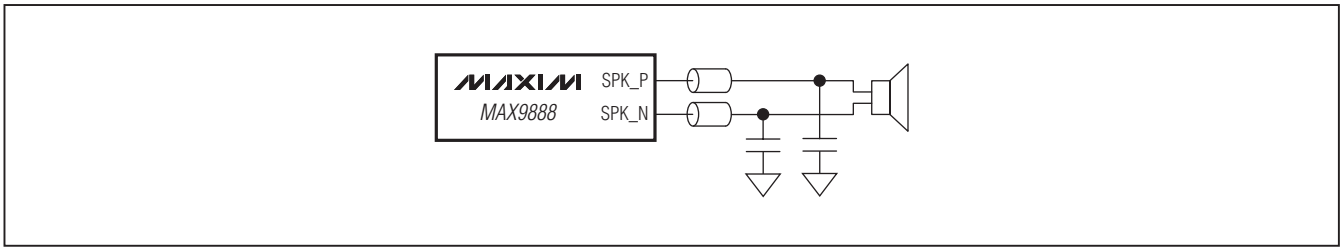

Figure 41. Optional Class D Ferrite Bead Filter

Charge-Pump Flying Capacitor

The value of the flying capacitor (connected between C1N and C1P) affects the output resistance of the charge pump. A value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of the flying capacitor reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the internal switches and the ESR of external charge-pump capacitors dominate.

Charge-Pump Holding Capacitor

The holding capacitor (bypassing HPVSS) value and ESR directly affect the ripple at HPVSS. Increasing the capacitor's value reduces output ripple. Likewise, decreasing the ESR reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* section for more information

Unused Pins

Table 41 shows how to connect the IC's pins when unused.

Table 41. Unused Pins

NAME	CONNECTION	NAME	CONNECTION
SPKRP	Unconnected	INB1	Unconnected
SPKRVDD	Always connected	INA2/MICEXTN	Unconnected
SPKLVDD	Always connect	LRCLKS2	Unconnected
SPKLP	Unconnected	MCLK	Always connect
RECN/RXINN	Unconnected	SDINS2	AGND
HPVDD	Always connect	$\overline{IRQ}$	Unconnected
C1P	Unconnected	MIC1P/DIGMICDATA	Unconnected
HPGND	AGND	INA1/MICEXTP	Unconnected
SPKRN	Unconnected	DGND	Always connect
SPKRGND	Always connect	BCLKS2	Unconnected
SPKLGND	Always connect	SDA	Always connect
SPKLN	Unconnected	SCL	Always connect
RECP/RXINP	Unconnected	REG	Always connect
C1N	Unconnected	REF	Always connect
HPL	Unconnected	MIC1N/DIGMICCLK	Unconnected
HPVSS	Unconnected	MIC2P	Unconnected
SDINS1	AGND	SDOUTS2	Unconnected
LRCLKS1	Unconnected	DVDDS2	DVDD
HPSNS	AGND	DVDD	Always connect
INB2	Unconnected	AVDD	Always connect
HPR	Unconnected	PREG	Always connect
DVDDS1	DVDD	AGND	Always connect
SDOUTS1	Unconnected	MICBIAS	Unconnected
BCLKS1	Unconnected	MIC2N	Unconnected
JACKSNS	Unconnected		

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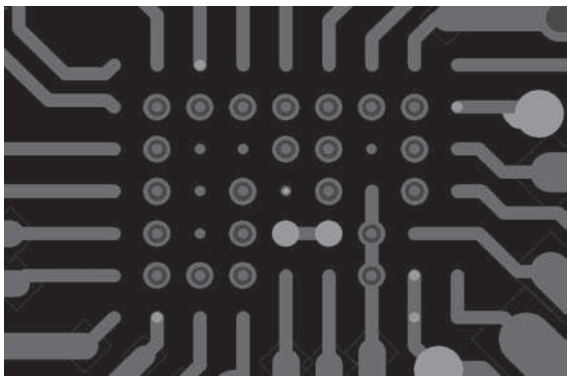
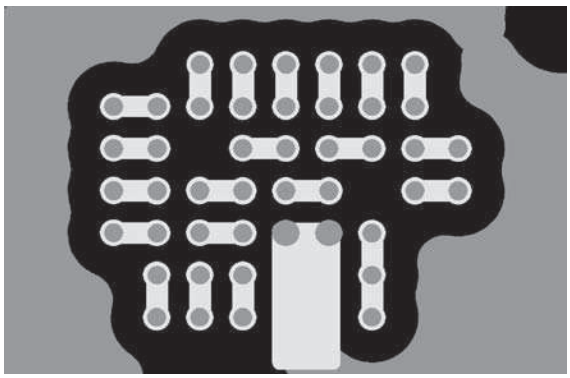
Recommended PCB Routing

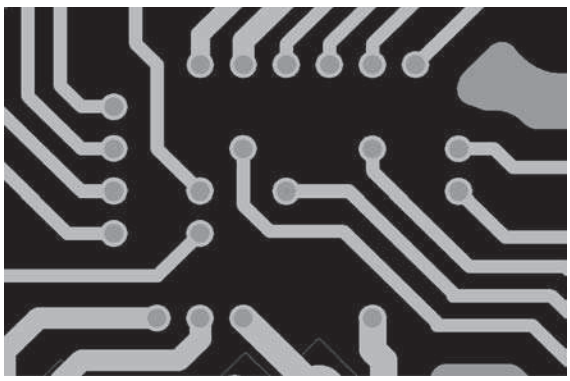
The IC uses a 63-bump WLP package. Figure 42 provides an example of how to connect to all active bumps using 3 layers of the PCB. To ensure uninterrupted ground returns, use layer 2 as a connecting layer between layer 1 and layer 2 and flood the remaining area with ground.



LAYER 1



LAYER 2



LAYER 3

Figure 42. Suggested Routing

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. When designing a PCB for the IC, partition the circuitry so that the analog sections of the IC are separated from the digital sections. This ensures that the analog audio traces are not routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND, DGND, HPGND, SPKLGND, and SPKRGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Ground the bypass capacitors on MICBIAS, REG, PREG, and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND. Bypass AVDD directly to AGND.

Connect all digital I/O termination to the ground plane with minimum path length to DGND. Bypass DVDD, DVDDS1, and DVDDS2 directly to DGND.

Place the capacitor between C1P and C1N as close as possible to the IC to minimize trace length from C1P to C1N. Inductance and resistance added between C1P and C1N reduce the output power of the headphone amplifier. Bypass HPVSS with a capacitor located close to HPVSS with a short trace length to HPGND. Close decoupling of HPVSS minimizes supply ripple and maximizes output power from the headphone amplifier.

HPSNS senses ground noise on the headphone jack and adds the same noise to the output audio signal, thereby making the output (headphone output minus ground) noise free. Connect HPSNS to the headphone jack shield to ensure accurate pickup of headphone ground noise.

Bypass SPKLVDD and SPKRVDD to SPKLGND and SPKRGND, respectively, with as little trace length as possible. Connect SPKLP, SPKLN, SPKRP, and SPKRN to the stereo speakers using the shortest traces possible. Reducing trace length minimizes radiated EMI. Route SPKLP/SPKLN and SPKRP/SPKRN as differential pairs on the PCB to minimize loop area, thereby the inductance of the circuit. If filter components are used on the speaker outputs, be sure to locate them as close as possible to the IC to ensure maximum effectiveness. Minimize the trace length from any ground-connected passive components to SPKLGND and SPKRGND to further minimize radiated EMI.

Route microphone signals from the microphone to the IC as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, ground the negative microphone input as close as possible to the audio source and then treat the positive and negative traces as differential pairs.

An evaluation kit (EV kit) is available to provide an example layout for the IC. The EV kit allows quick setup of the IC and includes easy-to-use software allowing all internal registers to be controlled.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*. Figure 43 shows the dimensions of the WLP balls used on the IC.

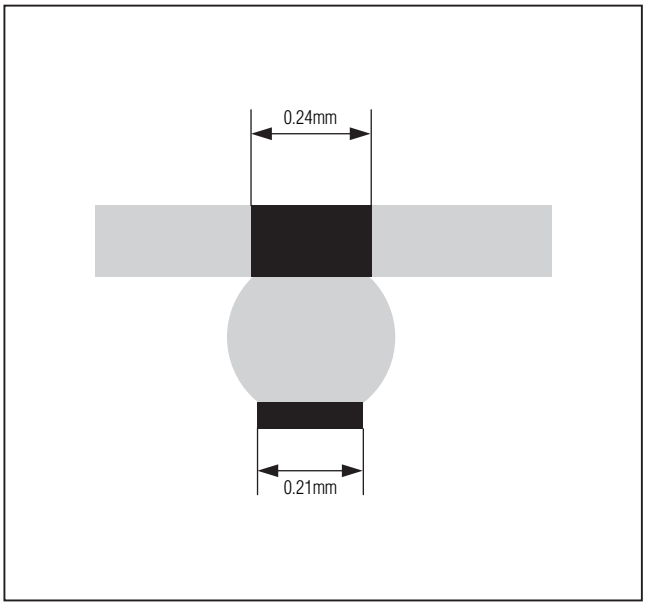


Figure 43. WLP Ball Dimensions

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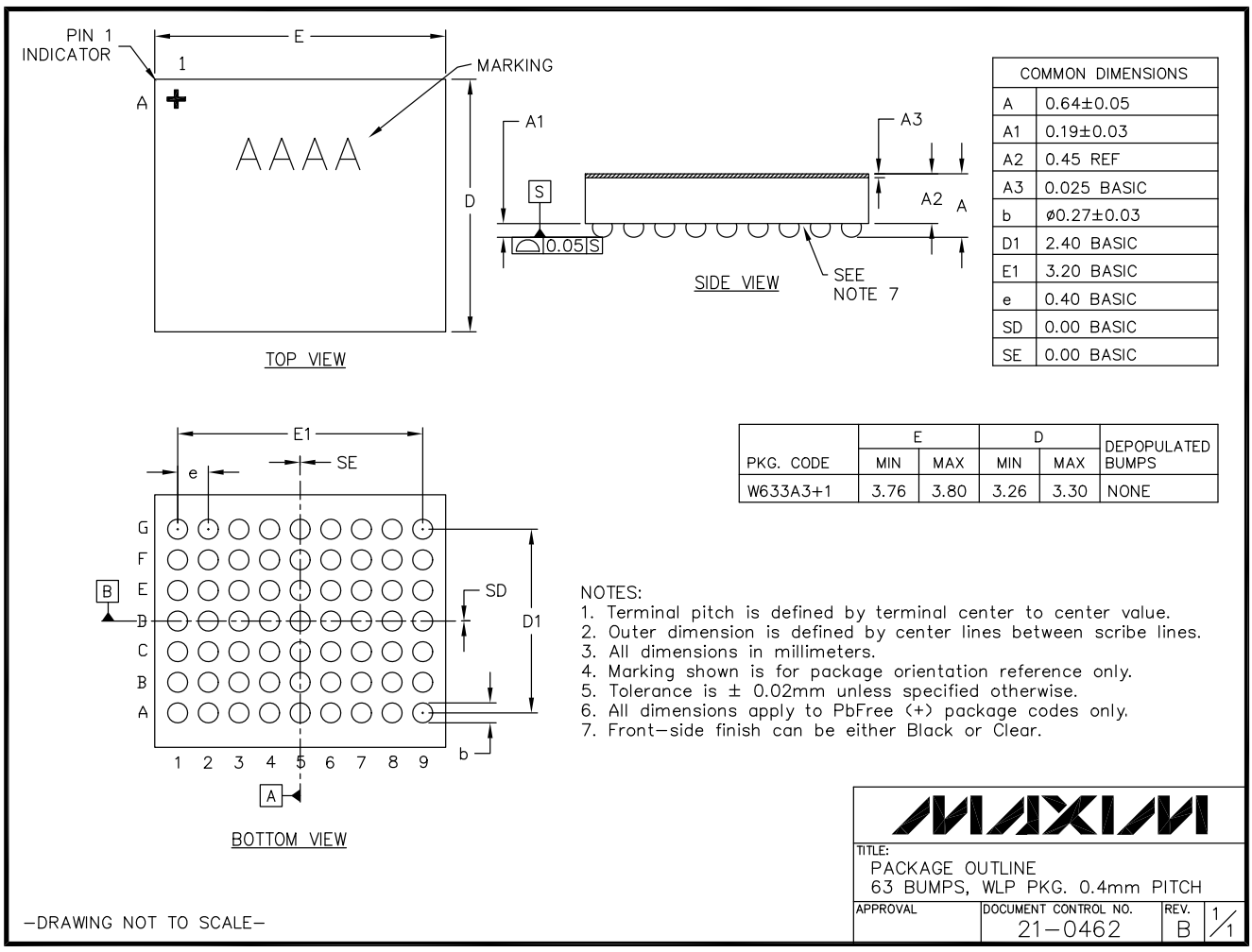
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
63 WLP	W633A3+1	21-0462	Refer to Application Note 1891



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	2/11	Updated DAC playback 48kHz stereo, speaker outputs, speaker maximum value	6