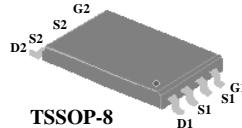




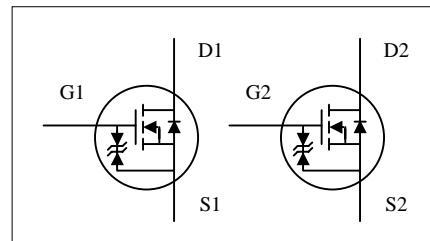
- ▼ Low On-resistance
- ▼ Capable of 2.5V Gate Drive
- ▼ Low Drive Current
- ▼ Surface Mount Package
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	20V
$R_{DS(ON)}$	28mΩ
I_D	4.6A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_A=25^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 4.5\text{V}$	4.6	A
$I_D @ T_A=70^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 4.5\text{V}$	3.7	A
I_{DM}	Pulsed Drain Current ¹	20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1	W
	Linear Derating Factor	0.008	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	125	$^\circ\text{C/W}$



Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=4\text{A}$	-	-	28	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=2\text{A}$	-	-	40	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.5	-	-	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=4.6\text{A}$	-	9.7	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	uA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	25	uA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 10\text{ V}, V_{\text{DS}}=0\text{V}$	-	-	± 10	uA
Q_g	Total Gate Charge	$I_{\text{D}}=4.6\text{A}$	-	12.5	-	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=20\text{V}$	-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=5\text{V}$	-	6.5	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DS}}=10\text{V}$	-	5	-	ns
t_r	Rise Time	$I_{\text{D}}=1\text{A}$	-	9	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_{\text{G}}=3.3\Omega$	-	26.2	-	ns
t_f	Fall Time	$V_{\text{GS}}=5\text{V}$	-	6.8	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	355	-	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=20\text{V}$	-	190	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	85	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_s	Continuous Source Current (Body Diode)	$V_D=V_G=0\text{V}, V_S=1.2\text{V}$	-	-	0.83	A
V_{SD}	Forward On Voltage ²	$T_j=25^\circ\text{C}, I_s=1.25\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board ; 208°C/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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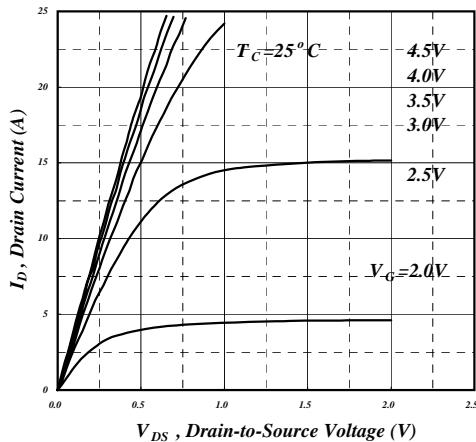


Fig 1. Typical Output Characteristics

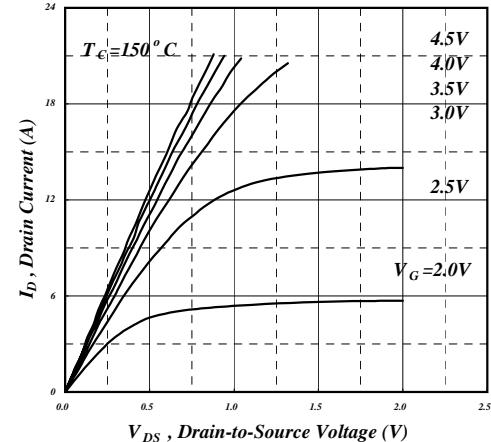


Fig 2. Typical Output Characteristics

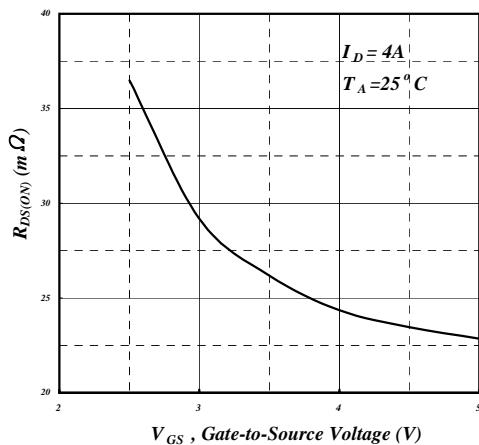


Fig 3. On-Resistance v.s. Gate Voltage

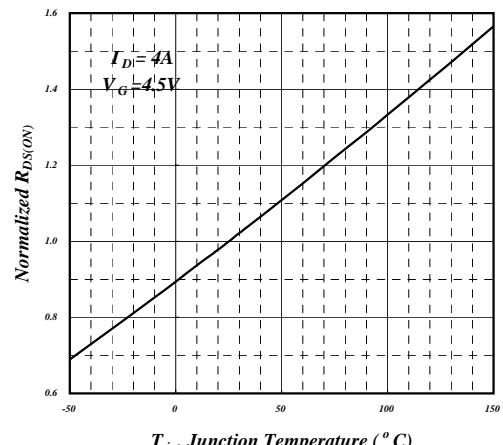


Fig 4. Normalized On-Resistance

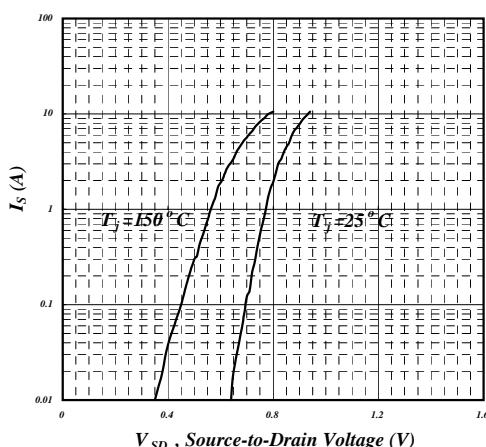


Fig 5. Forward Characteristic of Reverse Diode

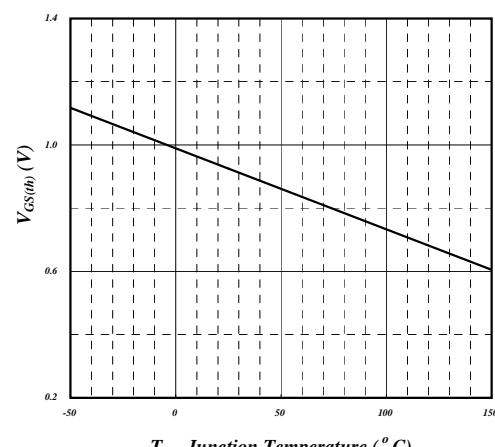


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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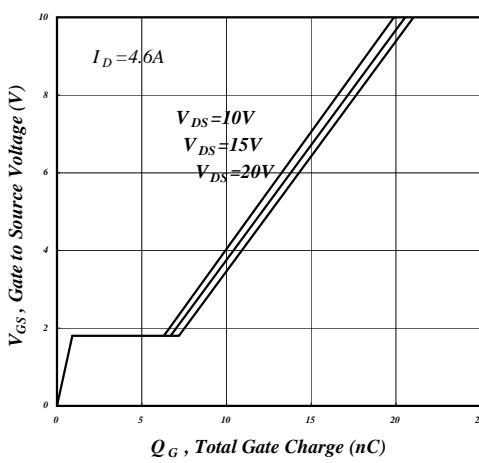


Fig 7. Gate Charge Characteristics

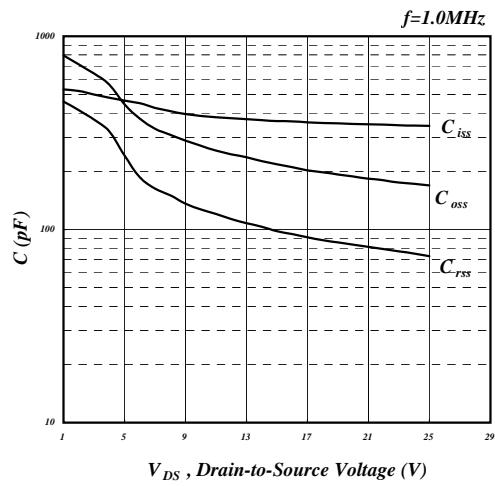


Fig 8. Typical Capacitance Characteristics

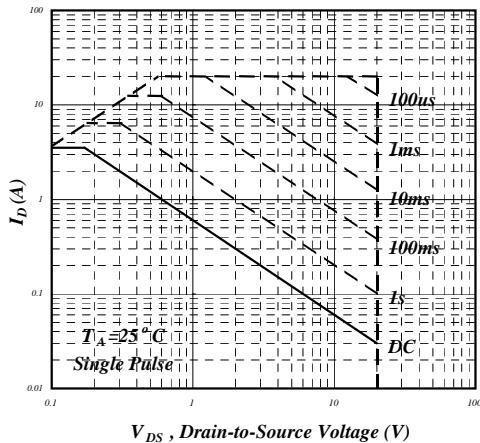


Fig 9. Maximum Safe Operating Area

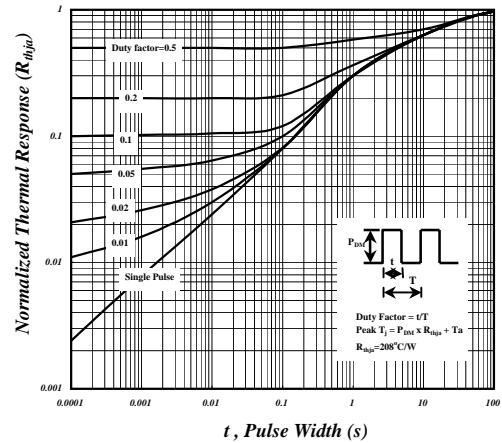


Fig 10. Effective Transient Thermal Impedance

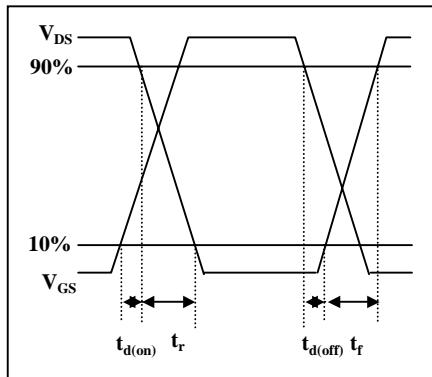


Fig 11. Switching Time Waveform

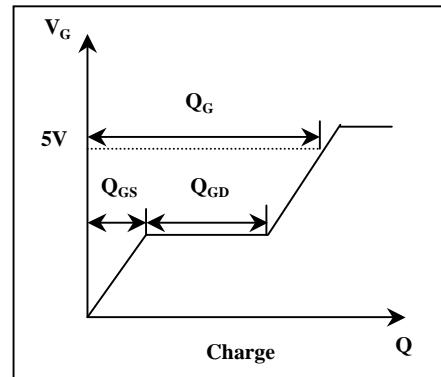


Fig 12. Gate Charge Waveform



MARKING INFORMATION

