plerow™ APL0800-R/T

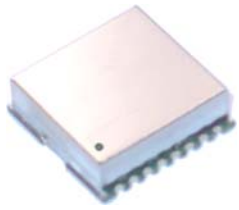
PLL Synthesizer Module

Features

- +8 dBm Output Level at 800 MHz
- Channel Step Size : 200kHz
- 2nd Harmonic: < - 20dBc
- Spurious Level : < -70 dBc
- Lock Time : <10 ms
- 40 mA Current Consumption

Description

The plerow™ PLL synthesizer module was designed for use in wireless and wireline systems in a wide range of frequency from 50 MHz to 6 GHz. ASB's PLL provides exceptionally low spurious and phase noise performance with fast locking time and low current consumption. All products are available in a surface-mount type package.



Specifications

Parameter	Unit	Min.	Typical	Max.
Frequency Range	MHz		800	
Output Power	dBm	+6	+ 8	+10
Supply Voltage	V	4.7	5.0	5.3
Current Consumption	mA		30	40
Channel Step Size	kHz		200	
2 Harmonics (Fundamental)	dBc		-25	-20
Spurious Level	dBc		-75	-70
Lock Time	ms		5	10
Reference Frequency	MHz		13	
Reference Input Level	dBm			
Phase Noise (C / N)				
@ 1 KHz	dBc/Hz		-80	-75
@ 10 kHz			-105	-102
@ 100 kHz			-120	-115
Output Impedance	Ω		50	
Operating Temp. Range	°C	-40	25	85
Package Type & Size	mm	SMT, 19.0W×19.0L×5.8H		

1) Measurement conditions are as follows: T = 25°C, V_{CC} = 5 V, Freq. = 800 MHz, 50 ohm system.

More Information

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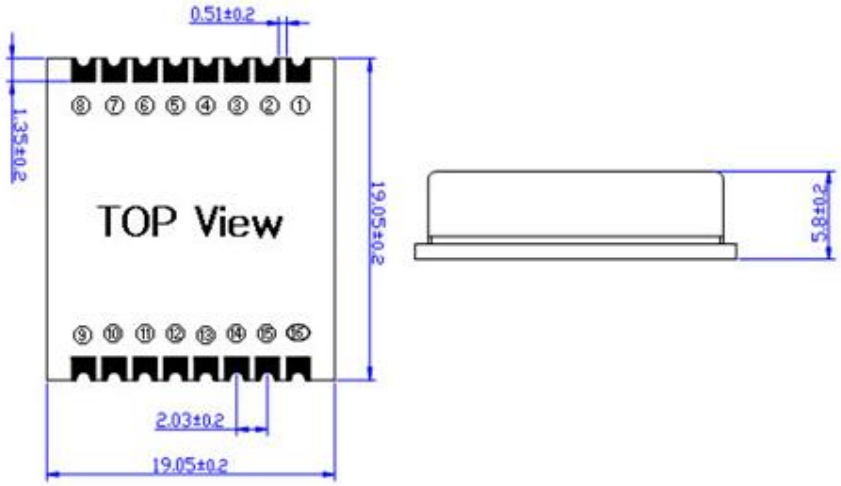
Outline Drawing

APL0000-R/T Type

Type	Dimension
PLL IC + VCO + ROM + TCXO	19 x 19 x 5.8



Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GROUND	9	VCC (VCO)
2	GROUND	13	RF OUT
3	GROUND	15	VCC (PLL)
4	GROUND	16	LOCK DETECT
All other Pins are Grounded / Internal TCXO and ROM