POSEICO SPA
Via Pillea 42-44, 16153 Genova - ITALY
Tel. + 39 010 8599400 - Fax + 39 010 8682006
Sales Office:
Tel. + 39 010 8599400 - sales@poseico.com

PHASE CONTROL THYRISTOR

AT875HT

Repetitive voltage up to **4400 V**
Mean forward current **2003 A**
Surge current **25,2 kA**

FINAL SPECIFICATION

Feb. 17 - Issue: 4

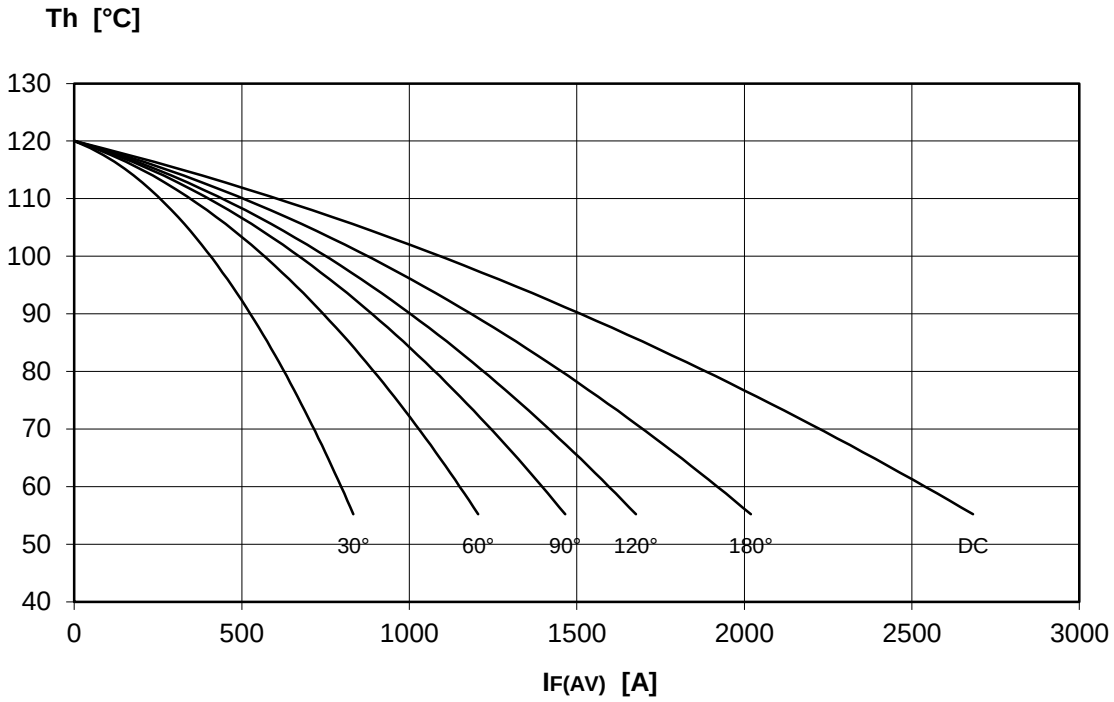
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		120	4400	V
V_{RSM}	Non-repetitive peak reverse voltage		120	4500	V
V_{DRM}	Repetitive peak off-state voltage		120	4400	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	120	200	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	120	200	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin ,50 Hz, Th=55°C, double side cooled		2003	A
$I_{T(AV)}$	Mean forward current	180° sin ,50 Hz, Tc=85°C, double side cooled		1522	A
I_{TSM}	Surge forward current	Sine wave, 10 ms	120	25,2	kA
I^2t	I^2t	without reverse voltage		3175 x 10^3	A^2s
V_T	On-state voltage	On-state current = 2000 A	25	2,00	V
$V_{T(TO)}$	Threshold voltage		120	1,30	V
r_T	On-state slope resistance		120	0,334	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 1600 A; gate 10V, 5Ω	120	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	120	1000	V/µs
t_d	Gate controlled delay time, typical	VD=100V; gate source 40V, 10Ω , tr=.5 µs	25	3	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 75% VDRM		400	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I= 1050 A	120		µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=12V, tp=30µs	25	1000	mA
GATE					
V_{GT}	Gate trigger voltage	VD=12V	25	3,50	V
I_{GT}	Gate trigger current	VD=12V	25	400	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	120	0,80	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			10	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		11	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T_j	Operating junction temperature			-30 / 120	°C
F	Mounting force			40.0 / 50.0	kN
	Mass			1500	g

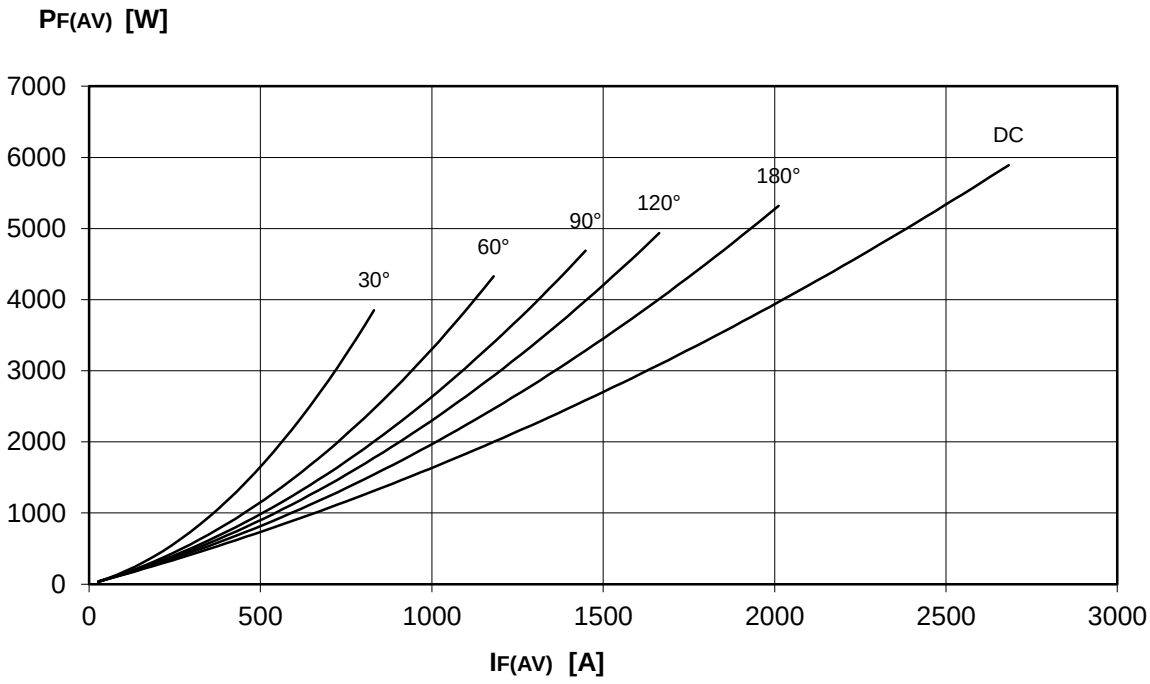
ORDERING INFORMATION : AT875HT S 44

standard specification — VRRM/100

DISSIPATION CHARACTERISTICS

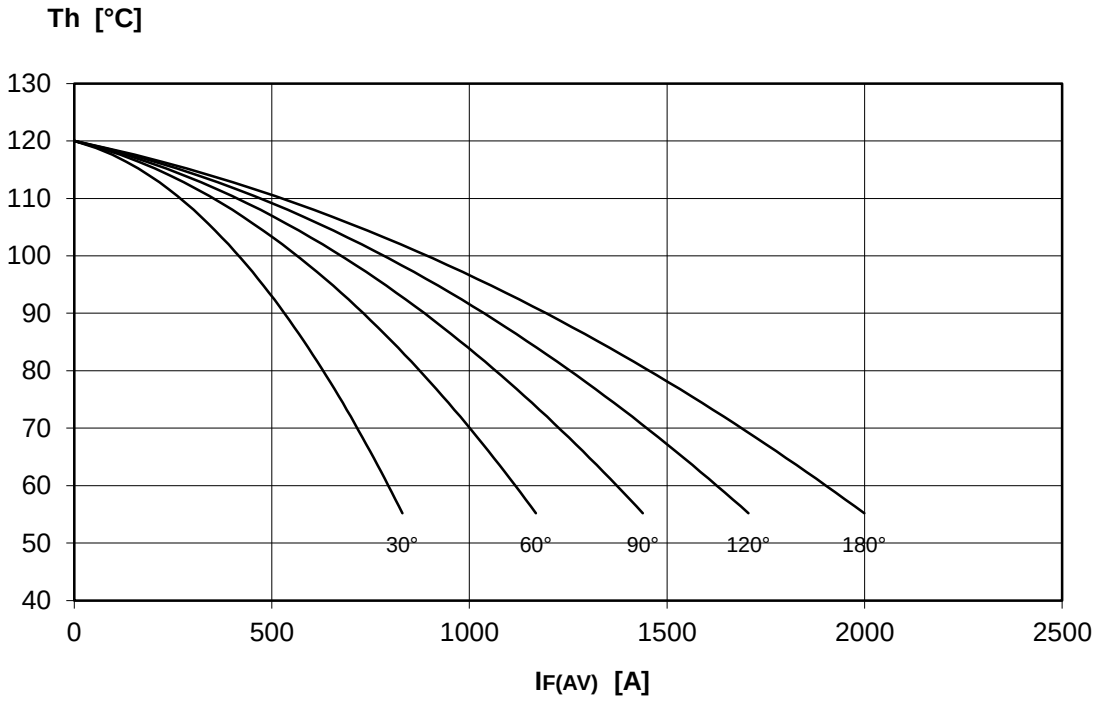
SQUARE WAVE

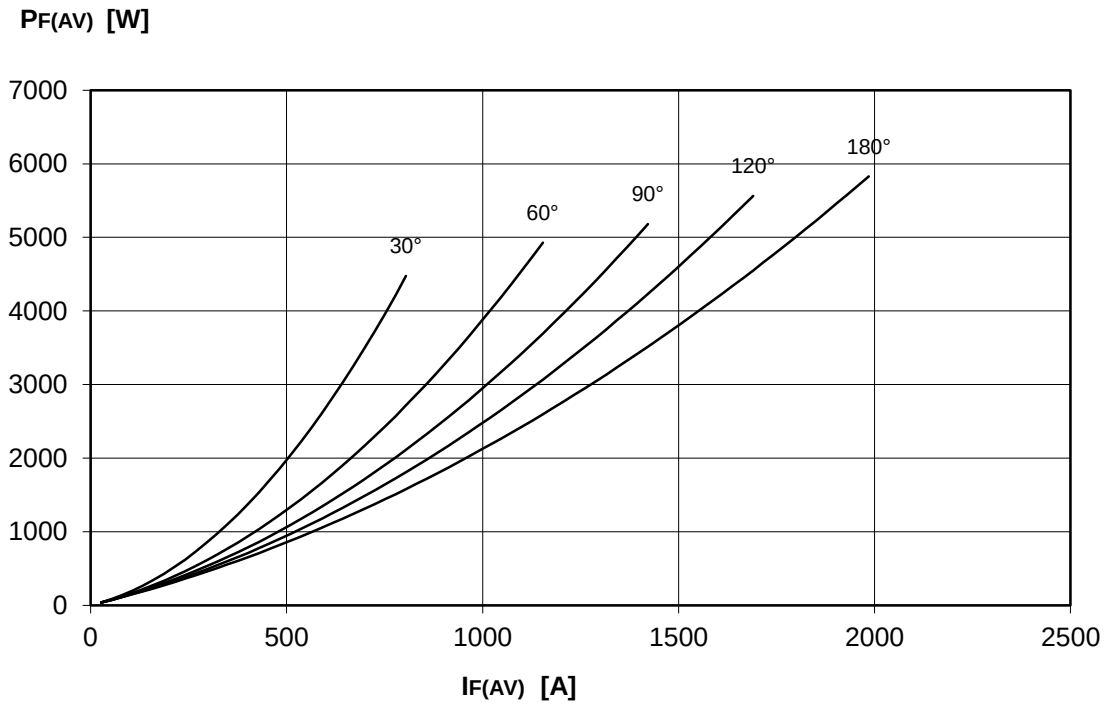




DISSIPATION CHARACTERISTICS

SINE WAVE

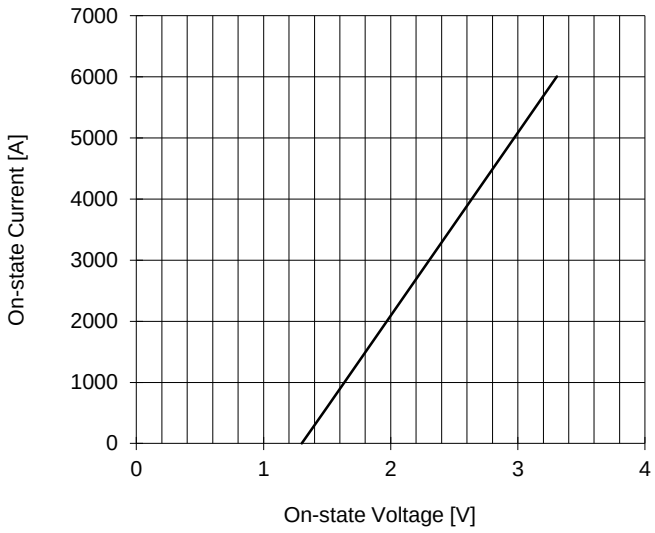




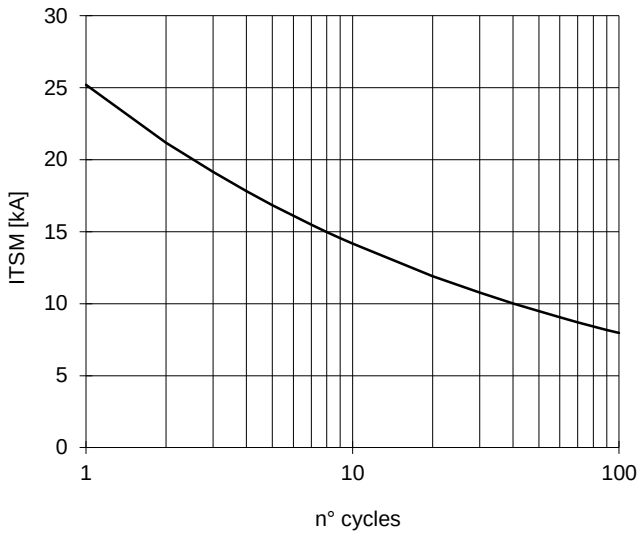
AT875HT PHASE CONTROL THYRISTOR

FINAL SPECIFICATION Feb. 17 - Issue: 4

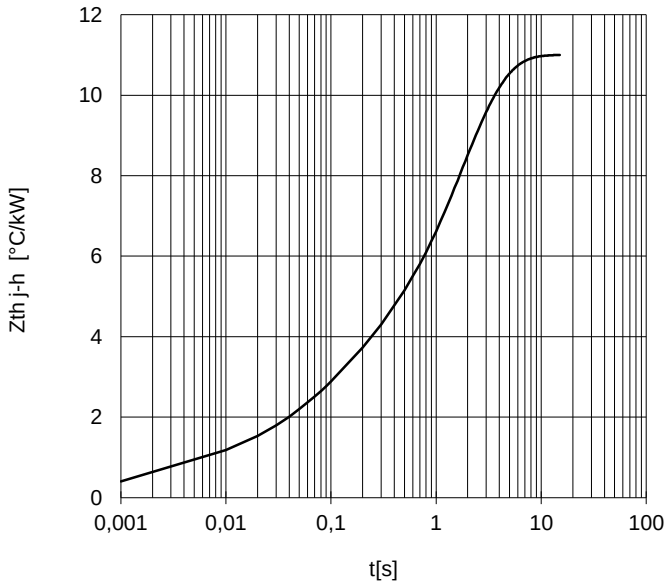
ON-STATE CHARACTERISTIC
Tj = 120 °C

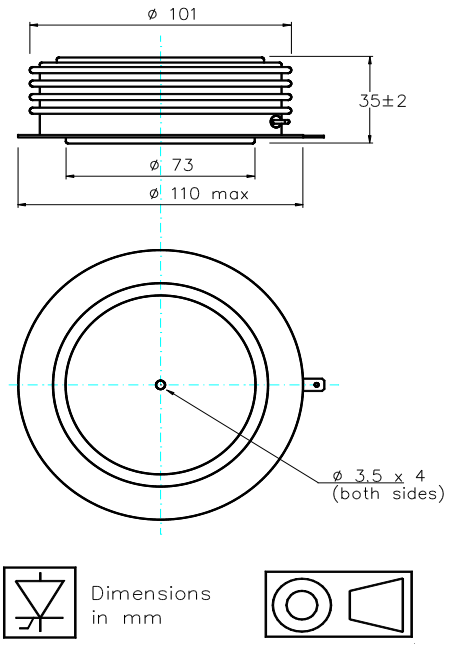


SURGE CHARACTERISTIC
Tj = 120 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Cathode terminal type DIN 46244 - A 4.8 - 0.8
Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

Distributed by