

## **Analog CMOS Integrated Circuits**

# Adjustable 1 - Channel Current Limited Power Switch

#### Description

The KIC6961T is integrated power switches optimized for USB and other hot-swap applications with a programmable current limit feature. Current limit accuracy  $\pm$  10 % can be achieved at high current-limit settings.

The family of devices complies with USB 2.0 and is available with high polarity of Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality.

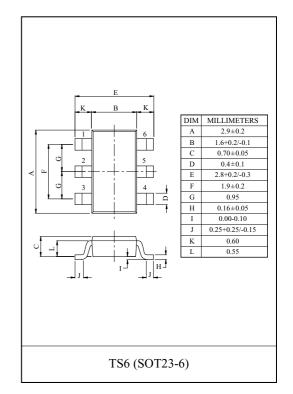
#### Features

□ Single USB Port Power Switches with discharge
□ Operating input voltage range 2.7V to 5.5V
□ Up to 2.1A Maximum Load Current
□ Adjustable Current Limit : 0.5A to 2.6A
□ Reverse Current Blocking
□ Fault report with blanking time(7ms)
□ 100mΩ Power MOSFET
□ Qualified to AEC-Q100.

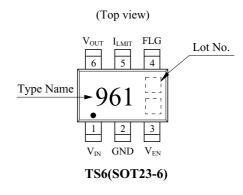
## Maximum Ratings (Ta=25°C)

Characteristic	Symbol	Rating	Unit
Input Voltage	V <sub>IN</sub>	6.5	V
Output Voltage	V <sub>OUT</sub>	6.5	V
Power Dissipation (No Heatsink)	P <sub>D</sub> *	900	mW
Operating Junction Temperature	Tj	-40 ~ 125	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ 150	

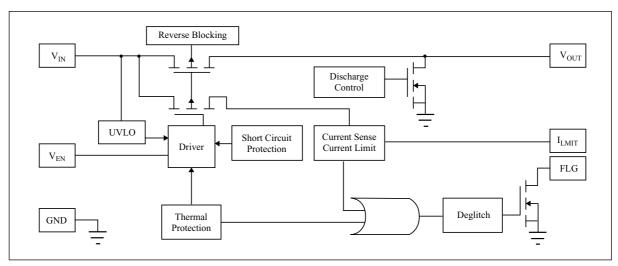
\* Note ) Package Mounted on a Ceramic Board (600mm<sup>2</sup>  $\times$  0.8mm)



#### **Pin Configurations**



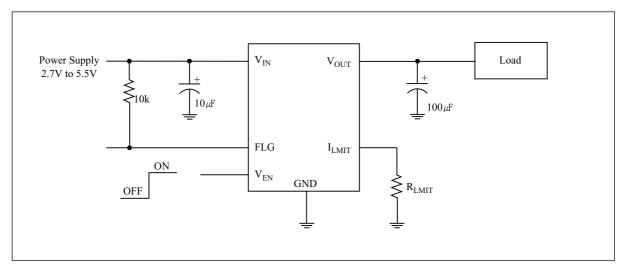
## **Block Diagram**



## **Pin Descriptions**

Pin Number	Pin Name	Descriptions
1	V <sub>IN</sub>	Voltage input pin
2	GND	Ground
3	V <sub>EN</sub>	Enable input (Active high)
4	FLG	Over-current and over-temperature fault report pin (Open drain)
5	I <sub>LMIT</sub>	Current limit set pin
6	V <sub>OUT</sub>	Voltage output pin

## **Typical Application Circuit**



# Recommended Operating Conditions (Ta=25 °C, Unless otherwise stated)

Symbol	Parameter	Min.	Max.	Units
V <sub>IN</sub>	Input Voltage	2.7	5.5	V
V <sub>EN</sub>	Enable Voltage	0	5.5	V
V <sub>IH</sub>	High-Level Input Voltage on EN	2.0	V <sub>IN</sub>	V
V <sub>IL</sub>	V <sub>IL</sub> Low-Level Input Voltage on EN		0.8	V
R <sub>LMIT</sub>	Current-Limit Threshold Resistor Range (1% initial tolerance)	10	49.9	kΩ

# Electrical Characteristics (V\_{IN}\!\!=\!\!5V, Ta=25 $^\circ\!\!\mathbb{C},$ Unless otherwise stated)

Characteristics	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Supply						
Input UVLO	V <sub>UVLO</sub>	V <sub>IN</sub> rising	1.6	2.2	2.5	V
Input UVLO Hysteresis	VUVLO	V <sub>IN</sub> decreasing	50	100	150	mV
Input Shutdown Current	I <sub>SHDN</sub>	Disabled, $I_{OUT} = 0A$	0.2	0.5	1.0	μA
Input Quiescent Current	I <sub>Q</sub>	Enabled, $I_{OUT} = 0A$	20	45	70	μA
Input Leakage Current	I <sub>LEAK</sub>	Disabled, V <sub>OUT</sub> grounded	-	0.1	1	μA
Power Switch						
Switch On-Resistance	D	I <sub>OUT</sub> = 1.0A, Ta=25 ℃	-	100	-	mΩ
Switch On-Resistance	R <sub>DS(ON)</sub>	$I_{OUT} = 1.0A, -40 \text{°C} \le Ta \le 85 \text{°C}$	-	-	150	mΩ
Output Turn-On Rise Time	T <sub>R</sub>	$C_L=1\mu F, R_{LOAD}=10\Omega$	-	0.6	1.5	ms
Output Turn-Off Fall Time	T <sub>F</sub>	$C_L=1\mu F, R_{LOAD}=10\Omega$	-	0.2	0.4	ms
Current Limit						
		R <sub>LMIT</sub> =10kΩ	2.335	2.594	2.853	А
Current Limit	I <sub>LMIT</sub>	R <sub>LMIT</sub> =20kΩ	1.121	1.246	1.370	А
		R <sub>LMIT</sub> =49.9kΩ	0.419	0.477	0.534	А
Enable Pin	1		I	1	1	1
EN Input Logic Low Voltage	V <sub>IL</sub>	V <sub>IN</sub> = 2.7V to 5.5V	-	-	0.8	V
EN Input Logic High Voltage	V <sub>IH</sub>	V <sub>IN</sub> = 2.7V to 5.5V	2	-	-	V
EN Input Leakage	I <sub>SINK</sub>	V <sub>EN</sub> =5V	-	-	1	μA
Output Discharge		-	I	1		1
Discharge time	T <sub>DIS</sub>	$C_L=100\mu F, R_{LOAD}=10\Omega$	1	3	6	ms
Reverse Voltage Protection		1	I	1		1
Reverse Leakage Current	I <sub>REV</sub>	Disabled, $V_{IN}=0V$ , $V_{OUT}=5V$ , $I_{REV}@V_{IN}$	-	0.1	1	μA
Fault Flag	1	1		1	1	
FLG Blanking time	T <sub>BLANK</sub>	$C_{IN}=10\mu F, C_L=22\mu F$	4	7	15	ms
Thermal Shutdown						I
Thermal Shutdown Threshold	T <sub>SHDN</sub>	Enabled, $R_{LOAD}$ =1k $\Omega$	130	150	170	°C
Thermal Shutdown Hysteresis	T <sub>HYS</sub>	-	-	25	-	°C

### **Current- Limit Threshold Programming (Cont.)**

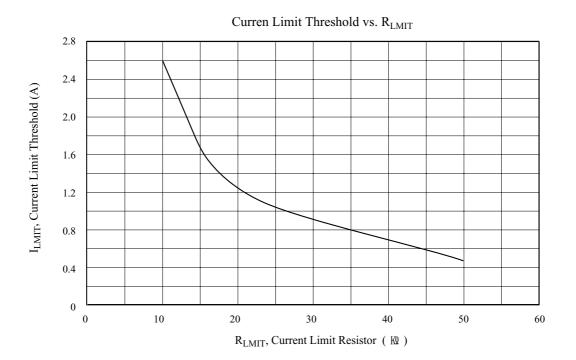
When a heavy load or short circuit situation occurs while the switch is enabled, large transient current may flow through the device. KIC6961T includes a current-limit circuitry to prevent these large currents from damaging the MOSFET switch and the hub downstream ports.

Especially, The KIC6961T is proposed to have current limit flexibility for customer.  $I_{LMIT}$  pin is available to connect pull down resistor to ground, which participate to the current threshold adjustment.

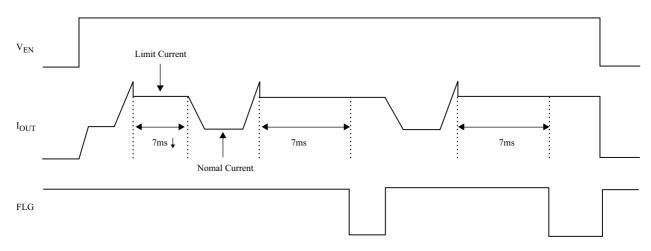
The KIC6961T provides an adjustable current limit threshold between 0.5A and 2.6A (Typ.) via an external resistor,  $R_{LMIT}$ , between 10k $\Omega$  and 49.9k $\Omega$ .

It s strongly recommended to use 0.1 or 1% resistor tolerance to keep the over current accuracy.

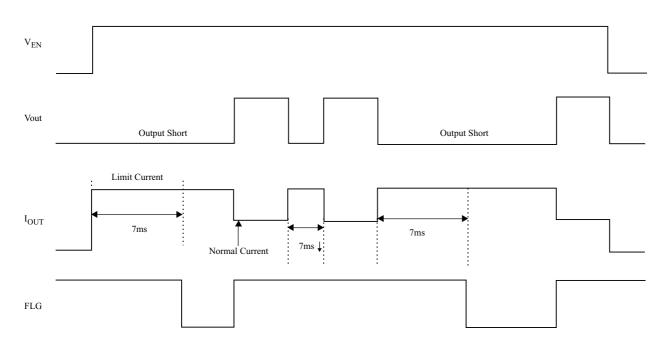
Once the current limit threshold is exceeded, the device enters constant-current mode until either thermal shutdown occurs or the fault is removed.

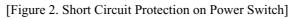


# **Over Current & Short Circuit Protection Timing Chart**



[Figure 1. Over Current Protection on Power Switch]





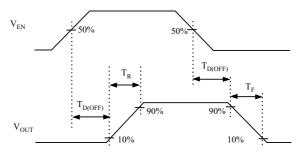
## **\* FLG Response Condition**

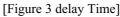
	CONDITION	FLG	Remark
Over - Load	V <sub>IN</sub> - V <sub>OUT</sub> □0.5V	Active L	
Short Circuit	-	Active L	

# **\***Actual Waveform

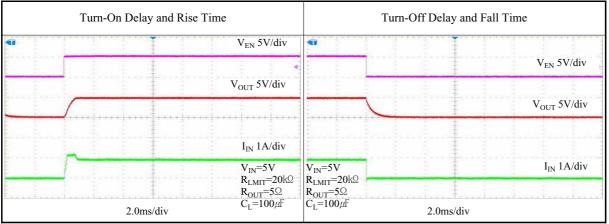
R <sub>LMIT</sub>	Over Load	Short Circuit	
	V <sub>OUT</sub> 5V/div	V <sub>OUT</sub> 5V/div	
	FLG 5V/div	$\begin{array}{c} V_{IN}=5V\\ C_{IN}=10\mu\Gamma\\ C_{OUT}=100\mu\Gamma\\ C_{OUT}=100\mu\Gamma\end{array}$	
10kΩ	$I_{IN} \frac{V_{IN}=5V}{R_{L}=1.5\Omega} \\ C_{IN}=10\mu F \\ C_{OUT}=100\mu F$	I <sub>IN</sub> 2A/div	
	100ms/div	100ms/div	
	V <sub>OUT</sub> 5V/div	$\begin{array}{c} V_{IN}=5V\\ C_{IN}=10\mu F\\ C_{OUT}=100\mu F\end{array}$	
	FLG 5V/div	FLG 5V/div	
20kΩ I <sub>IN</sub> 1A/div	$I_{IN} 1A/div \qquad \begin{array}{c} V_{IN} = 5V \\ R_L = 3\Omega \\ C_{IN} = 10 \mu F \\ C_{OUT} = 100 \mu F \end{array}$	I <sub>IN</sub> 1A/div	
	100ms/div	100ms/div	
	V <sub>OUT</sub> 5V/div	V <sub>out</sub> 5V/div	
<b>49.9</b> kΩ	FLG 5V/div	FLG 5V/div	
	$I_{IN}$ 500mA/div $V_{IN}$ =5V $R_L$ =4 $\Omega$ $C_{IN}$ =10 $\mu$ F	$I_{IN} 500 \text{mA/div} V_{IN} = 5V C_{IN} = 10 \mu F C_{OUT} = 100 \mu F$	
	C <sub>OUT</sub> =100µf 100ms/div	100ms/div	

(7) Enable Function Timing Chart

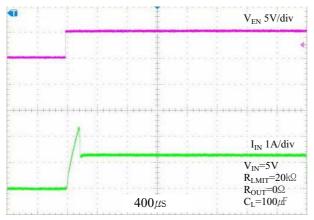




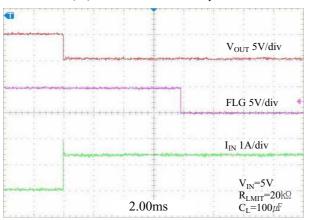
## **\***Actual Waveform



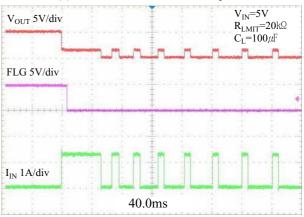
(8) Device Enabled into Short-Circuit



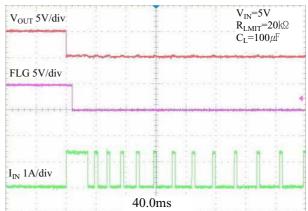
(10) Short-Circuit Limit Response



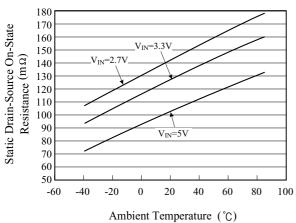
(9) No Load to  $1\Omega$  Transient Response

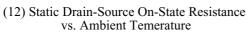












### **Functional Description**

### 1. Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

### 2. Thermal Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults are present for extended periods of time. The KIC6961T implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately  $150^{\circ}$ C, the Thermal protection feature gets activated as follows: The internal thermal sense circuitry turns the power switch off and the FLG output is asserted thus preventing the power switch from damage. Hysteresis in the thermal sense circuit allows the device to cool down to approximately  $25^{\circ}$ C before the output is turned back on. This built-in thermal hysteresis feature is an excellent feature, as it avoids undesirable oscillations of the thermal protection circuit. The switch continues to cycle in this manner until the load fault is removed, resulting in a pulsed output. The FLG open-drain output is asserted when an over-current occurs with 7-ms deglitch.

### 3. Under-Voltage Lockout (UVLO)

Under-voltage lockout function (UVLO) guarantees that the internal power switch is initially off during start-up. The UVLO functions only when the switch is enabled. Even if the switch is enabled, the switch is not turned ON until the power supply has reached at least 2.2V. Whenever the input voltage falls below approximately 2.2V, the power switch is turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

## 4. Reverse Current Protection

In a normal MOSFET switch, current can flow in reverse direction (from the output side to the input side) when the output side voltage is higher than the input side, even when the switch is turned off. A reverse-current blocking feature is implemented in the KIC6961T to prevent such back currents. This circuit is activated by the difference between the output voltage and the input voltage. When the switch is disabled, this feature blocks reverse current flow from the output back to the input.

#### 5. Discharge Function

When enable is de-asserted, the discharge function is active. The output capacitor is discharged through an internal NMOS that has a discharge resistance of  $100\Omega$ . Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

#### 6. FLG Response

The FLG open-drain output goes active low for any of the two conditions: Over-Current or Over-Temperature. The time from when a fault condition is encountered to when the FLG output goes low is 7-ms (TYP). The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary Over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The KIC6961T is designed to eliminate erroneous Over-current reporting without the need for external components, such as an RC delay network.

## **Applications Information**

## 1. Supply Filtering

Placing a high-value electrolytic capacitor on the input (10uF minimum) and output pin (100uF) is recommended when the output load is heavy.

This precaution also reduces power-supply transients that may cause rining on the input.

## 2. Enable Input

 $V_{EN}$  must be driven logic high for a clearly defined input. Floating the input may cause unpredictable operation.  $V_{EN}$  should not be allowed to go negative with respect to GND.