

NPN High Voltage Planar Transistor

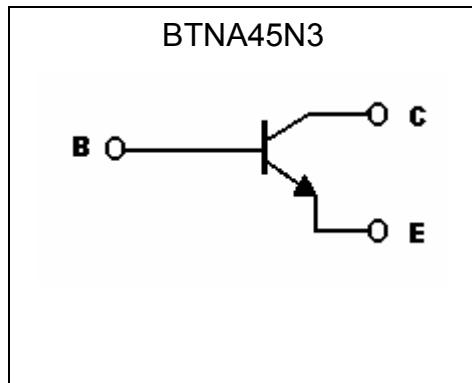
BTNA45N3

BV_{CEO}	500V
I_C	150mA
V_{CESAT}	150mV (max)

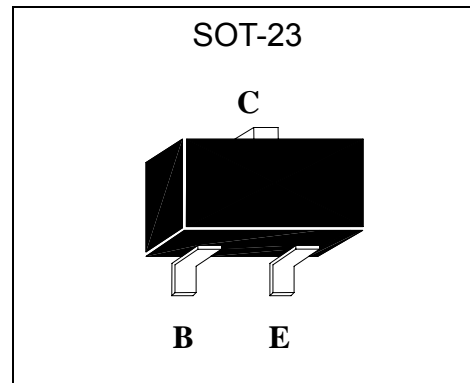
Features

- High breakdown voltage. ($BV_{CEO}=500V$)
- Low collector-emitter saturation voltage V_{CESAT} .
- High collector current capability I_C and I_{CM} .
- High collector current gain H_{FE} at high collector current I_C .
- Low collector output capacitance. (Typ. 5pF at $V_{CB}=20V$)
- Pb-free lead plating and halogen-free package.

Symbol



Outline



Absolute Maximum Ratings ($T_a=25^{\circ}C$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CB0}	500	V
Collector-Emitter Voltage	V_{CES}	500	
Collector-Emitter Voltage	V_{CEO}	500	
Emitter-Base Voltage	V_{EBO}	7	
Collector Current	I_C	150	mA
Peak Collector Current , single pulse, pulse width $t_p < 1ms$	I_{CM}	500	
Peak Base Current, single pulse, pulse width $t_p < 1ms$	I_{BM}	200	
Power Dissipation (Note)	P_d	300	mW
Junction Temperature	T_j	150	$^{\circ}C$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}C$

Note : Device mounted on a FR-4 PCB, single sided copper, tin plated and standard footprint.

**Thermal Characteristics**

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient, in free air (Note)	Rth,j-a	417	°C/W
Thermal Resistance, Junction-to-Solder point	Rth,j-sp	70	

Note : Device mounted on a FR-4 PCB, single sided copper, tin plated and standard footprint.

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
*BV _{CBO}	500	-	-	V	I _C =50μA
*BV _{CES}	500	-	-		I _C =50μA
*BV _{CEO}	500	-	-		I _C =10mA
BV _{EBO}	7	-	-		I _E =50μA
I _{CBO}	-	-	100	nA	V _{CB} =500V
I _{CES}	-	-	100		V _{CE} =500V
I _{EBO}	-	-	100		V _{EB} =5V
*V _{CE(sat) 1}	-	-	90	mV	I _C =20mA, I _B =2mA
*V _{CE(sat) 2}	-	-	150		I _C =50mA, I _B =6mA
*V _{BE(sat)}	-	-	0.9	V	I _C =50mA, I _B =5mA
*V _{BE(on)}	-	-	0.9		V _{CE} =10V, I _C =50mA
*h _{FE 1}	120	-	-	-	V _{CE} =10V, I _C =1mA
*h _{FE 2}	120	-	300	-	V _{CE} =10V, I _C =30mA
*h _{FE 3}	120	-	-	-	V _{CE} =10V, I _C =50mA
*h _{FE 4}	30	-	-	-	V _{CE} =10V, I _C =100mA
f _T	50	-	-	MHz	V _{CE} =20V, I _C =10mA, f=100MHz
Cob	-	5	8	pF	V _{CB} =20V, I _E =0A, f=1MHz
ton	-	110	-	ns	V _{CE} =100V, I _C =50mA, I _{B1} =5mA, I _{B 2} = -10mA
toff	-	1500	-		

*Pulse Test: Pulse Width ≤300μs, Duty Cycle ≤2%

Ordering Information

Device	Package	Shipping	Marking
BTNA45N3	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel	LK

Moisture Sensitivity Level : Conform to JEDEC Level 1

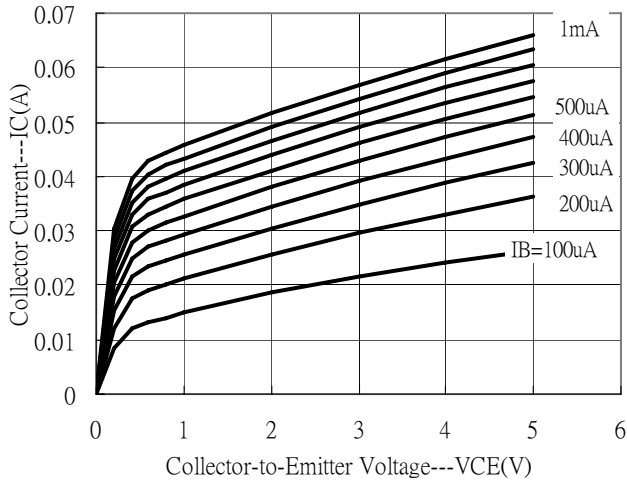
Recommended Storage Condition:

Temperature : ≤ 30 °C

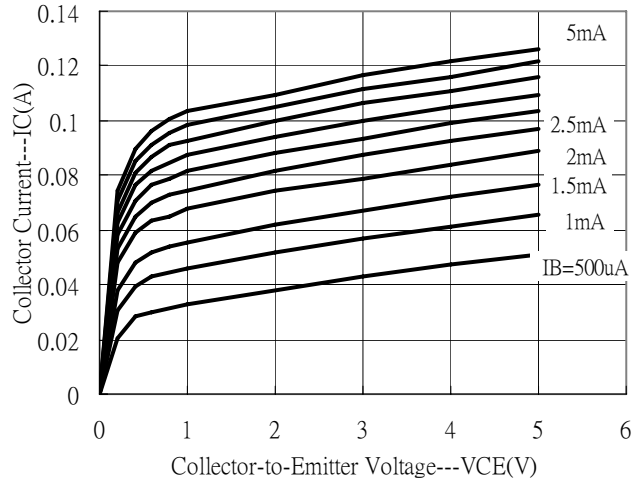
Humidity : ≤ 60% RH

Typical Characteristics

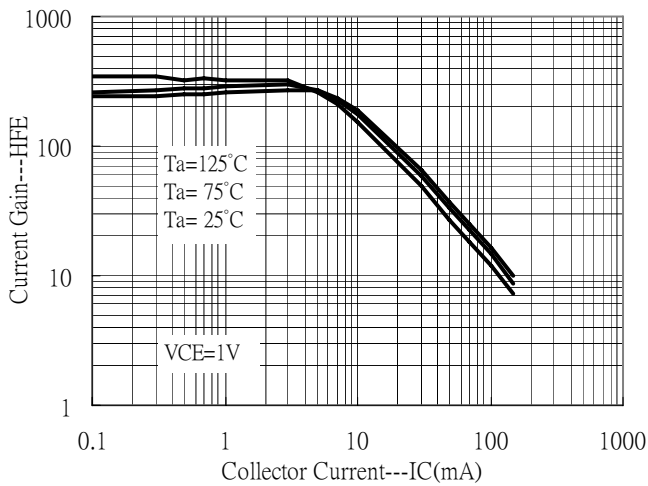
Emitter Grounded Output Characteristics



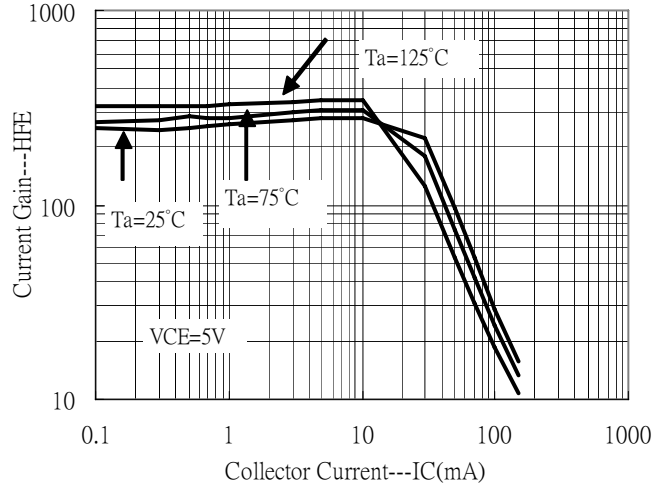
Emitter Grounded Output Characteristics



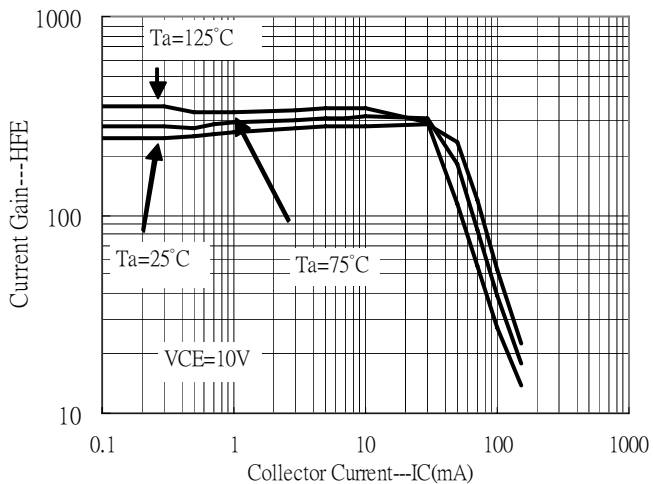
Current Gain vs Collector Current



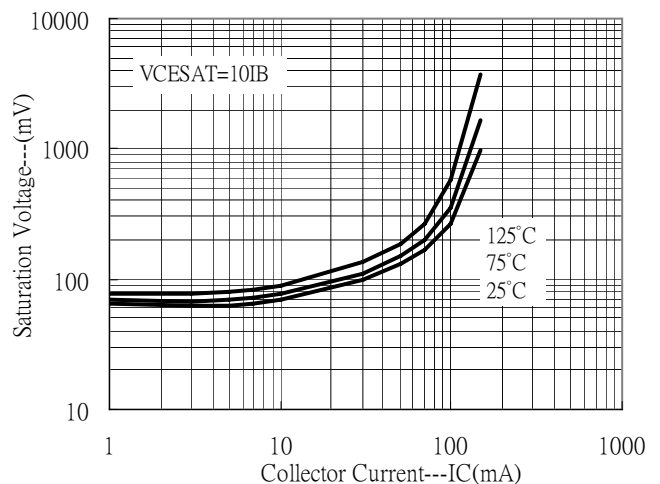
Current Gain vs Collector Current



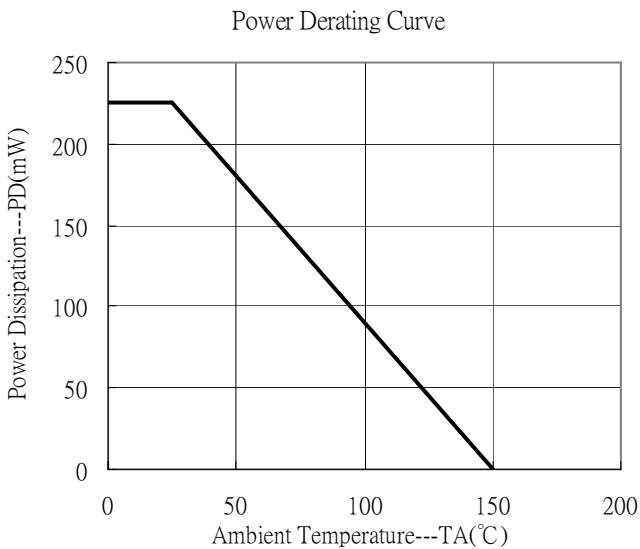
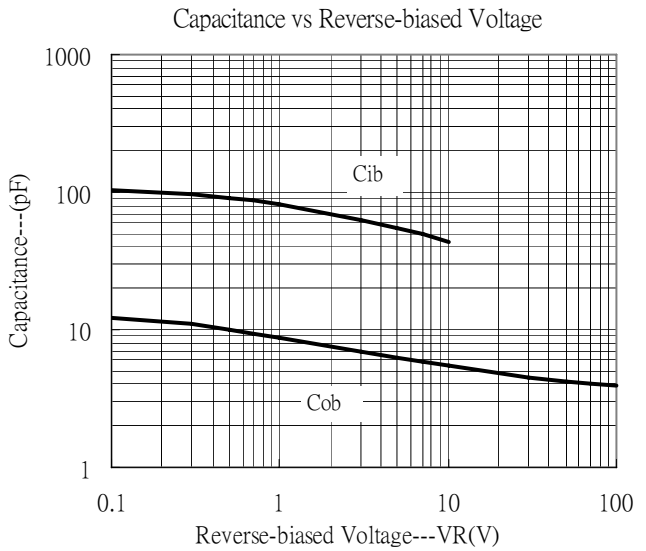
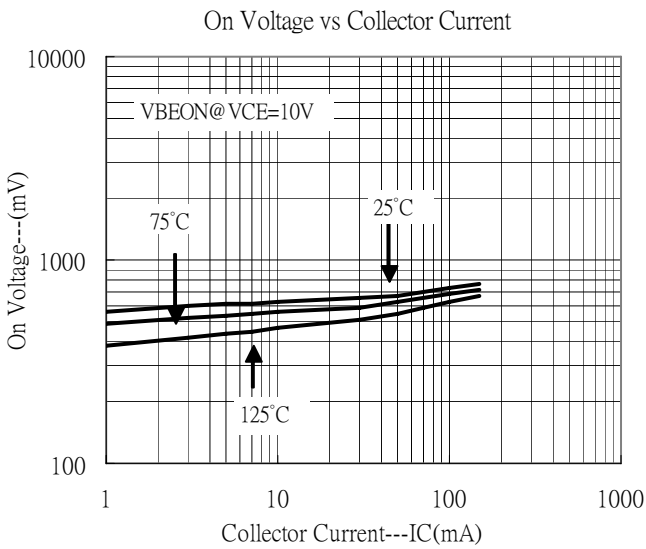
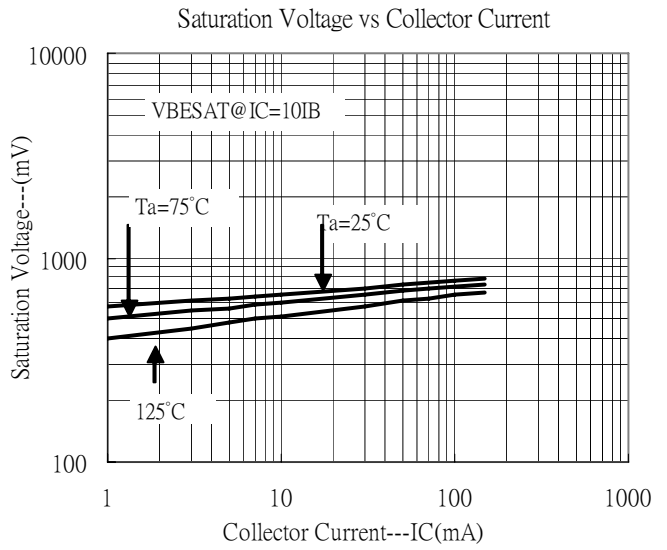
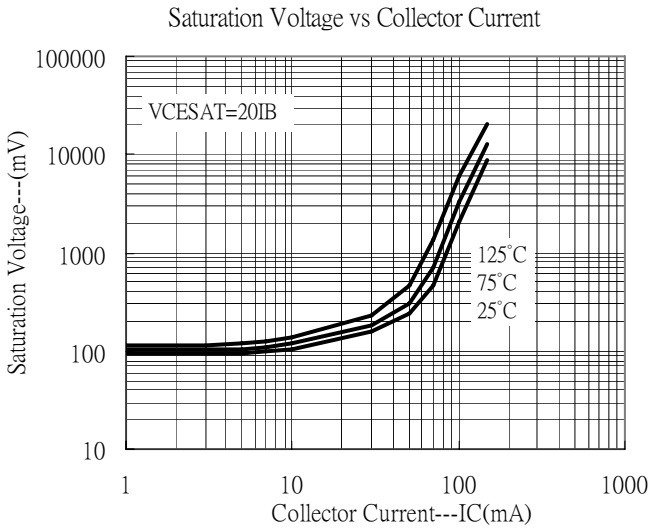
Current Gain vs Collector Current



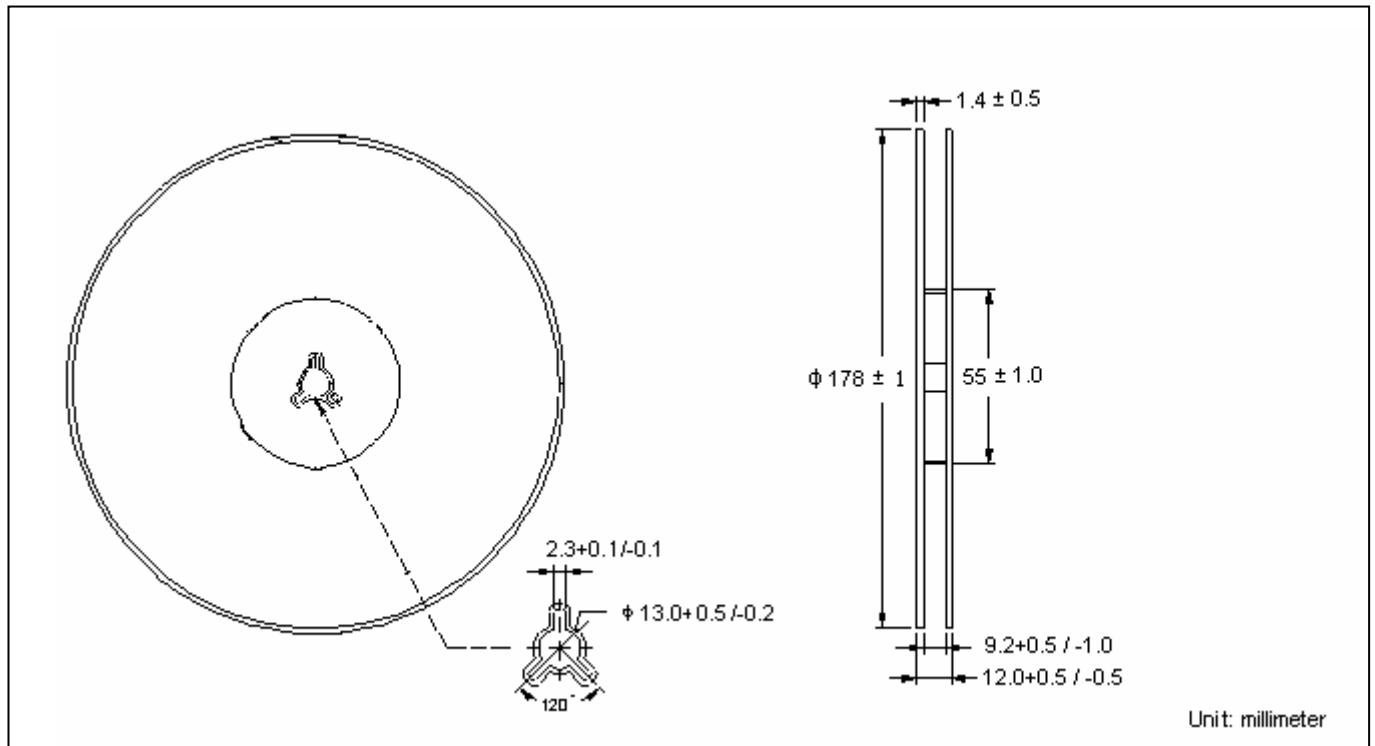
Saturation Voltage vs Collector Current



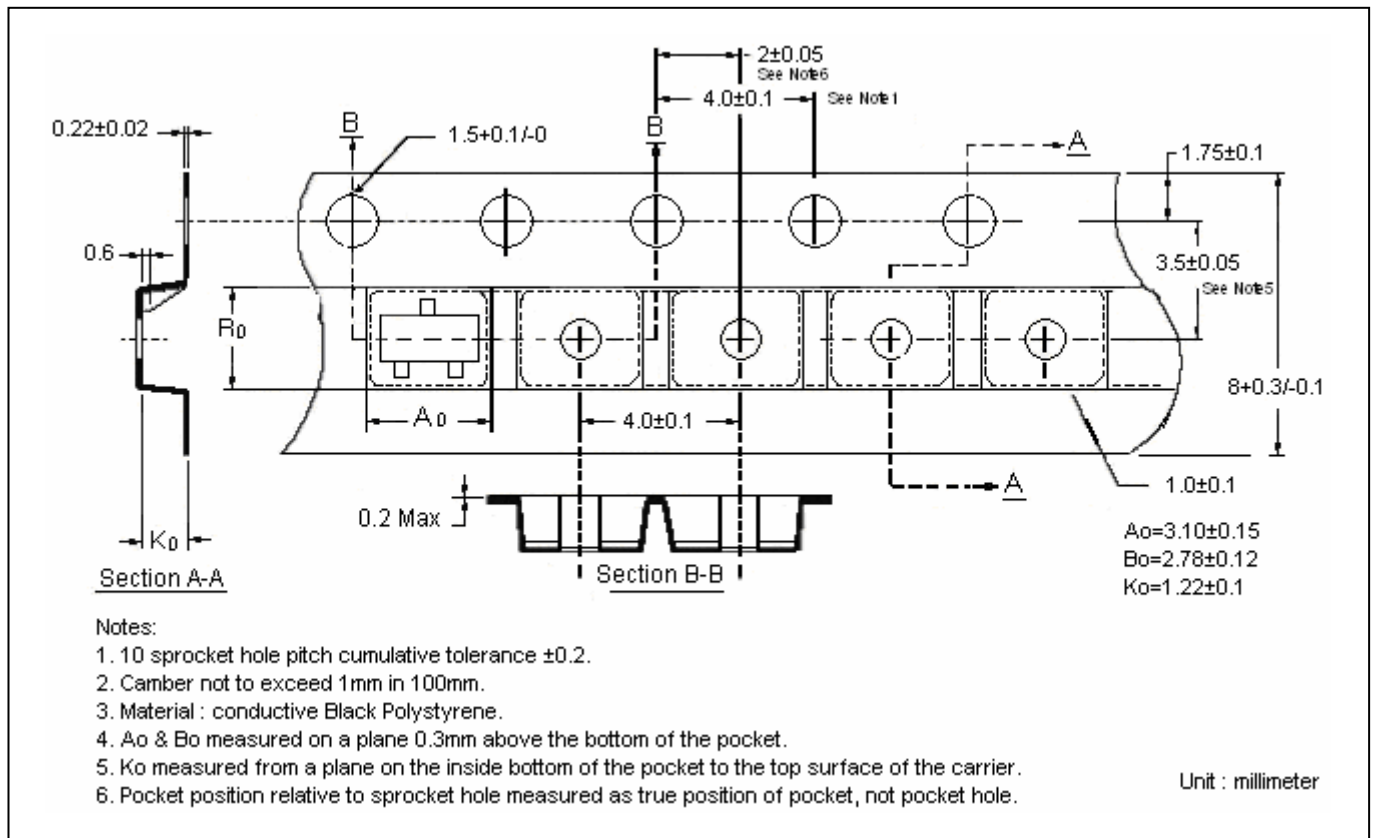
Typical Characteristics(Cont.)



Reel Dimension



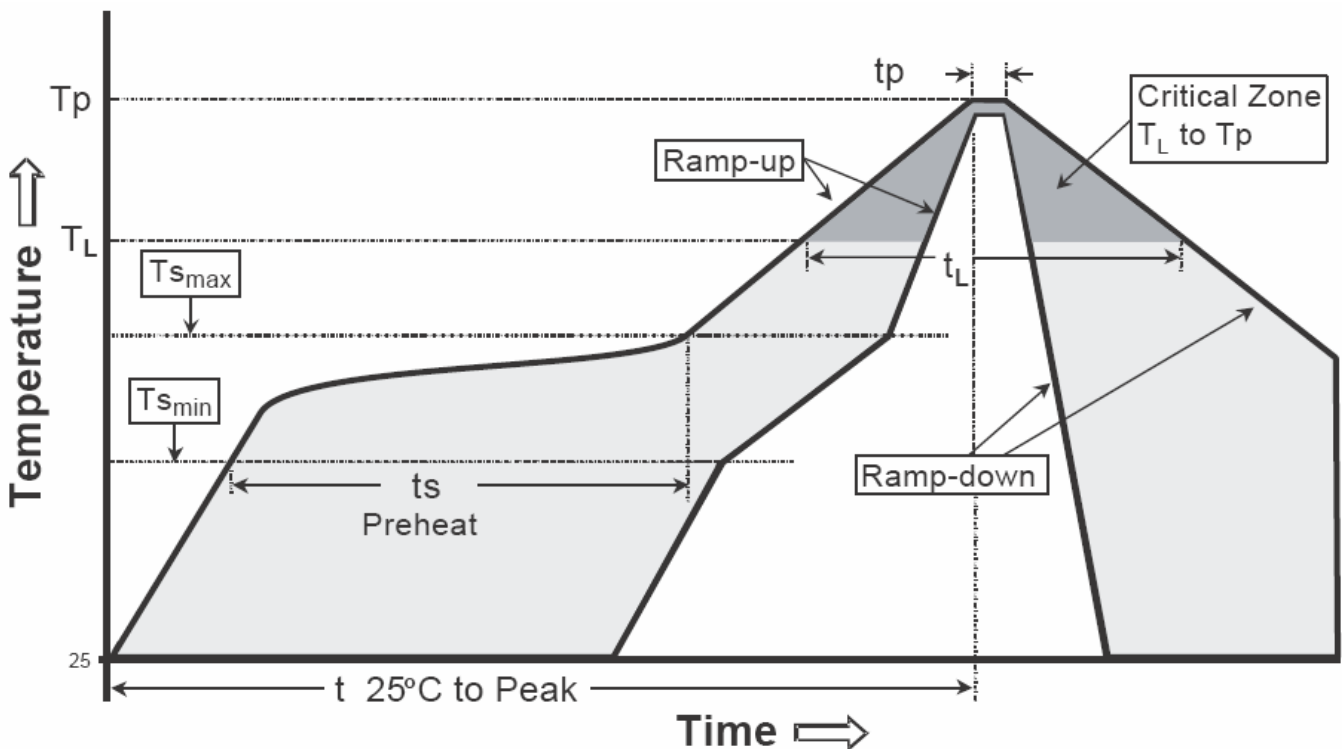
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

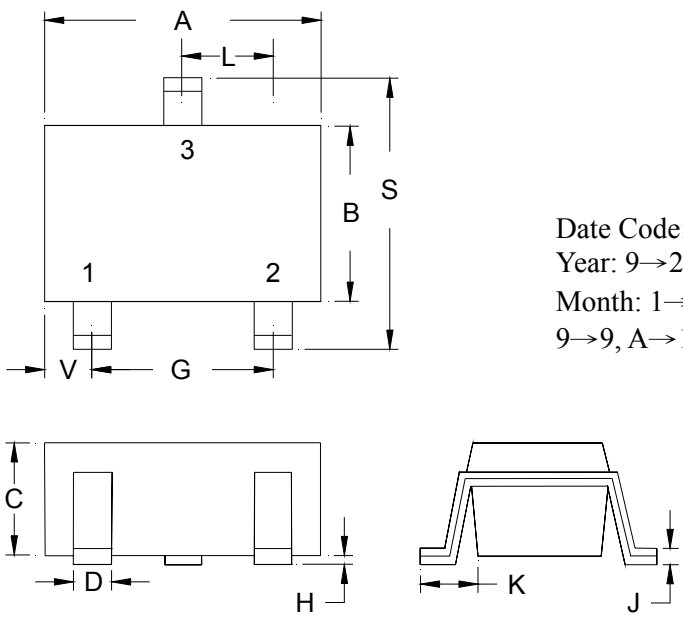
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

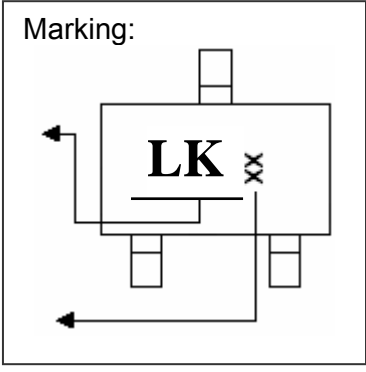
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, and H; and a perspective view with dimensions K and J. The top view labels 1, 2, and 3 correspond to Pin 1, Base, and Collector respectively.

Marking:



The marking diagram shows a rectangular package with three pins. The top surface is marked with 'LK' and 'xx'. Arrows indicate the pin locations.

Product Code

Date Code: Year+Month
 Year: 9→2009, 0→2010
 Month: 1→1, 2→2, . . .
 9→9, A→10, B→11, C→12

3-Lead SOT-23 Plastic Surface Mounted Package
 CYStek Package Code: N3

Style : Pin 1.Base 2.Emitter 3.Collector

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0034	0.0070	0.085	0.177
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1083	2.10	2.75
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0005	0.0040	0.013	0.10					

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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