CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7163
QAM Modem

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DATASHEET

Advance Information

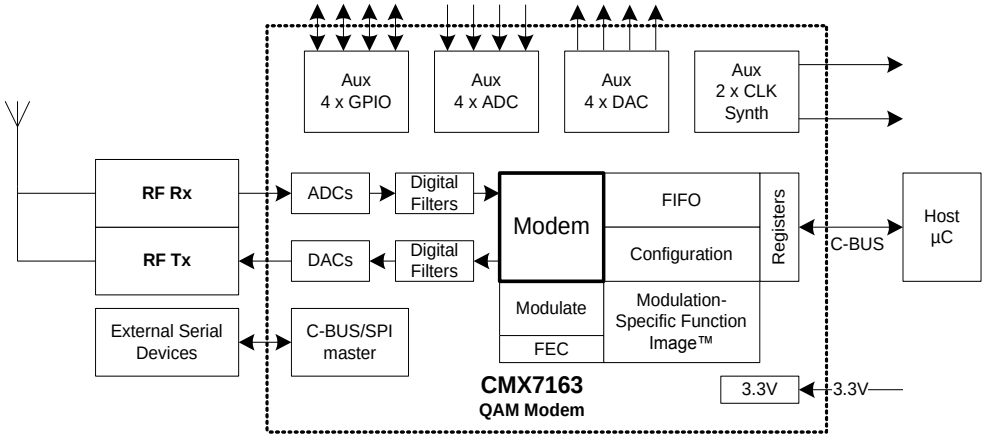
7163 FI-4.x QAM Modem

Features

- Half-duplex QAM modem supports multiple modulations and channel spacings
- No DSP or Codecs required; simply upload modulation Function Image™ (FI)
- QAM 7163 FI-4.x
  - 4/16/64 QAM up to 96kbps in 25kHz
  - Different rate, robust FEC choices
  - Channel estimation and equalisation
  - FEC and raw (uncoded) modes
  - Two x frame sync detectors
  - Automatic frame sync detect
  - Formatted blocks for packet construction
  - Rx carrier frequency and phase correction
  - Receive signal quality measurement
- High Performance I/Q Radio Analogue Interface
  - Tx and Rx: 'Direct connect' to zero IF transceiver
  - Simple external RC filters
  - Digital IF filter reconfigures for multiple RF channel spacings (Rx)
  - Deviation control without manual trim (Tx)
  - I/Q trims
- C-BUS host Serial Interface
  - SPI-like with register addressing
  - Read/Write 128-byte FIFOs and data buffers streamline transfers and relax host service latency
- Auxiliary Functions
  - Four x 10-bit DACs
  - Autonomous RAMDAC sequencer
  - Automatic support for dc calibration of CMX998
  - Four x 10-bit ADCs
  - ADC averaging and trip on high/low 'watch' modes
  - Four x GPIO
  - Sequence GPIO on Tx or Rx trigger
  - Start Tx on digital trigger input
- Master C-BUS/SPI Serial Interface
  - For external slave devices e.g. RF transceiver and synthesiser
  - Pass-through mode expands host C-BUS/SPI capacity
- Two Synthesised Clock Generators
- Low Power 3.3V Operation with Powersave Functions
- Small 64-pin VQFN and LQFP Packages

Applications

- High Performance Narrowband Data Radio
  - Telemetry/SCADA/data modems
  - 6.25kHz to 25kHz RF channel spacing
  - Compatible worldwide e.g. ETSI, FCC, ARIB, etc.
  - FCC Part 90 per new spectral efficiency requirements
- Digital Software Defined Radio (SDR)
- High-speed Wireless Data
- Mobile Data over Fading Channels



This document contains:

Datasheet | User Manual

1 Brief Description

The CMX7163 QAM Modem is a half-duplex device supporting multiple channel spacings under host microcontroller (µC) control. Its *Function Image (FI) is loaded to initialise the device and determine modulation types.

The7163 FI-4.x supports 4-, 16- and 64-QAM modulations, root raised cosine filtered with α=0.2, 0.35 or a user programmable filter. The7163 FI-4.x supports up to 96kbps in a 25kHz channel, with channel estimation and equalization to provide robust performance under realistic channel conditions. Flexible bit rates support a wide range of applications requiring a selectable bit rate and robustness. The 7163FI-4.x supports zero IF (I/Q) transmit and receive. QAM data is over-air compatible with the (CMX)7164FI-4.x.

Forward error correction and raw modes are available and support user-defined packet structures to support a range of applications. For greater flexibility, different rate FEC modes are provided. Receive signal quality measurement is supported, making a useful assessment of link conditions.

High performance digital IF filters may be reconfigured to support multiple channel spacings via host command. This feature may eliminate the need to switch between multiple discrete IF filters.

An integrated analogue interface supports ‘direct connection’ to zero IF I/Q radio transceivers with few external components; no external codecs are required.

Intelligent auxiliary ADC, DAC and GPIO subsystems perform valuable functions and minimise host interaction and host I/O resources. Two synthesised System Clock generators develop clock signals for off-chip use. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

***The *FirmASIC*® Function Image™.** The device utilises CML’s proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7163, which is available in 64-pin VQFN and LQFP packages, operates in the range 3.0 to 3.6 volts and embodies selectable powersaving modes.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

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Information in this data sheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date (D/M/Y)
12	• Section 10.2.6: Entries and descriptions for P4.8 to P4.10 which offer additional control • Section 10.2.4: Clarification to description of frame sync detection and error tolerance	19/6/14
11	• Figure 5 replaced by new drawing showing removal of unused components • Described the state of GPIO pins after reset and before a Function Image is loaded • Added voltage differential between power supplies to section 11 specification • Added details of RAMDAC ramp profile scaling control • Clarified PLL Lock time/Ref divide register • Miscellaneous typographical and editorial improvements	6/2/14
10	• Added details of Equaliser operation and control: Mode register, programming block • Added details of programming block read mechanism (Available for selected programming registers only) • Updated receive performance curves • Added details of bus hold function for unused inputs • Added details of Core regulator select • Corrected conditions under which current measurements were made • Changed reference to input impedance of I,QINPUTs • Typos/clarifications	6/1/12
9	• Advice in section 5.5 greyed out as not implemented in current FI.	22/08/11
8	• Added advice about terminating unconnected GPIO pins in section 5.5	17/8/11
7	• Added details of default and inverting gains to the description of the I Q Output Control - $5D, $5E registers • Pointed out correct use of handshaking when using signal control (Register $61) to select I and Q offset measurements (Registers $75 and $76) • Clarified behaviour of the I and Q offset registers (Rx dc offset correction) when using automatic Rx IQ dc mode • Clarified behaviour and scaling of RSSI measurements • Documented further AGC controls added in FI-4.0.5.4, and described AGC operation in detail • Documented the Pll On bit added to the mode register in FI-4.0.5.4, which provides a fast idle mode for programming register modifications without powersave, but with improved speed • Added parameters in Program Block 1 to reduce delay when transitioning from Idle to Tx or Rx modes • Added information about receive dynamic range • Corrected and clarified scaling of Tx output fine control.	3/8/11

6	• Remove information indicating that a reset with no FI load is possible. See sections 10.1.1 Reset Operations, 7.3 Function image loading • FIFO level interrupts to the host require re-arming using $50 FIFO control. See 10.1.4 FIFO Control $50 • Include description for "I/Q Input dc correction loop gain". See 10.1.10 Signal control $61 • Spectrum figure ACP mislabeled as for 25kHz when it is for 12.5kHz • Include over-air symbol sequence for FI-4 data. See 7.4.15, 10.1.3 and 10.1.26. Specifically this matters for bit wise transfers, indicating which bits are valid • Default values in 10.1.9 to be changed: $07FF becomes $0400; $0801 becomes $0C00 • Addition of "Tx Done flag set on completion of DC Calibration" to 7.4.11, 10.1.18 and 10.1.36. Also indicated that AuxADC paths, etc in 7.4.11 are fixed permanently, by changing the description "assumed" to "required" • Figure 27 to show "Main PLL out" sourced directly from the Xtal in Idle mode • Update Figure 3	12/4/11
5	• Add descriptions for Program Blocks 8 and 9 • Clarify text at the end of section 11.2.2 • Change b11 to b9 in section 10.1.14 • Remove FI Load Activation Block references and describe default states in section10.1.2 • Clarify bit names in section 10.1.20, to avoid duplication • Add missing action #20 in section 10.2.1 • Add details of the method of programming the lower part of the Rx I/Q dc offset ($5F,$60) • Simplify the detail of the system clock architecture • Describe RRC α=0.2/0.35 option • Added programmable filter option (details on request) • Update I/Q output reconstruction filter Capacitor values to be preferred values	21/3/11
4	• Clarified the structure of words put into the Modem Command FIFO • Revised recommended crystal tolerance • Revised C-BUS clock rate • Revised current drawn by AuxDACs • Clarify maximum input signal levels • Improved programming register settings determining baud rate resulting in improved adjacent channel performance (P1.0-P1.6). • Improved consistency of naming of signals and registers within the document and when compared to other CML devices. Notably AuxADC/DAC are now numbered 1-4 • Added detail for new FI feature: Tx DC calibration when attached to a CMX998 • Added detail for new FI feature: Discard symbol count which allows modulation to begin earlier than it would otherwise. • Many editorial changes	6/12/10
3	• Added Output dc offset lower part control to registers $5D, $5E • Changed default GPIO and RAMDAC setup to manual • Added Reg Done Select register ($69) and changed to description of PRG flag to be a type of “Reg Done” • Corrections to Boot description • Corrected several minor typographical and presentational errors.	27/9/2010

2	• Correction to power supply and de-coupling schematic (Figure 3). • Corrected rate documentation error (table in section 8.1). • Improved presentation of V_{BIAS} and its connections (sections 3, 9.1.3, 10.1.23, etc). • Corrected Xtal tolerance specification (now 20ppm recommended). • Updated parametric specifications (sections 9.1.2, 9.1.3 and 9.1.4) following further device characterisation. • Corrected bit description error in section 10.1.5. • Correction of FS Found description in section 10.1.25 • Clarify description of Preamble/Tail configuration and operation (section 10.2.5 Program Block 3). • Updated the Rx and Tx examples in sections 11.5 and 11.6 • Corrected several minor typographical and presentational errors.	1/9/2010
1	• Original document, prepared for first alpha release of FI.	30/4/2010

2 Block Diagrams

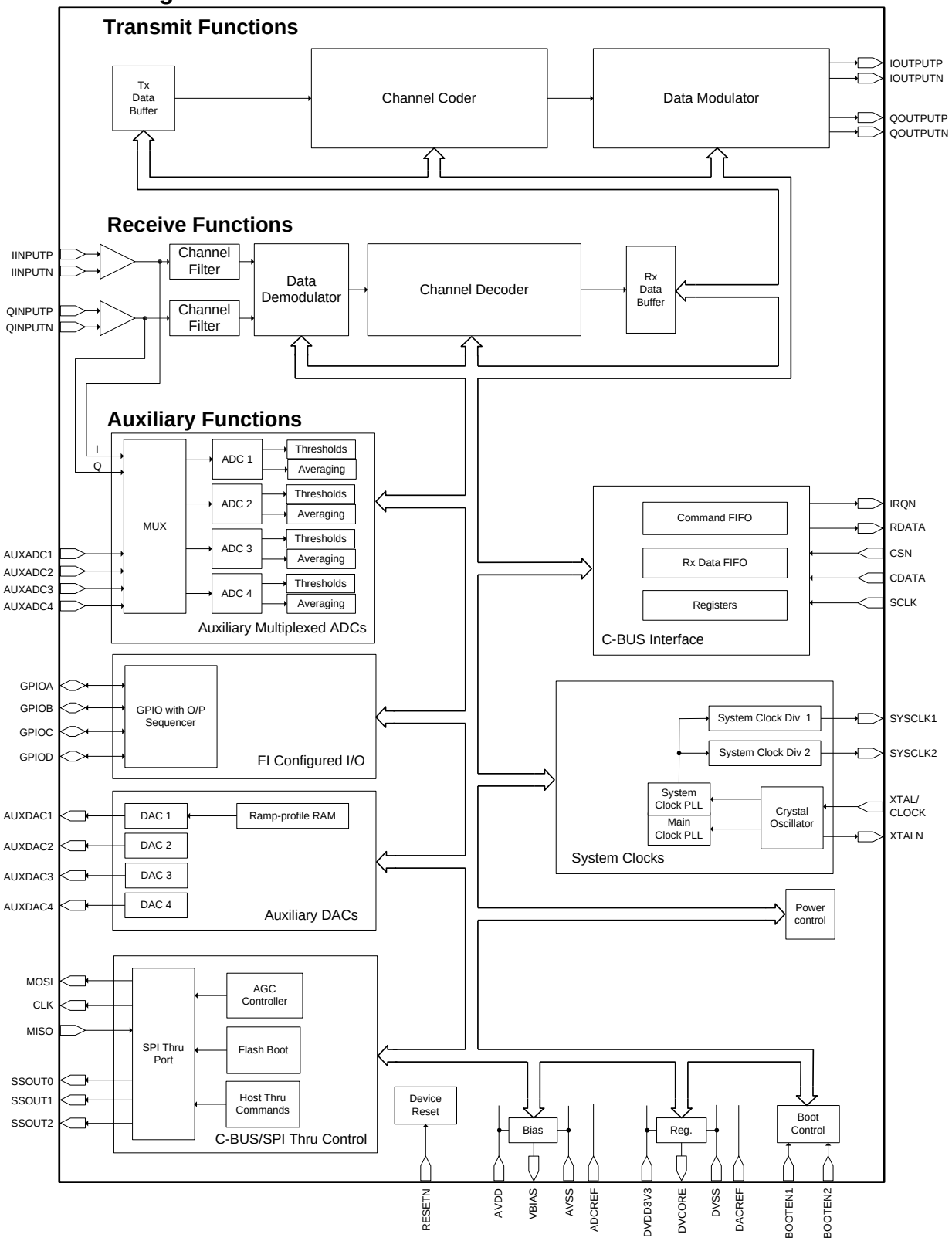


Figure 1 Overall Block Diagram

Figure 1 illustrates the overall functionality of the CMX7163, detailing the auxiliary functions. The following figure expands upon the transmit and receive functions.

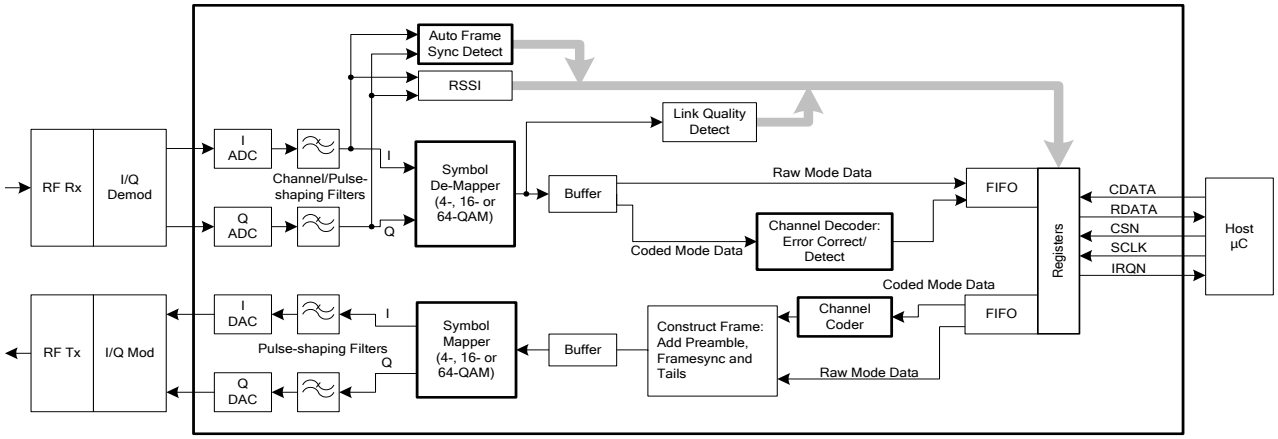


Figure 2 FI-4.x Block Diagram – I/Q Tx and Rx

3 Signal List

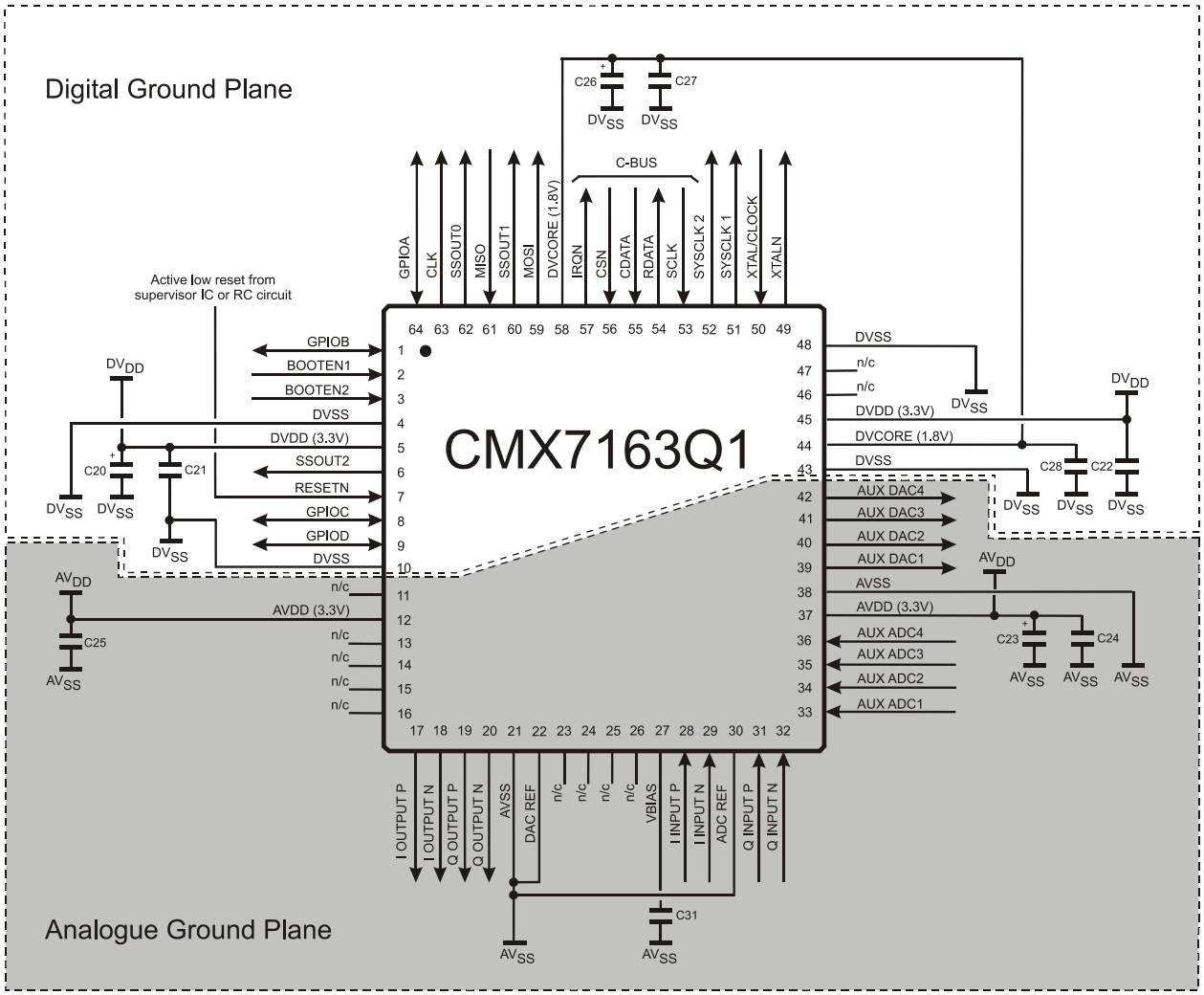
64-pin Q1/L9	Signal		Description
Pin No.	Name	Type	
1	GPIOB	BI	General Purpose I/O
2	BOOTEN1	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
3	BOOTEN2	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
5	DVDD 3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
6	SSOUT2	OP	SPI: Slave Select Out 2
7	RESETN	IP	Logic input used to reset the device (active low)
8	GPIOC	BI	General Purpose I/O
9	GPIOD	BI	General Purpose I/O
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
11	NC	NC	Do not connect
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
13	NC	NC	May also be connected to AVSS
14	NC	NC	Do not connect
15	NC	NC	Do not connect
16	NC	NC	May also be connected to AVDD
17	IOUTPUTP	OP	Differential outputs for I channel; ‘P’ is positive, ‘N’ is negative. Together these are referred to as the I Output.
18	IOUTPUTN	OP	
19	QOUTPUTP	OP	Differential outputs for Q channel; ‘P’ is positive, ‘N’ is negative. Together these are referred to as the Q Output.
20	QOUTPUTN	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF		DAC reference voltage, connect to AVSS
23	NC	NC	Do not connect
24	NC	NC	Do not connect
25	NC	NC	Do not connect
26	NC	NC	Do not connect

64-pin Q1/L9 Pin No.	Signal Name	Signal Type	Description
27	VBIAS	OP	Internally generated bias voltage of approximately AVDD/2. If VBIAS is powersaved this pin will be connected via a high impedance to AVDD. This pin must be decoupled to AVSS by a capacitor mounted close to the device pins.
28	IINPUTP	IP	Differential inputs for I channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the I Input.
29	IINPUTN	IP	
30	ADCREF		ADC reference voltage; connect to AVSS
31	QINPUTP	IP	Differential inputs for Q channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the Q Input.
32	QINPUTN	IP	
33	AUXADC1	IP	Auxiliary ADC input 1
34	AUXADC2	IP	Auxiliary ADC input 2
35	AUXADC3	IP	Auxiliary ADC input 3
36	AUXADC4	IP	Auxiliary ADC input 4
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits.
39	AUXDAC1	OP	Auxiliary DAC output 1 (Optionally the RAMDAC output)
40	AUXDAC2	OP	Auxiliary DAC output 2
41	AUXDAC3	OP	Auxiliary DAC output 3
42	AUXDAC4	OP	Auxiliary DAC output 4
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
44	DVCORE	PWR	Digital core supply, nominally 1.8V. By default this will be supplied by an on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins. For details see programming register P1.19 in section in 10.2.3 Program Block 1 – Clock Control.
45	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
46	NC	NC	Do not connect
47	NC	NC	May also be connected to DVSS
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
49	XTALN	OP	Output of the on-chip Xtal oscillator inverter
50	XTAL/CLOCK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source

64-pin Q1/L9 Pin No.	Signal Name	Signal Type	Description
51	SYSCLK1	OP	Synthesised digital clock output 1
52	SYSCLK2	OP	Synthesised digital clock output 2
53	SCLK	IP	C-BUS serial clock input from the µC
54	RDATA	TS OP	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC
56	CSN	IP	C-BUS chip select input from the µC
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DVSS when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE	PWR	Digital core supply, nominally 1.8V. Normally this will be supplied by the on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins. For details see programming register P1.19 in section in 10.2.3 Program Block 1 – Clock Control.
59	MOSI	OP	SPI: Master Out Slave In
60	SSOUT1	OP	SPI: Slave Select Out 1
61	MISO	IP	SPI: Master In Slave Out
62	SSOUT0	OP	SPI: Slave Select Out 0
63	CLK	OP	SPI: Serial Clock
64	GPIOA	BI	General Purpose I/O
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on the Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

Notes:
IP = Input (+ PU/PD = internal pull-up / pull-down resistor of approximately 75kΩ)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

4 PCB Layout Guidelines and Power Supply Decoupling



C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C31	100nF
C24	10nF		
C25	10nF		

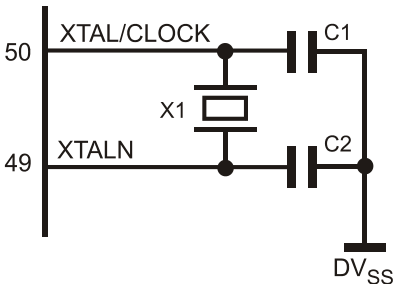
Figure 3 CMX7163 Power Supply and De-coupling

Notes:

To achieve good noise performance, V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7163 area to provide a low impedance connection between the VSS pins and the V_{DD} and V_{BIAS} decoupling capacitors.

5 External Components

5.1 Xtal Interface



X1 For frequency range see 9.1.2 Operating Limits
C1 22pF Typical
C2 22pF Typical

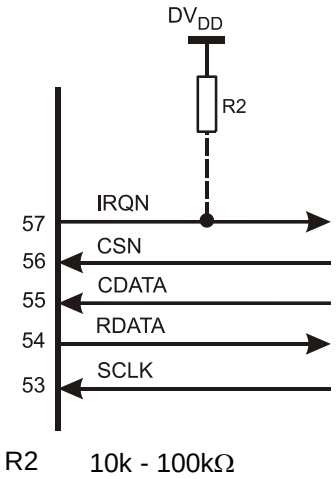
Figure 4 Recommended External Components – Xtal Interface

Notes:
The clock circuit can operate with either a Xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLOCK pin and the xtal and other components are not required. For external clock generator frequency range see 9.1.2 Operating Limits. When using an external clock generator the Xtal oscillator circuit may be disabled to save power, see 10.2.3 Program Block 1 – Clock Control for details. Also refer to section 7.1 Xtal Frequency.

The tracks between the Xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the Xtal capacitors and the ground plane.

The DV_{SS} to the Xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. For correct values of capacitors C1 and C2 refer to the documentation of the Xtal used.

5.2 C-BUS Interface



R2 10k - 100kΩ

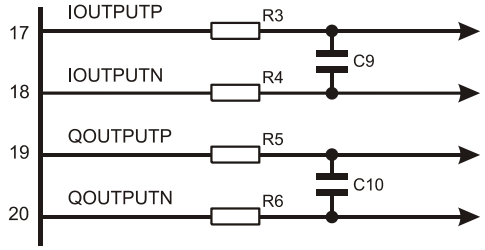
Figure 5 Recommended External Components – C-BUS Interface

Note:
If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 I/Q Output Reconstruction Filter

The CMX7163 I/Q Outputs provide internal reconstruction filtering with four selectable bandwidths (-3dB point shown in section 10.1.22). The bandwidth of the internal reconstruction filter may be selected using the I/Q Output Configuration - $B3 write or Signal Control - $61 write registers.

To complete the I/Q output reconstruction filter one of the following external RC networks should be used for each of the differential outputs. The external RC network should have a bandwidth that matches the bandwidth of the selected internal reconstruction filter.



Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
100	22	33
50	20	75
25	22	150
12.5	22	270

Figure 6 Recommended External Components – I/Q Output Reconstruction Filter

When transmitting an I/Q signal, each I/Q Output will produce a signal with bandwidth half the channel bandwidth. A reconstruction filter with a –3dB point close to half the channel bandwidth will therefore have significant roll off within the channel bandwidth – which is undesirable. An appropriate choice for channels occupying up to a 25kHz bandwidth (channel bandwidth/2 = 12.5kHz) would be a reconstruction filter of 25kHz bandwidth.

5.4 I/Q Input Antialias Filter

The device has a programmable antialias filter in the I/Q input path, which is controlled using the I/Q Input Configuration - $B0 write or Signal Control - $61 write registers. This should be sufficient for most applications, however if additional filtering is required it can be done at the input to the device.

The input impedance of the I/Q Input pins varies with the input gain setting, see section 9.1.3 Operating Characteristics.

5.5 GPIO Pins

All GPIO pins are configured as inputs with an internal bus-hold circuit, after the Function Image™ has been loaded. This avoids the need for users to add external termination (pullup/pulldown) resistors onto these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using programming register P1.20 in Program Block 1 – Clock Control.

If the device is reset (either by asserting RESETN pin 7, issuing a C-BUS General RESET or by triggering an internal power on reset) all GPIO pins will be immediately configured as inputs. Any GPIO pins not being pulled either up or down by an external load will be left in a floating state until the Function Image™ is loaded. To avoid GPIO floating input states that may somewhat elevate supply current between a RESET and Function Image™ load, it will be necessary to connect pull up or pull down resistors of 220kΩ to these pins.

6 General Description

6.1 CMX7163 Features

The CMX7163 is intended for use in half-duplex modems. Transmission takes the form of a data burst consisting of preamble, frame sync and data payload, followed by a tail sequence. Reception may utilise the preamble to assist with signal acquisition[1], but is then followed by frame sync detection and data decoding.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a Xtal clock generator, with phase locked loop and buffered output, to provide a System Clock output, if required, for other devices.

Block diagrams of the device are shown in section 2, Block Diagrams.

Tx Functions:

- Automatic preamble and frame sync insertion simplifies host control
- I/Q analogue outputs
- Pulse shape filtering
- RAMDAC capability for PA ramping control
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramp and Tx hardware switching
- Carrier sense for “listen before talk” operation
- Raw and formatted (channel coded) data modes
- Flexible Tx coded data block size, up to 416 bytes

Rx Functions:

- Automatic frame sync detection simplifies host control
- I/Q analogue inputs
- Rx channel filtering and pulse shape filtering
- Channel estimation and equalisation
- Tracking of symbol timing and input I/Q dc offsets
- AGC using SPI Thru-Port
- Raw and formatted (channel coded) data modes
- Flexible Rx coded data block size, up to 416 bytes

Auxiliary Functions:

- Two programmable system clock outputs
- Four auxiliary ADCs with six selectable input paths
- SPI Thru-Port for interfacing to synthesisers, Cartesian loop IC (CMX998) and other serially controllable devices
- In-build calibration routine to support CMX998 Cartesian Loop transmitter IC
- Four auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer
- Open drain IRQ to host
- Four GPIO pins
- Tx trigger input (Provided by GPIOA)
- Serial memory or C-BUS (host) boot mode

[1] The frame sync detection algorithm of the CMX7163 is capable of detecting a frame sync without having bit synchronisation, so preamble is not required for obtaining bit sync. Some preamble is still needed to ensure that the beginning of the frame sync is transmitted and received without distortion. Preamble may also be used to provide a known signal on which to acquire I/Q dc offset corrections.

Both transmit and receive data can be raw or coded data blocks. FI-4.x provides a variety of coding rates for flexibility and very large block sizes having the potential to improve performance in fading conditions considerably.

6.2 Signal Interfaces (I/Q Tx and Rx)

FI-4.x produces QAM modulation. The transmitted signal is provided as an I/Q baseband, for mixing up onto an RF carrier, with amplification. For reception an I/Q baseband signal should be interfaced into the CMX7163 FI-4.x.

As the I/Q interface provides amplitude information, the RSSI signal is calculated internally. It is averaged in order to produce the RSSI measurement and to support the carrier sense decision whether to transmit.

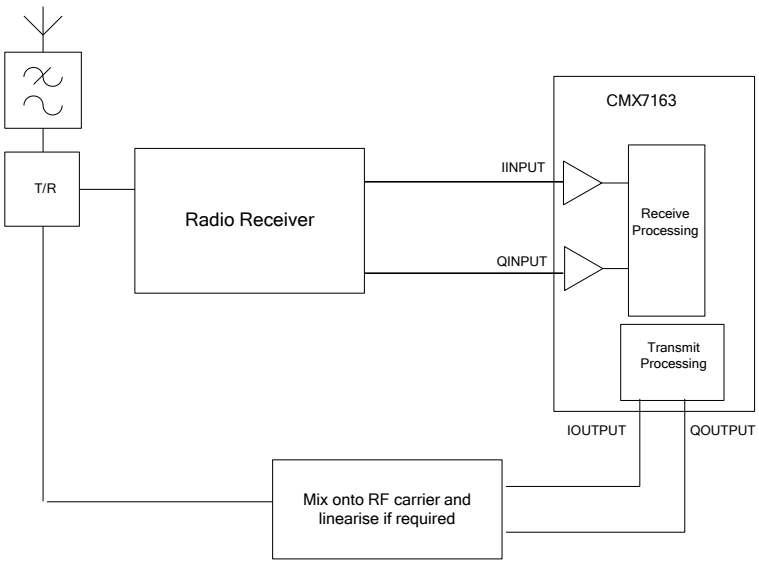


Figure 7 CMX7163 I/Q Tx, I/Q Rx

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7163 is designed to work with a Xtal, or an external frequency oscillator within the ranges specified in section 9.1.3 Operating Characteristics. Program Block 1 (see User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of configuration values can be found in Table 8 supporting baud rates up to 20k symbols per second when the Xtal frequency is 9.6MHz or the external oscillator frequency is 9.6 or 19.2 MHz. Rates other than those tabulated (within this range) are possible, see section 10.2.3 Program Block 1 – Clock Control. Further information can be provided on request. The modem can operate with a clock or Xtal input frequency tolerance of 50ppm. The receive performance will be compromised as the system tracks, so a maximum tolerance of 20ppm is recommended.

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7163 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred; the µC should read the IRQ Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Interrupt Operation.

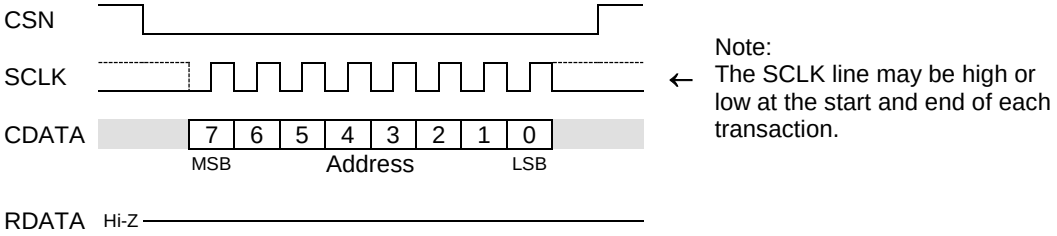
7.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7163 internal registers and the host µC over the C-BUS serial bus. Single register transactions consist of a single register address byte sent from the µC, which may be followed by a data word sent from the µC to be written into one of the CMX7163's write-only registers, or a data word read out from one of the CMX7163's read-only registers. Streaming C-BUS transactions consist of a single register address byte followed by many data bytes being written to or read from the CMX7163. All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 8.

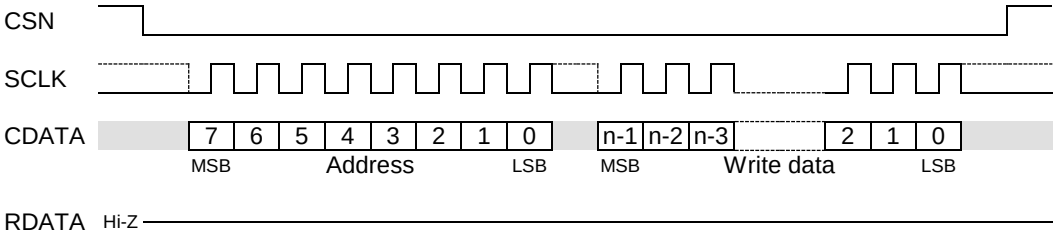
Data sent from the µC on the CDATA (command data) line is clocked into the CMX7163 on the rising edge of the SCLK input. Data sent from the CMX7163 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Section 9.2 C-BUS Timing gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

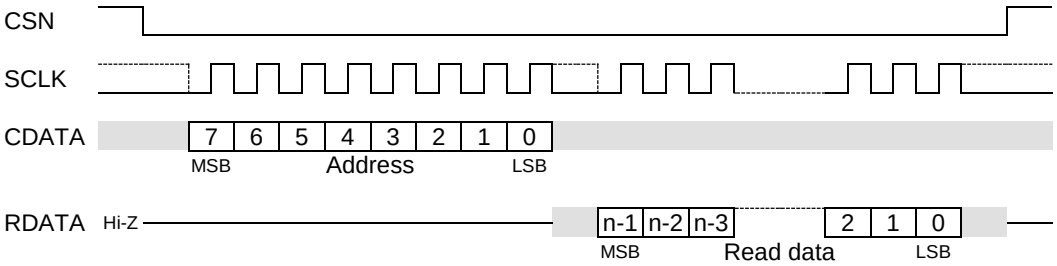
C-BUS single byte command (no data)



C-BUS n-bit register write



C-BUS n-bit register read



Data value unimportant

Repeated cycles

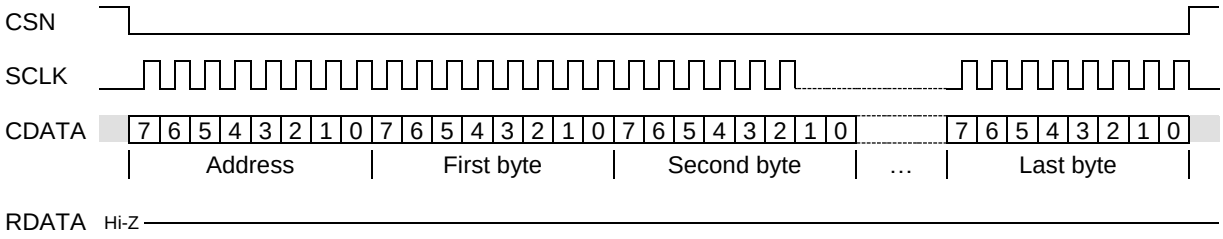
Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 8 Basic C-BUS Transactions

To increase the data bandwidth between the µC and the CMX7163, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 9.

Example of C-BUS data-streaming (8-bit write register)



Example of C-BUS data-streaming (8-bit read register)

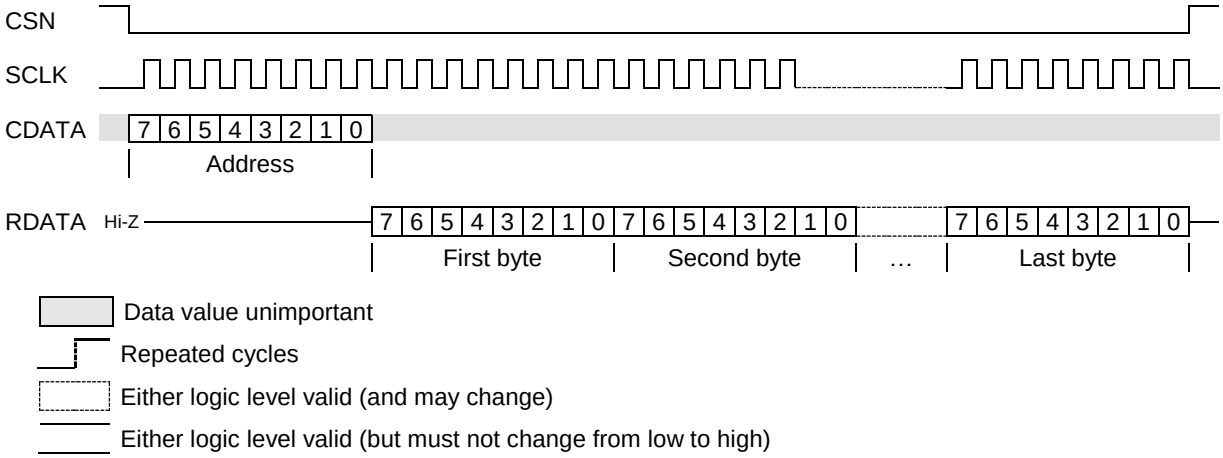


Figure 9 C-BUS Data Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The Function Image™ size can never exceed 128 kbytes, although a typical FI will be considerably less than this. Note that the BOOTEN1/2 pins are only read at power-on, when the RESETN pin goes high, or following a C-BUS General Reset, and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN1/2 pins are ignored by the CMX7163 until the next power-up or Reset.

The BOOTEN1/2 pins are both fitted with internal low current pull-up devices.

For serial memory load operation, BOOTEN2 should be pulled low by connecting it to DV_{SS} either directly or via a 47k resistor (see Table 1).

Whilst booting the boot loader will return the checksum of each block loaded in the C-BUS Rx Data FIFO. The checksums can be verified against the published values to ensure that the FI has loaded correctly.

Once the FI has been loaded, the CMX7163 performs these actions:

(1) The product identification code ($7163) is reported in the C-BUS Rx Data FIFO
(2) The FI version code is reported in C-BUS Rx Data FIFO.

Table 1 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
reserved	1	0
Serial Memory load	0	1
reserved	0	0

7.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7163 at power-up over the C-BUS interface, using the Command FIFO. For Function Image™ load, the FIFO accepts raw 16-bit Function Image™ data (using the Modem Command FIFO Word) - $49 write register, there is no need for distinction between control and data fields. The BOOTEN1/2 pins must be set to the C-BUS load configuration, the CMX7163 powered or Reset, and then data can then be sent directly over the C-BUS to the CMX7163.

If the host detects a brownout, the BOOTEN1/2 pins should be set to re-load the FI. A General Reset should then be issued or the RESETN pin used to reset the CMX7163 and the appropriate FI load procedure followed.

Streaming C-BUS may be used to load the Modem Command FIFO Word - $49 write register with the Function Image™, and the Modem Command FIFO Level - $4B read register used to ensure that the FIFO is not allowed to overflow during the load process.

The download time is limited by the clock frequency of the C-BUS; with a 5MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

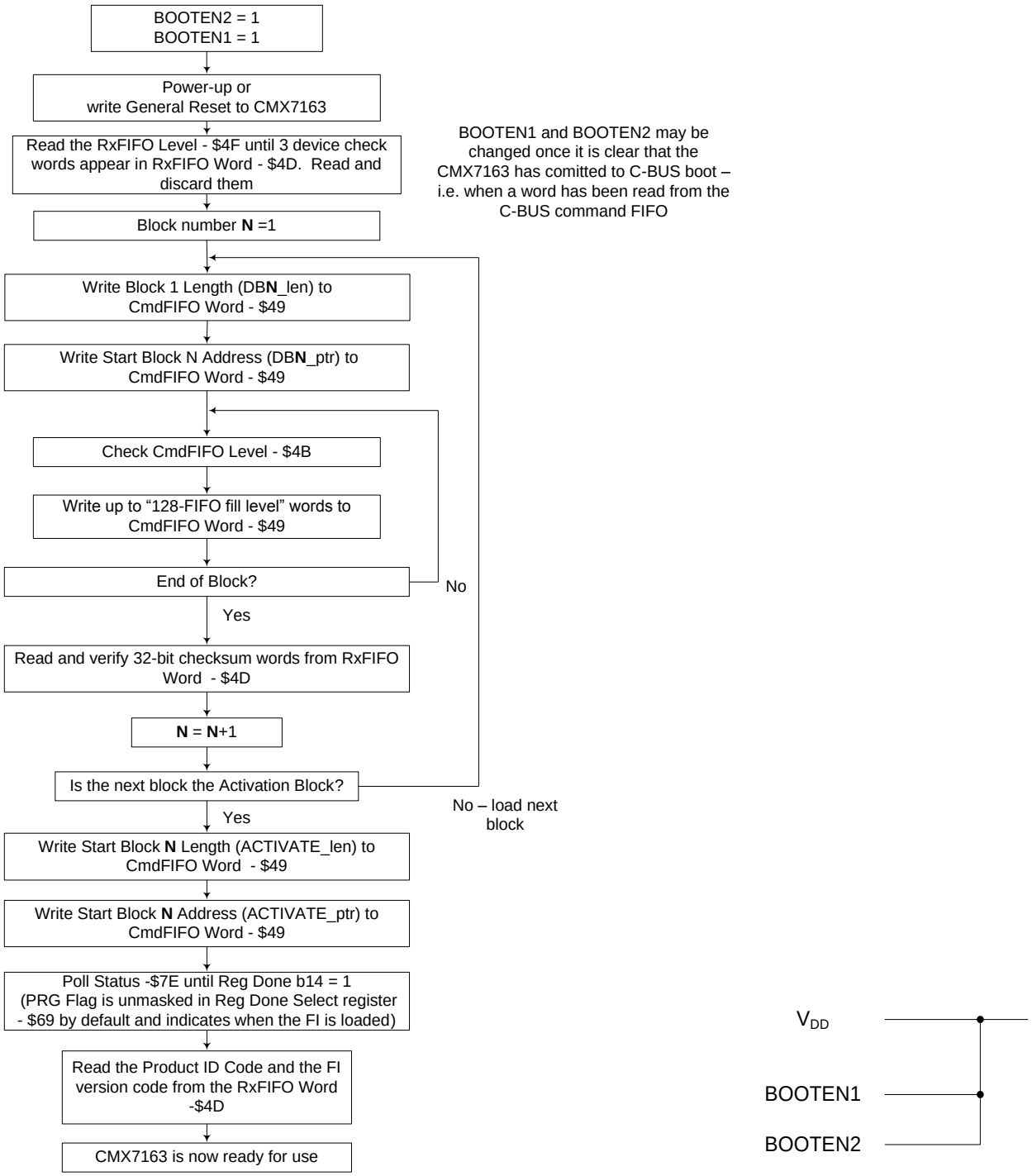


Figure 10 FI Loading from Host

7.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The serial memory should contain the same data stream as written to the Command FIFO shown in Figure 10. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7163 SPI Thru-Port using SSOUT0 as the chip select. The CMX7163 needs to have the BOOTEN pins set to Serial Memory Load, and then on power-on, following the RESETN pin becoming high, or following a C-BUS General Reset, the CMX7163 will automatically load the data from the serial memory without intervention from the host controller.

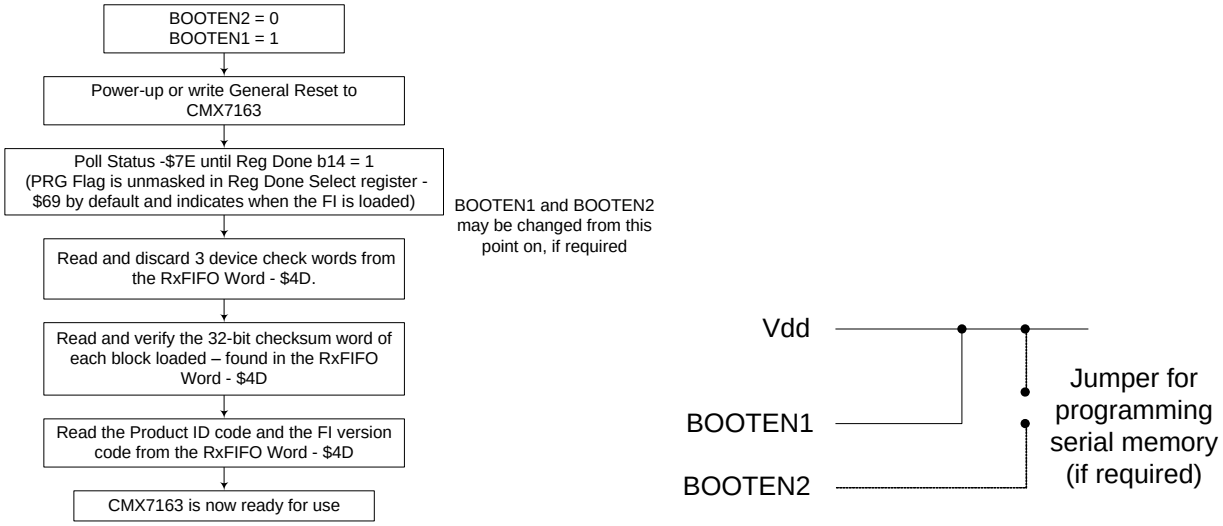


Figure 11 FI Loading from Serial Memory

The CMX7163 has been designed to function with the AT25F512 serial flash device, however other manufacturers' parts may also be suitable. The time taken to load the FI should be less than 500ms even when loading the largest possible Function Image™.

7.4 Device Control

Once the Function Image™ is loaded the CMX7163 can be set into one of four main modes using the Modem Mode and Control - $6B write register:

- Idle mode – for configuration or low power operation
- Transmit mode – for transmission of raw or formatted data
- Receive mode – for detection and reception of bursts containing raw or formatted data
- Carrier sense mode – for attempting to transmit if the channel is free, otherwise continuing to receive

These four modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers in transmit, receive and carrier sense modes or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in Idle mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. Additional power-saving can be achieved by disabling unused hardware blocks, however, most of the hardware power-saving is automatic. Note that V_{BIAS} must be enabled to allow any of the Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- 10.1.17 Programming Register - $6A write
- 10.1.18 Modem Mode and Control - $6B write
- 10.2 Programming Register Operation
- 10.1.24 VBIAS Control - $B7 write.

7.4.1 Normal Operation Overview

In normal operation (after the CMX7163 is configured) the appropriate mode must be selected and data provided in transmit or retrieved in receive. This process is carried out by selecting the mode (Tx, Rx or Carrier Sense), selecting the frame sync to use (Frame Sync 1 or 2) and selecting formatted or raw data. Such a selection is required at the beginning of transmission or reception of a burst.

In transmit (or following a carrier sense period where no signal is detected on channel) the CMX7163 will begin by switching GPIO signals as configured by the transmit sequence. The RAMDAC can also be configured to ramp up at this point. Transmission then begins with preamble and the selected frame sync. The main payload of user data comes next, ending with selectable tail bits. The burst ends with the transmission sequence ramping the RAMDAC down and/or switching GPIO signals.

In receive (or following a carrier sense period where signal is detected on channel) the CMX7163 will begin by searching for either or both of the configured frame sync patterns. On detection of a frame sync, reception and delivery of Rx data will begin. Reception continues until the CMX7163 is switched into a different mode, determined by the host.

During the burst, data must be transferred into or out of the CMX7163. Transfers use the Command FIFO to transfer data and commands about data type into the CMX7163, and the Rx FIFO to transfer data out of the CMX7163. The IRQ Status register is used to indicate that the data has been dealt with. The CMX7163 can be configured to interrupt the host when a specified data block has been transferred, or on FIFO fill level.

The CMX7163 offers internal buffering of data in addition to the Command and Rx FIFOs in both receive and transmit directions. The amount of buffering offered is dependant on the mode in which the device is operating. In the process of burst transmission or reception the most significant registers are:

- 10.1.18 Modem Mode and Control - $6B write
- 10.1.37 IRQ Status - $7E read
- 10.1.19 IRQ Mask - $6C write
- 10.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 10.1.26 Receive FIFO Data/Control - $4C, $4D, $4E read
- 10.1.25 Modem Command FIFO Level - $4B read
- 10.1.27 Receive FIFO Level - $4F read.

7.4.2 Basic Tx and Rx Operation

The CMX7163 has many features that provide a great deal of flexibility, but basic data transmission and reception can be carried out fairly easily by understanding the operation of just a few registers. There are other ways of controlling signal transmission and reception but a basic example is given below:

Basic Transmit Operation

Transmission of raw data bytes uses the following procedure:

C-BUS Operation	Action	Description
Write $0080 to FIFO Control - $50 write	Flush the Command FIFO	To ensure that no data is remaining from previous transmissions
Write $18 to the Modem Command FIFO Control Byte (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Select 8 byte data blocks	Selects blocks of data bytes to be transmitted – 8 bytes in each, after which the CMX7163 will request more data from the host
Write 8 data bytes to the Modem Command FIFO Data Byte - see Modem Command FIFO Data/Control - $48, $49 and $4A write	Pre load the Command FIFO with data to transmit	This provides a buffer of 8 data bytes before transmission starts, so that the host does not need to write data as promptly for the rest of the burst
Write $0042 to Modem Mode and Control - $6B write	Start transmission	Initiates a transmission with preamble, Frame Sync 1 and then the pre loaded data
Poll the IRQ Status - $7E read register for bit 8 – Cmd Done = 1	Wait until the data block has been read from the FIFO	When this is complete a further 8 data bytes may be written to the Modem Command FIFO Data Byte (see Modem Command FIFO Data/Control - $48, $49 and $4A write) and the IRQ Status - $7E read register polled again. This step may be repeated as many times as needed
Write $F000 to the Modem Command FIFO Word (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Indicate burst end is intended	Indicate that no more data is to follow – so when the data loaded into the Command FIFO is modulated the CMX7163 will terminate the burst with tail bits
Poll the IRQ Status - $7E read register for bit 9 – Tx Last Tail = 1	Wait until the burst ends	The burst has completed, with all data and tail bits having been modulated. It is now possible to transition to other modes, or transmit another burst using the Modem Mode and Control - $6B write register

The procedure described above can be adapted, making transmission of different numbers of bytes, bits or coded blocks possible.

Basic Receive Operation

Reception of raw data bytes uses the following procedure:

C-BUS Operation	Action	Description
Write $8000 to FIFO Control - $50 write	Flush the Command FIFO	To ensure that no data is remaining from previous data reception
Write $1400 to the Modem Command FIFO Word (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Select 4 byte data block reception – repeat forever	Selects blocks of data bytes to be received (after frame sync is detected) – 4 bytes in each, at which point the host will be notified. This will continue until the mode is changed

C-BUS Operation	Action	Description
Write $0033 to Rx Tracking - $66 write	Select tracking modes	Selects automatic I/Q dc offset correction and symbol timing tracking
Write $0401 to Modem Mode and Control - $6B write	Start reception	Initiates a frame sync search, searching for Frame Sync 1. Once it is detected then Rx data will be made available
-	Apply input signal	The input signal should contain preamble, Frame Sync 1 and then raw data. The frame sync should be detected and Rx data made available
Poll the IRQ Status - $7E read register for bit 8 – Cmd Done = 1	Wait for data	This indicates that the 4 data bytes requested have been received and are available
Read the Receive FIFO Data Byte (see Receive FIFO Data/Control - $4C, $4D, $4E read) 4 times	Retrieve the received data	Data is read from the Receive Data FIFO. Once 4 data bytes are read the IRQ Status register may be polled again to check if more data is available if required, and then those data bytes read. This step may be repeated as many times as needed
-	End of reception	Once enough data has been received a mode change (using the Modem Mode and Control - $6B write register) will stop reception or start searching for another frame sync

The procedure described above can be adapted, making reception of different numbers of bytes, bits or coded blocks possible.

The registers used for basic transmission and reception are:

- 10.1.18 Modem Mode and Control - $6B write
- 10.1.37 IRQ Status - $7E read
- 10.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 10.1.26 Receive FIFO Data/Control - $4C, $4D, $4E read
- 10.1.4 FIFO Control - $50 write
- 10.1.15 Rx Tracking - $66 write

7.4.3 Device Configuration (Using the Programming Register)

While in Idle mode the Programming register becomes active. The Programming register provides access to the Program Blocks. Program Blocks allow configuration of the CMX7163 during major mode change. Features that can be configured include:

- Flexible selection of Baud rates, from 2k to 20k baud
- Pre-amble and frame syncs to be using in transmit and receive
- Selection of Automatic control of 4 x GPIO and the RAMDAC during transmission
- Configuration of RAMDAC profile
- Configuration of RSSI averaging
- Configuration of the carrier sense window and thresholds
- Configuration of System Clock outputs
- Configuration of SPI Thru-Port rate and word format
- Configuration of AGC commands using the SPI Thru-Port.

Full details of how to configure these aspects of device operation are given in section 10.2 in the User Manual.

7.4.4 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of Idle mode. Configuration of the following features is possible:

- Auxiliary ADC detect thresholds
- Auxiliary ADC input selection and averaging mode
- Output gain
- Output dc offsets
- Selection of AGC mode, or manual control of the gain level.

The registers that allow configuration of these features are:

- 10.1.8 I/Q Output Control - $5D, $5E write
- 10.1.9 I/Q Input Control - $5F, $60 write
- 10.1.21 I/Q Input Coarse Gain - $B1, $B2 write
- 10.1.23 I/Q Output Coarse Gain - $B4, $B5 write
- 10.1.22 I/Q Output Configuration - $B3 write
- 10.1.20 I/Q Input Configuration - $B0 write
- 10.1.5 AuxADC1-4 Control - $51 to $54 write
- 10.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 10.1.10 Signal Control - $61 write
- 10.1.14 AGC Control - $65 write.

7.4.5 Interrupt Operation

The CMX7163 can produce an interrupt output when various events occur. Examples of such events include detection of a frame sync, an overflow of the internal data buffering in receive, or completion of transmission whilst in transmit.

Each event has an associated IRQ Status register bit and an IRQ Mask register bit. The IRQ Mask register is used to select which status events will trigger an interrupt on the IRQN line. All events can be masked using the IRQ mask bit (bit 15) or individually masked using the IRQ Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the IRQ Status register reflects the IRQN line state.

All interrupt flag bits in the IRQ Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. See:

- 10.1.37 IRQ Status - $7E read
- 10.1.19 IRQ Mask - $6C write.

7.4.6 Signal Control

The CMX7163 offers two signal inputs (I Input, Q Input), and two modulator outputs (I Output, Q Output). The analogue gain/attenuation of each input and output can be set individually.

During I/Q modulation transmit, I Output and Q Output will output in-phase and quadrature output signals. They may be independently inverted and their gains changed. During I/Q modulation receive, I Input and Q Input will accept in-phase and quadrature modulated signals. They may be independently inverted and their gains changed.

Note: When transmitting (or receiving) in I/Q mode it may be necessary to swap the I and Q signals. This effect can be achieved by negating either the I or Q signals.

See:

- 10.1.8 I/Q Output Control - $5D, $5E write
- 10.1.9 I/Q Input Control - $5F, $60 write
- 10.1.21 I/Q Input Coarse Gain - $B1, $B2 write
- 10.1.23 I/Q Output Coarse Gain - $B4, $B5 write
- 10.1.22 I/Q Output Configuration - $B3 write
- 10.1.20 I/Q Input Configuration - $B0 write.

7.4.7 Tx Mode

In typical Tx operation, the preamble and FS1 or FS2 are transmitted automatically, and then data from the Command FIFO is transmitted directly until a TxEnd command is processed or the mode is changed to Rx or Idle. Data may be written to the Command FIFO prior to starting transmission, enabling the host to create a buffer of data and therefore avoiding risk of the data running out during transmission. Further buffering is provided to expand the amount of data that may be absorbed by the CMX7163.

The host should write the initial data to the Command FIFO and then set modem control to the required transmit type with the Mode bits as Tx. As soon as the data has been read from the C-BUS TxData registers the Cmd Done IRQ and/or Command FIFO IRQ will be asserted (when configured correctly). More data should be loaded into the Command FIFO at this stage before data buffered in the CMX7163 runs out, otherwise an under-run will occur. To end the burst the host should send a TxEnd command, signalling to the CMX7163 that the burst is to end, and the imminent data under-run is intentional.

It is possible to define a transmission sequence with defined RAMDAC ramp up/down, and GPIO on/off events. The transmission sequence is configured using Program Block 5. For precise control of the instant that transmission starts it is possible to trigger a transmission using GPIOA as an input. Selecting a Tx mode with GPIOA configured as an “automatic input” places the device into a “Tx pending” state, where it is neither receiving nor transmitting, just waiting for a trigger on GPIOA to begin transmission.

In general Figure 12 describes operation when a transmit sequence is defined by the host by:

- Removing the need for the host to provide a ramp up – instead the configured Tx sequence will deal with this
- Inserting GPIO on/off events before ramp up and after ramp down as specified by the transmit sequence.

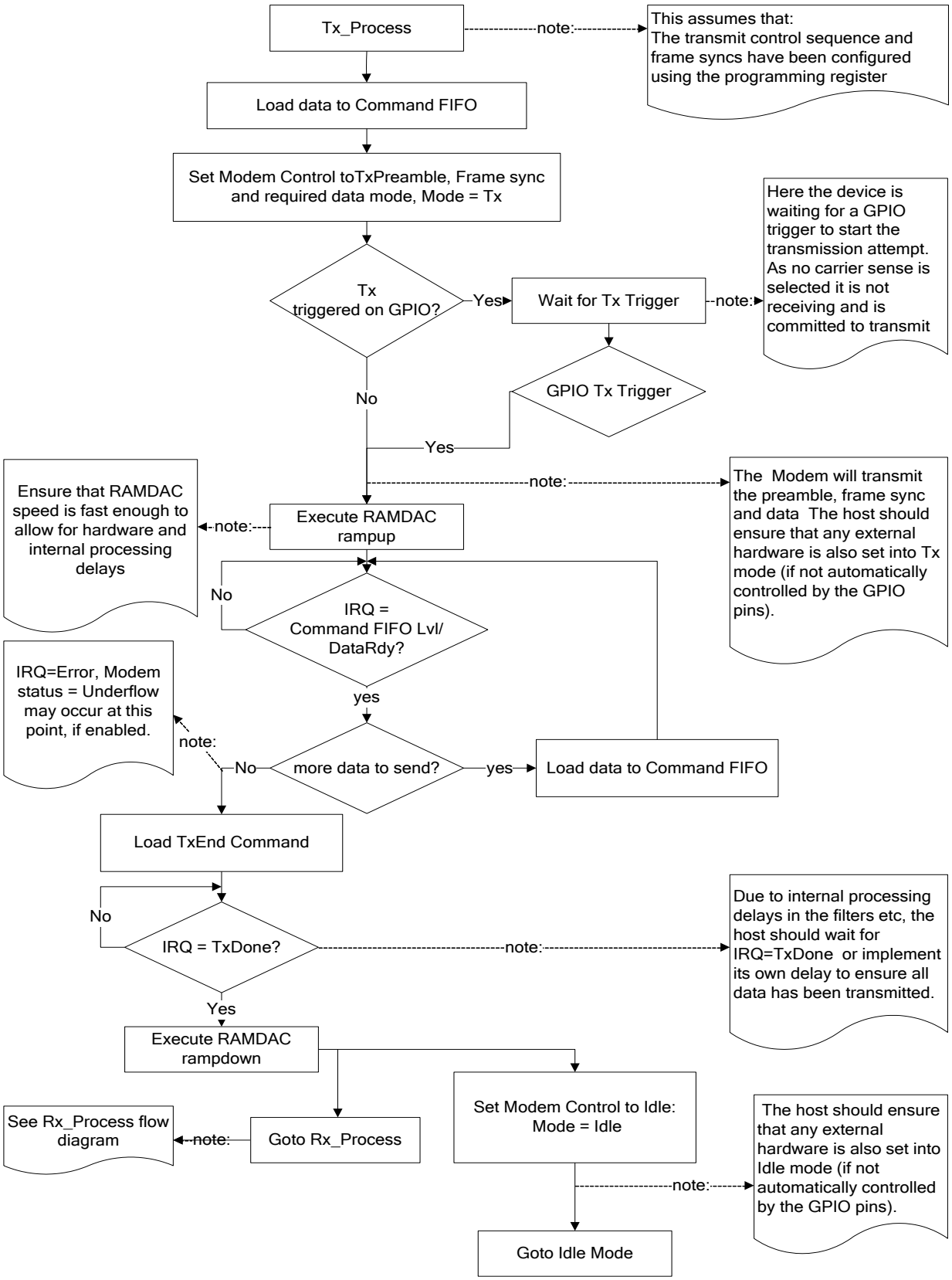


Figure 12 Host Tx Data Flow (No Tx Sequence/Carrier Sense)

7.4.8 Rx Mode

In Rx mode a frame sync must be detected, then data is supplied to the host through the Rx Data FIFO and should be read in response to a Cmd Done IRQ/Rx Data FIFO IRQs (when configured). The CMX7163 will continue decoding the input waveform until the host sets the mode bits to either Tx or Idle, as required. Once initial timing is established, timing corrections can be derived from the data to track the received signal. The Rx Tracking register allows selection of the tracking mode used to track the signal level, I/Q dc offset and symbol timing of the input signal as required. Use of the automatic tracking modes is recommended.

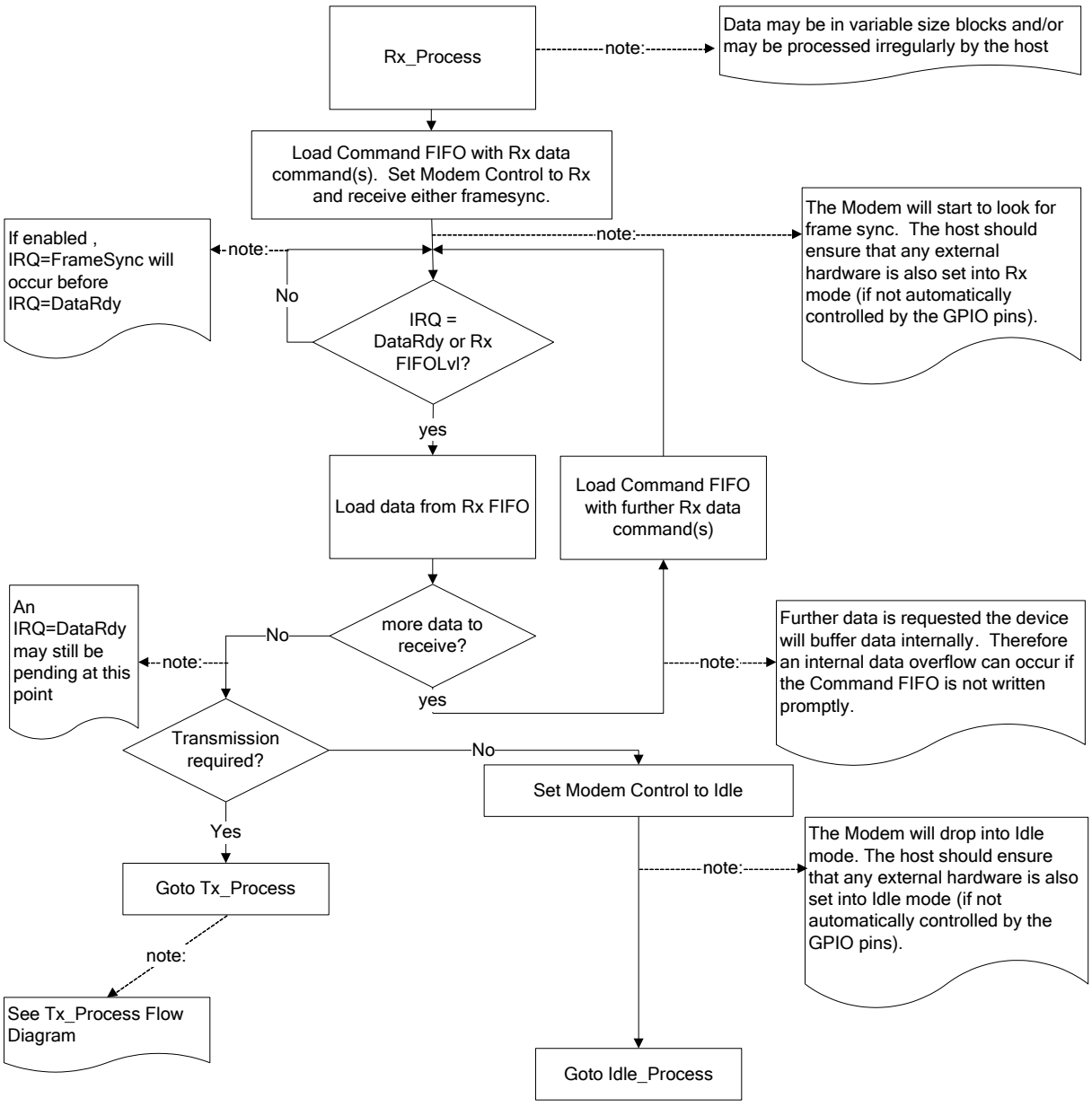


Figure 13 Host Rx Data Flow

7.4.9 Carrier Sense Mode

Carrier sense mode is a receive mode, pending a transmission. A carrier sense period, averaging window length and threshold must be defined in the Program Blocks prior to entering this mode. When the CMX7163 is in I/Q receive mode the signal strength is calculated internally – as the I/Q signal contains amplitude information.

On entry to Carrier Sense mode, reception will begin (or continue if the previous mode was receive) with an attempt to search for a frame sync. During the defined carrier sense period average RSSI will be computed over a moving window. Three outcomes are possible:

1. If during the carrier sense period the average RSSI is above the carrier sense threshold then transmission will be aborted, and search for frame sync will continue. The device reverts to receive.
2. There is a possibility that a valid frame sync will be detected during the carrier sense period. If this is the case, the transmission will be aborted immediately and the device reverts to receive.
3. If the RSSI average remains below the carrier sense threshold then transmission will proceed.

In each of the three possible cases, status bits will be used to indicate the result of the carrier sense period.

If the carrier sense mechanism is used in conjunction with GPIOA as a Tx trigger, operation is as follows: The device is put in receive, searching for a frame sync. If frame sync is found during this period then it is indicated to the host via the status bits and normal reception resumes. No carrier sense happens until GPIOA is used to start the transmit process, at which point carrier sense begins and operation is as described above.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7163 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

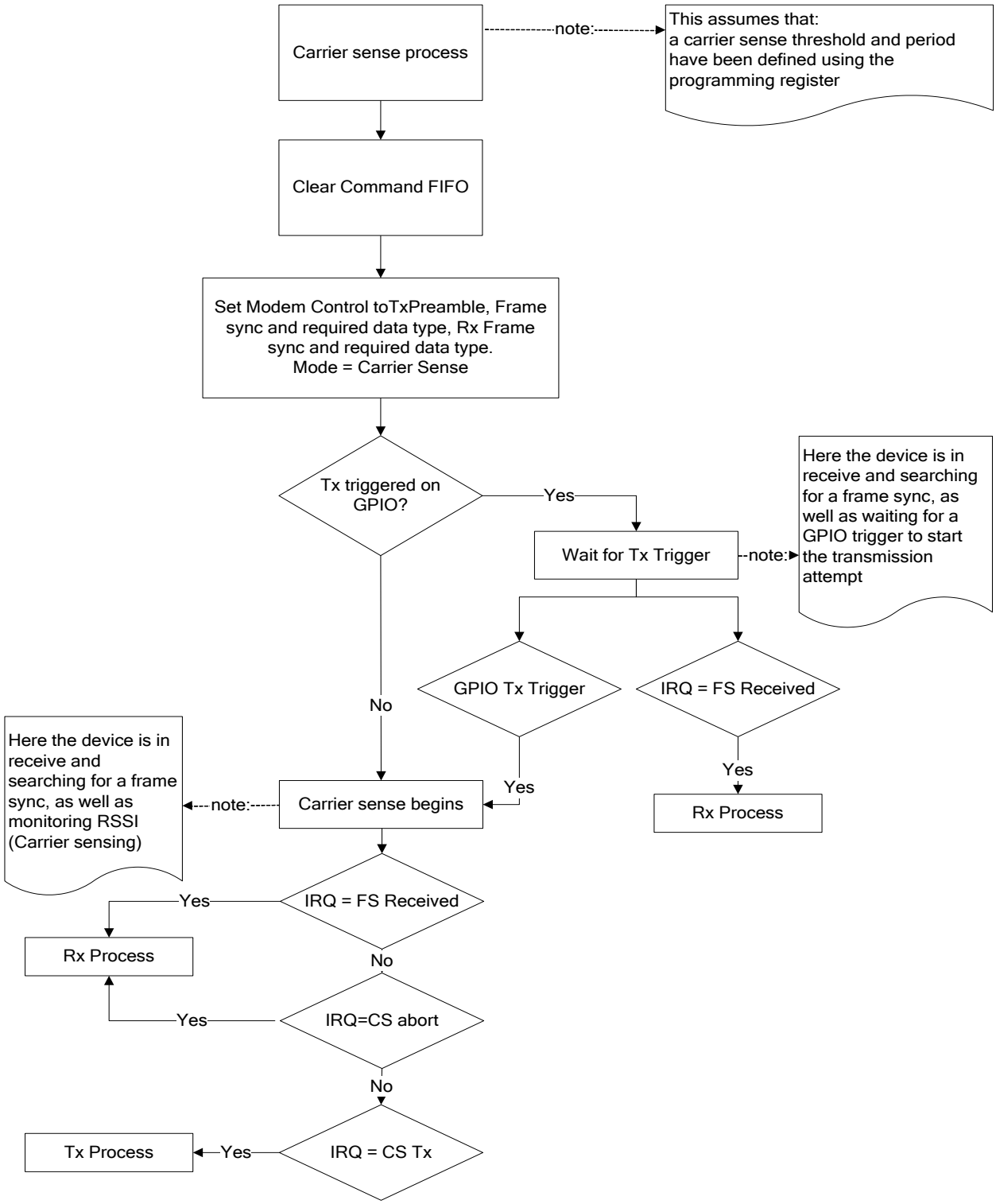


Figure 14 Carrier Sense

7.4.10 The Transmit Sequence

The CMX7163 is capable of being configured to provide the following features:

1. Selecting Tx mode results in transmission starting directly on entry to Tx mode or is delayed until GPIOA is used as an input trigger
2. Selecting carrier sense mode will result in behaviour as in point 1, followed by a carrier sense period, where transmission is delayed (reception continues) until a carrier sense period is completed and no activity is sensed on the channel
3. Selecting Tx calibration will cause CMX998 cartesian loop dc calibration to be carried out prior to transmission, as part of the programmable transmit sequence. See section 7.4.11 CMX998 DC Offset Calibration for details.
4. Once started, transmission can be configured to be a simple modulation output or can include a programmable sequence of events including RAMDAC ramp up/down and GPIO On/Off.

   Each of these operations can be selected independently of the others. The following diagram illustrates transmit operation.

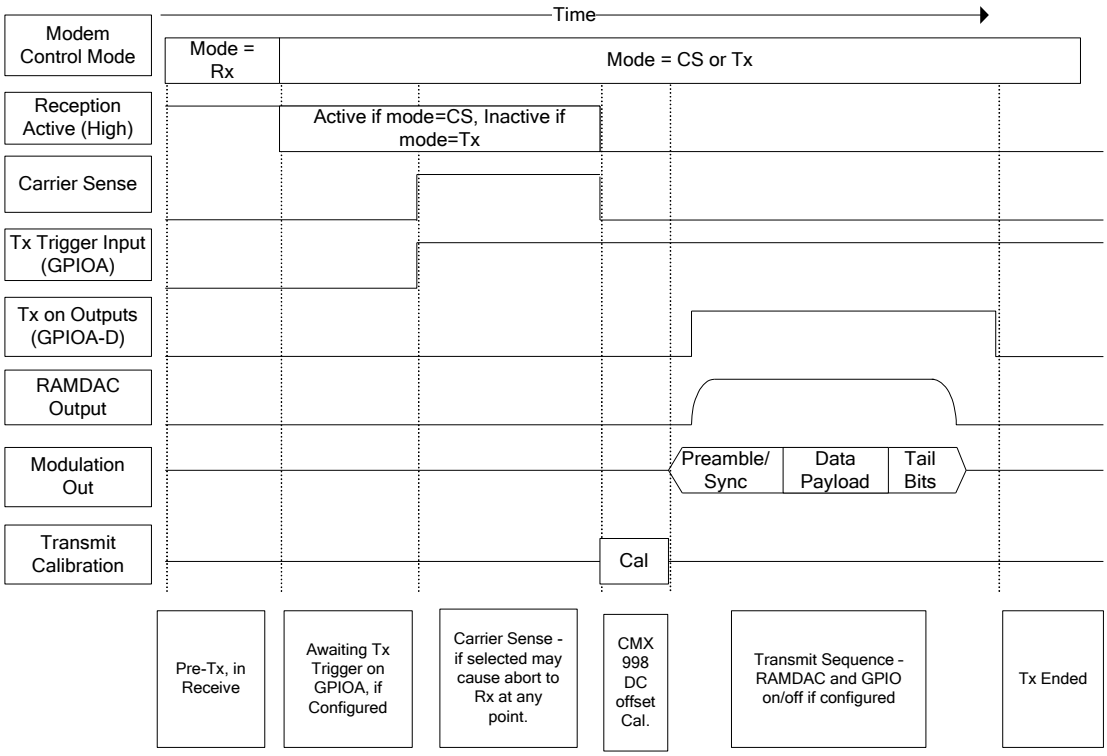


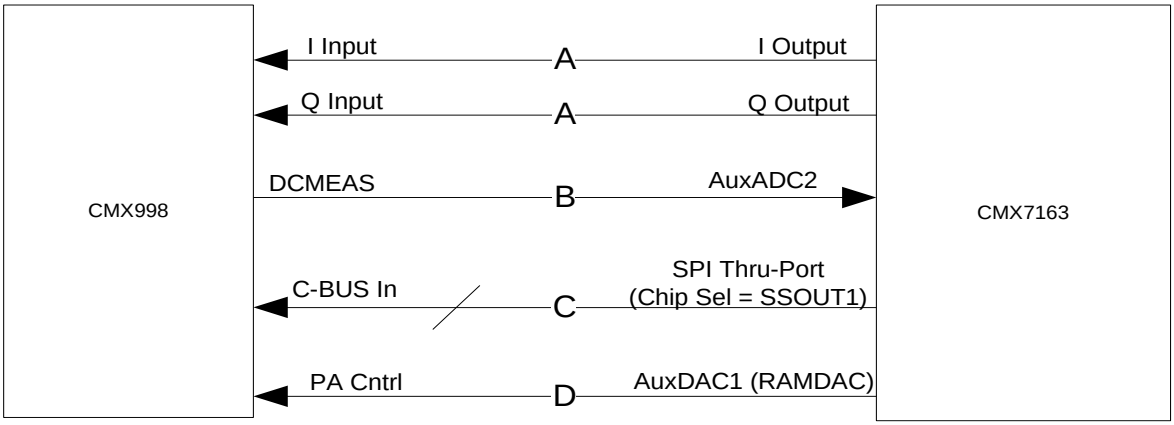
Figure 15 Transmit Sequence

7.4.11 CMX998 DC Offset Calibration

The CMX7163 may be interfaced to a CMX998 Cartesian Loop IC. The CMX998 is used to provide linearisation of the power amplifier used to transmit the modulation produced by the CMX7163. If the signal produced by the CMX7163 when no modulation is present does not exactly match the dc reference of the CMX998, carrier leakage will result. This worsens the transmitted signal quality. DC offset calibration is intended to significantly reduce the carrier leakage.

The CMX998 Cartesian Feed-back Loop Transmitter datasheet and an application note "CMX998 Cartesian Feedback Loop dc Calibration" are both available from the CML website (www.cmlmicro.com) and should be referred to for a more in-depth understanding of the need for dc offset calibration.

The CMX7163 performs automatic dc offset calibration as either part of a transmit sequence or in a separate calibration stage. DC offset calibration determines the dc offset that should be applied to the I Output and Q Output signals by the CMX7163 to minimise carrier leakage. The results of calibration will be held by the CMX7163 for use in later transmissions and are made available to the host. The interface is required to be as shown in Figure 16 CMX998 DC Calibration Interfaces.



A. The CMX7163 I and Q Outputs are used to provide dc levels, which are adjusted to make the error I/Q measurements equal to the Reference I/Q measurements

B. AuxADC2 is used to sample DCMEAS – To measure Reference signals and error signals

C. The SPI Thru-Port is used to control the CMX998 – selecting Reference I/Q and Error I/Q as measurements, as well as high gain/low gain modes of the CMX998

D. The RAMDAC is typically used to ramp the PA Control voltage up after calibration is complete. This is not a part of the calibration sequence, but may be active as part of the transmit sequence.

Figure 16 CMX998 DC Calibration Interfaces

During calibration the CMX998 is controlled by the CMX7163 using the SPI Thru-Port (The CMX998 is assumed to be device 1) to select one of the following to be output to the CMX998 DCMEAS output:

I Reference	The CMX998 dc reference for the In-phase signal path
Q Reference	The CMX998 dc reference for the Quadrature signal path
I Error (Low/high gain[2])	The CMX998 measure of the dc produced by the input signal on the In-phase signal path
Q Error (Low/high gain)	The CMX998 measure of the dc produced by the input signal on the Quadrature signal path

During calibration the CMX7163 uses AuxADC2 to measure Reference I and Reference Q. It then outputs a dc level on the I Output, Q Output signals. AuxADC2 is used to measure the DCMEAS I and Q Error and I Output, Q Output are adjusted to make the DCMEAS I and Q errors equal to the DCMEAS I Reference and Q Reference measurements.

[2] The low and high gain states are created by adjusting the gain of the error amplifiers in the CMX998, see the CMX998 datasheet for more information.

There are three complications to this process:

1. The total gain of the feedback loop I Output to CMX998 DCMEAS Error signal to AuxADC is unknown – so the adjustment to the I Output signal may not be calculated completely accurately from a single measurement. Therefore the gain applied to the calculated adjustment may be programmed and a number of iterations selected, resulting in a damped feedback loop.
2. The dc error to be corrected is usually large enough that if measured with the CMX998 in high gain mode the DCMEAS output would saturate. This makes calculation of the magnitude of error impossible. Therefore low gain mode should be used initially.
3. When changing from low to high gain modes the circuit changes (see dc calibration Application Note referenced earlier), therefore the correction needed changes. However the low gain correction should at least be close to bringing the high gain measurement out of saturation. The relationship between correction computed using low gain and high gain is consistent – so may be noted and applied as an offset.

The calibration sequence implemented in the CMX7163 has the following stages:

Setup	Initialise the SSP port, AuxADC and select RefI as DCMEAS output from the CMX998
RefI	Read RefI, select DCMEAS = RefQ
RefQ	Read RefQ, select DCMEAS = ErrorI
ErrorILo	Read ErrorI assuming Low gain and adjust the I Output accordingly
ErrorQLo	Read ErrorQ assuming Low gain and adjust the Q Output accordingly
	Iterate – go to ErrorILo after a delay for corrected signals to settle
HighGain	Select High gain mode of the CMX998, apply Low to High gain mode correction
ErrorQHi	Read ErrorQ assuming High gain and adjust the Q Output accordingly
ErrorIHi	Read ErrorI assuming High gain and adjust the I Output accordingly
	Iterate – go to ErrorQHi after a delay for corrected signals to settle
Tidyup	Restore the CMX998, to its stage pre-calibration – ready to output modulation

Note: Despite no modulation being produced, the Tx Done flag of IRQ Status - $7E read register will be set at the completion of the CMX998 DC Offset Calibration task.

The timings of each calibration step can be configured using
P4.8: Set legacy timing mode

b0	ADC Sample Delay	0 - minimal delay mode (gives a delay of 1.2 symbol times) 1 - legacy delay mode (gives a delay of 8.2 symbol times)
b1	Tx Done and Tx Last Tail indication timing	0-Selects minimal jitter of +/-0.6 symbol times for Tx Done and Tx Last Tail indication timing. Enables the use of the P4.9 delay adjustment control for Tx Done and Tx Last Tail indication timing. Adjusting these delays enables indication timing to be changed to better match any changes in Tx pulse shaping filter delay or for other user purposes. 1-legacy timing delay mode (delay not specified; delay and jitter behaviours will be consistent so long as the number of data field symbols, number of tail symbols, and other factors are not changed)
b2-15	*Reserved*	Reserved – set to 1

P4.9: Set Tx Done delay

Only if P4.8 b1=0 then this controls the delay in indicating Tx Done and Tx Last Tail indications, in units of 1.2 symbol times. The default value makes Tx Done indication coincide with when the end of the last data field symbol analog signal is produced at the CMX7164 IOUTPUT and QOUTPUT pins when the default Tx pulse shaping filter is engaged. The user may adjust this parameter value to suit the different delay of any other different pulse shaping filter used.

P4.10: Offset tx end sequence start time
Adjusts the tx end sequence start time to be earlier than the default time. Adjustment is in symbols.

Program Block 5 – Burst Tx Sequence. To reduce calibration time a calibration sequence may be configured that omits some stages of the calibration process. However there must always be a Setup and TidyUp stage, and if ErrorQHi and ErrorIHi are included then the High gain stage must be included as well.

The registers used during Tx dc offset calibration are:

- 10.1.18 Modem Mode and Control - $6B write
- 0
- P4.8: Set legacy timing mode
-

b0	ADC Sample Delay	0 - minimal delay mode (gives a delay of 1.2 symbol times) 1 - legacy delay mode (gives a delay of 8.2 symbol times)
b1	Tx Done and Tx Last Tail indication timing	0-Selects minimal jitter of +/-0.6 symbol times for Tx Done and Tx Last Tail indication timing. Enables the use of the P4.9 delay adjustment control for Tx Done and Tx Last Tail indication timing. Adjusting these delays enables indication timing to be changed to better match any changes in Tx pulse shaping filter delay or for other user purposes. 1-legacy timing delay mode (delay not specified; delay and jitter behaviours will be consistent so long as the number of data field symbols, number of tail symbols, and other factors are not changed)
b2-15	*Reserved*	Reserved – set to 1

P4.9: Set Tx Done delay
Only if P4.8 b1=0 then this controls the delay in indicating Tx Done and Tx Last Tail indications, in units of 1.2 symbol times. The default value makes Tx Done indication coincide with when the end of the last data field symbol analog signal is produced at the CMX7164 IOUTPUT and QOUTPUT pins when the default Tx pulse shaping filter is engaged. The user may adjust this parameter value to suit the different delay of any other different pulse shaping filter used.

P4.10: Offset tx end sequence start time
Adjusts the tx end sequence start time to be earlier than the default time. Adjustment is in symbols.

- Program Block 5 – Burst Tx Sequence
- 10.1.30 I/Q Offset - $75, $76 read
- 10.1.8 I/Q Output Control - $5D, $5E write

7.4.12 Other Modem Modes

Tx Preamble
In Tx mode a transmit preamble feature is provided to aid setup – the preamble may be programmed to any useful repeating 8-bit pattern.

Tx PRBS

In Tx mode, a fixed PRBS (pseudo random bit sequence) or a repeated preamble transmission is provided and may be used for test and alignment. A 511 bit PRBS conforming to ITU-T O.153 (Paragraph 2.1) is used to generate the PRBS.

The output created by transmitting a PRBS using 16-QAM is shown in Figure 17. The 16 constellation points are just visible on the plot.

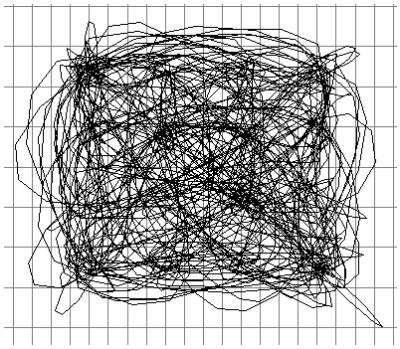


Figure 17 Transmit Constellation

Rx Constellation

A test mode to examine the Rx constellation diagram is also provided, this utilises the IOUTPUTP/N and QOUTPUTP/N pins to produce a diagnostic signal where the RRC filtered I/Q signals are output. This produces a two-dimensional constellation diagram which may be displayed on an oscilloscope in X-Y mode. Note that best results are often obtained with an analogue oscilloscope.

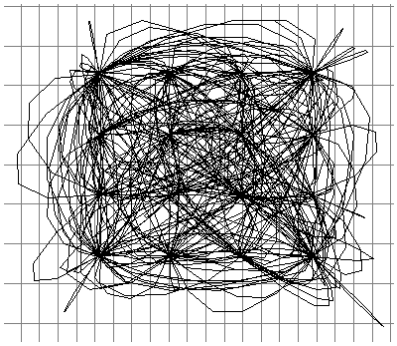


Figure 18 Constellation Diagram – no frequency or phase error

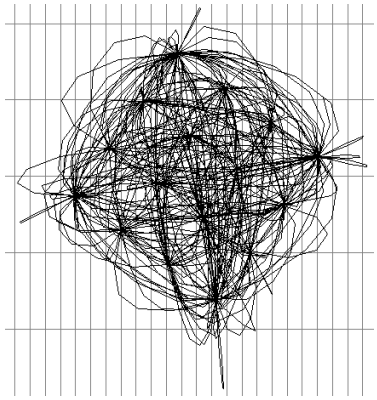


Figure 19 Constellation Diagram – phase error

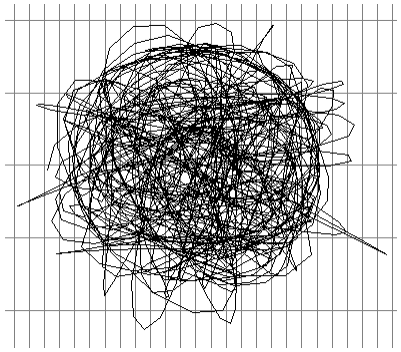


Figure 20 Constellation Diagram –frequency error

As shown in the third plot, if there is any frequency error between transmitting and receiving CMX7163 devices then the diagram will spin and be difficult to interpret. Therefore other diagnostic modes are provided as described below.

Any of the GPIO signals can be configured to produce a pulse train at the nominal symbol rate of the receiving CMX7163 to aid triggering whilst viewing the constellation diagram (I Output or Q Output alone

vs time) or other diagnostic modes in receive. In some cases it is advisable to obtain a trigger pulse that is synchronised to the transmitting modem symbol rate, for example if the transmitted signal comes from a signal generator.

Rx Diagnostics

A diagnostic mode is provided that produces channel filtered I/Q signals and an optional dc offset correction indication. This aids in diagnosing reception issues that may be related to I/Q dc offsets in the CMX7163 input signal. This diagnostic mode can still be of use when there is a frequency error present in the received signal. As shown in Figure 21 and Figure 22, the estimated I/Q dc offset correction is an extra dot in the centre of the constellation.

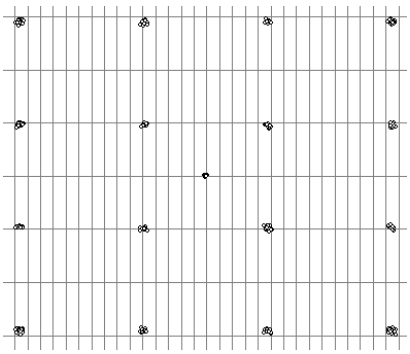


Figure 21 Sample at symbol timing with I/Q dc offset diagnostic mode (no frequency error)

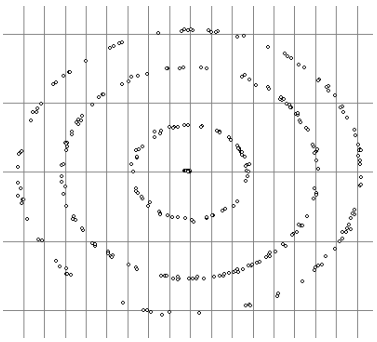
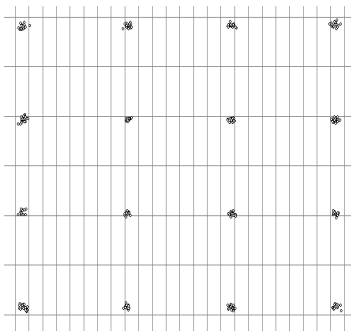


Figure 22 Sample at symbol timing with I/Q dc offset diagnostic mode (with frequency error)

A normalised received constellation diagnostic output is provided. It relies on having detected a frame sync and therefore being able to output the signal level measured at the symbol timing instant, with the frequency error removed and amplitude corrected. So long as the CMX7163 remains locked to a suitable signal the normalised constellation output will remain static regardless of frequency error and amplitude of the input signal (within limits – see section 9.1.4 CMX7163 FI-4.x Parametric Performance). If the signal becomes noisy or its amplitude small then the constellation points will spread as shown in Figure 23 and Figure 24.



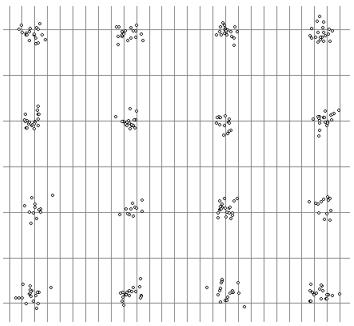


Figure 23 Normalised Constellation (even with a frequency or phase error)

Figure 24 Normalised Constellation (noisy received signal)

Note: The images of receive diagnostic modes shown above are idealised. In practice when using the I Output and Q Output signals to view diagnostics the transitions between constellation point are not instantaneous. Using an analogue oscilloscope is the best way to observe these diagnostic signals.

See:

- 10.1.18 Modem Mode and Control - $6B write
- 10.1.10Signal Control - $61 write.

7.4.13 Data Transfer

The payload data is transferred to and from the host via the C-BUS Command and Rx Data FIFOs, each of which provide efficient streaming C-BUS access. FIFO fill level can be determined by reading the Receive FIFO Level and Modem Command FIFO Level and controlled using FIFO Control - $50 write register. Interrupts may be provided on FIFO fill thresholds being reached, or successful transfer of a block of host requested FIFO data between CMX7163 modem and FIFOs.

Each FIFO word is 16 bits, with the least significant byte (LSByte) containing data, and the most significant (MSByte) containing control information. The control information indicates to the CMX7163 what type, or how much data is in the LSByte, for example if the byte belongs to a header block or contains only 4 valid bits. The control and data bytes may be written or read together using the Receive FIFO Word and Modem Command FIFO Word registers, or individually using their byte-wide registers.

Word wide FIFO writes involve writing 16-bit words to the Modem Command FIFO Word register using either a single write or streaming C-BUS. The whole word written is put into the Command FIFO, with the upper byte interpreted as control and the lower byte as data. This causes the control byte to be held in the Command FIFO Control Byte register.

Byte wide FIFO writes involve writing to the Modem Command FIFO Data Byte register using either single access or streaming C-BUS. This causes the Modem Command FIFO Control Byte (MSByte) and data written to the Modem Command FIFO Data Byte (LSByte) registers to be put into the command FIFO as one word. The control byte can be written separately as a single byte (this does not result in anything being added to the FIFO) or is preserved from a previous 16-bit Modem Command FIFO Data Byte write.

Likewise a word read from the Rx Data FIFO will return the Receive FIFO Control Byte in the MSByte and the Receive FIFO Data Byte at the top of the FIFO in the LSByte. Both registers will be updated so that when read next time they will provide details of the next item in the FIFO. Reading the Receive FIFO Control Byte only will not change the FIFO content. Reading the Receive FIFO Data Byte only will provide the data and remove the item from the FIFO – updating both control and data registers. In summary:

Operation	Effect
write Modem Command FIFO Control Byte register	Cmd FIFO control word updated, nothing added to Cmd FIFO
write Modem Command FIFO Data Byte register	Cmd FIFO control word + data byte written are added to Cmd FIFO
write Modem Command FIFO Word register	data word (control and data bytes) is added to Cmd FIFO. Cmd FIFO control word updated for future writes.
read Receive FIFO Control Byte register	Rx FIFO control word is returned, no effect on Rx FIFO contents

read Receive FIFO Data Byte register	Oldest Rx FIFO data byte is removed from FIFO and returned, Rx FIFO Word updated
read Receive FIFO Data Word register	Oldest Rx FIFO data word (control and data bytes) is removed from FIFO and returned, Rx FIFO control word updated

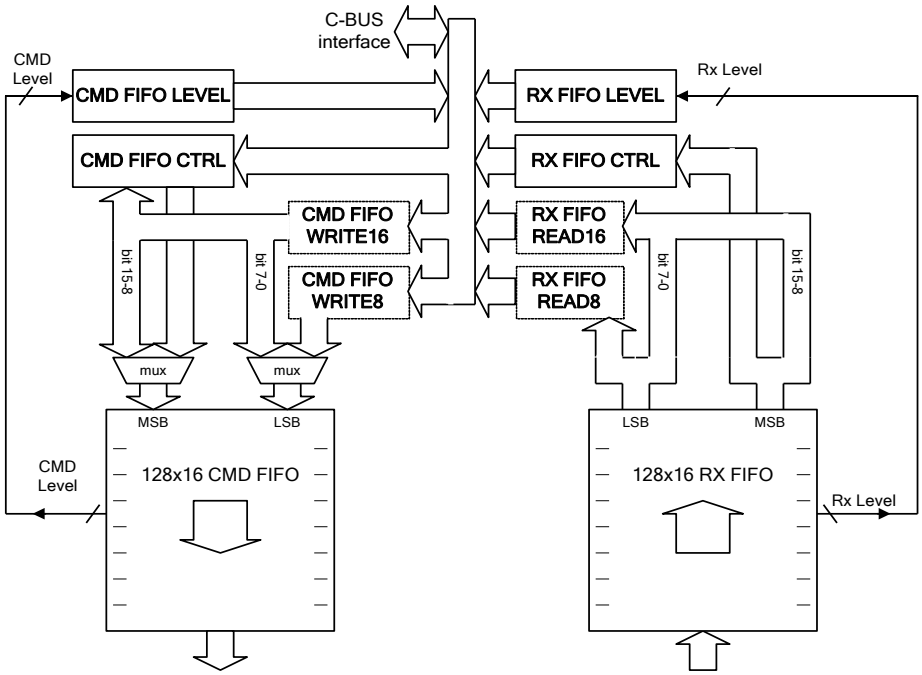


Figure 25 Command and Rx Data FIFOs

Raw or formatted data may be transmitted with the CMX7163 adding preamble, frame sync and tail bits. Raw or formatted transmission/reception is selected using the Modem Mode and Control - $6B write register, each whole transmission/reception must continue in the selected mode. Relevant registers are:

- 10.1.18 Modem Mode and Control - $6B write
- 10.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 10.1.26 Receive FIFO Data/Control - $4C, $4D, $4E read
- 10.1.25 Modem Command FIFO Level - $4B read
- 10.1.27 Receive FIFO Level - $4F read
- 10.1.4 FIFO Control - $50 write.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7163 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

7.4.14 Data Buffering

To expand the buffering capabilities of the CMX7163 two internal buffers are provided:

A Command buffer which buffers commands from the control FIFO which are yet to be processed.
An Rx data buffer which buffers received data yet to be loaded into the Rx data FIFO.

Transfer between the FIFOs and their respective buffers will occur during transmission, reception and Idle mode. Such transfer is not instantaneous so the FIFO fill levels should be used to indicate how much data the host may read or write at any time.

The Internal Buffer Fill Level - $70 read register allows the buffer fill levels to be read; their contents will be flushed when the respective FIFO is flushed.

See:

- 10.1.4 FIFO Control - $50 write
- 10.1.28 Internal Buffer Fill Level - $70 read.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7163 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

7.4.15 Raw Data Transfer

When transferring raw data the FIFO Control byte indicates the amount of data that will be transferred in a block before the CMX7163 interrupts the host. Byte and bit-wise transfers are possible, providing the facility to transmit or receive a burst of arbitrary length, not just a whole number of bytes. It is suggested that data is transferred in the maximum size blocks possible until the end of a burst - where the remaining bits, or bytes can be transferred in a single transaction of the required size.

When using byte wise or bit wise transfers the most significant bit of the data byte is transmitted (or received) first. When using bit wise transfers with a bit count of less than 8 the most significant bits are used. In all cases the bits are combined into symbols according to the selected modulation type.

It is also possible to ignore the concept of blocks of data whilst in raw mode. Instead, a transmission can just be treated as a series of bytes to transmit and FIFO levels/level IRQs used to manage the data flow. Likewise in receive the host can request continual data reception and the resulting bytes will be placed in the Rx Data FIFO. FIFO levels and level IRQs may be used to manage the data flow. This mode provides the ability to simply stream (using streaming C-BUS if desired) multiple bytes into or out of the CMX7163 as FIFO content allows.

7.4.16 Formatted Data Transfer

When the transfer of formatted data is selected by the Modem Mode and Control - $6B write register the FIFO Control byte indicates the block type to use in either sending or decoding the data. The block type dictates the format or quantity of data transferred, including how error detection and correction bits are added to the over air data stream.

7.4.17 Pre-loading Commands

It is advisable to pre-load data into the Command FIFO before transmission begins, or to pre-load receive data commands into the Command FIFO prior to frame sync reception.

7.4.18 GPIO Pin Operation

The CMX7163 provides 4 x GPIO pins, each pin can be configured independently as automatic/manual, input/output and rising/falling (with the exception of the combination automatic + input function which is only allowed for GPIOA).

Pins that are automatic outputs become part of a transmit sequence and will automatically switch, along with the RAMDAC – AuxDAC1 (if it is configured as automatic) during the course of a burst. Pins that are manual are under direct user control. When automatic, a rising, or a falling event at the start or end of transmission will cause the specified GPIO to be switched high or low accordingly.

GPIOA may be configured as an automatic input. This means that any attempted transmission will wait until GPIOA input is high (if rising is selected) or low (if falling is selected).

See:

- 0
- P4.8: Set legacy timing mode
-

b0	ADC Sample Delay	0 - minimal delay mode (gives a delay of 1.2 symbol times) 1 - legacy delay mode (gives a delay of 8.2 symbol times)
b1	Tx Done and Tx Last Tail indication timing	0-Selects minimal jitter of +/-0.6 symbol times for Tx Done and Tx Last Tail indication timing. Enables the use of the P4.9 delay adjustment control for Tx Done and Tx Last Tail indication timing. Adjusting these delays enables indication timing to be changed to better match any changes in Tx pulse shaping filter delay or for other user purposes. 1-legacy timing delay mode (delay not specified; delay and jitter behaviours will be consistent so long as the number of data field symbols, number of tail symbols, and other factors are not changed)
b2-15	*Reserved*	Reserved – set to 1

P4.9: Set Tx Done delay
Only if P4.8 b1=0 then this controls the delay in indicating Tx Done and Tx Last Tail indications, in units of 1.2 symbol times. The default value makes Tx Done indication coincide with when the end of the last data field symbol analog signal is produced at the CMX7164 IOUTPUT and QOUTPUT pins when the default Tx pulse shaping filter is engaged. The user may adjust this parameter value to suit the different delay of any other different pulse shaping filter used.

P4.10: Offset tx end sequence start time
Adjusts the tx end sequence start time to be earlier than the default time. Adjustment is in symbols.

- Program Block 5 – Burst Tx Sequence
- 10.1.13 GPIO Control - $64 write
- 10.1.33 GPIO Input - $79 read.

7.4.19 Auxiliary ADC Operation

The inputs to the four Auxiliary ADCs can be independently routed from any of four dedicated AuxADC input pins or the two main inputs. AuxADCs can be disabled to save power. BIAS in the VBIAS Control - $B7 write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC1-4 Control - $51 to $54 write registers. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in the AuxADC1-4 Control - $51 to $54 write registers. Setting the average counter to zero will disable the averager, for an average value of 1; 50% of the current value will be applied, for a value of 2 = 25%, 3 = 12.5%, continuing up to the maximum useful value of 11 = 0.0488%.

High and low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when an input exceeds the high or low threshold, or on every sample as required. The thresholds are programmed via the AuxADC1-4 Threshold- $55 to $58 write register.

Auxiliary ADC data is read back in the AuxADC1-4 Read - $71 to $74 read registers and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The AuxADC sample rate is selected using Program Block 1 – Clock Control.

See:

- 10.1.5 AuxADC1-4 Control - $51 to $54 write
- 10.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 10.1.29 AuxADC1-4 Read - $71 to $74 read
- 10.2.3 Program Block 1 – Clock Control

- 10.1.24 VBIAS Control - $B7 write.

7.4.20 Auxiliary DAC/RAMDAC Operation

The four auxiliary DACs are programmed via the AuxDAC1-4 Control - $59 to $5C write registers. AuxDAC1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The RAMDAC may be configured as automatic or manual using

P4.8: Set legacy timing mode

b0	ADC Sample Delay	0 - minimal delay mode (gives a delay of 1.2 symbol times) 1 - legacy delay mode (gives a delay of 8.2 symbol times)
b1	Tx Done and Tx Last Tail indication timing	0-Selects minimal jitter of +/-0.6 symbol times for Tx Done and Tx Last Tail indication timing. Enables the use of the P4.9 delay adjustment control for Tx Done and Tx Last Tail indication timing. Adjusting these delays enables indication timing to be changed to better match any changes in Tx pulse shaping filter delay or for other user purposes. 1-legacy timing delay mode (delay not specified; delay and jitter behaviours will be consistent so long as the number of data field symbols, number of tail symbols, and other factors are not changed)
b2-15	*Reserved*	Reserved – set to 1

P4.9: Set Tx Done delay

Only if P4.8 b1=0 then this controls the delay in indicating Tx Done and Tx Last Tail indications, in units of 1.2 symbol times. The default value makes Tx Done indication coincide with when the end of the last data field symbol analog signal is produced at the CMX7164 IOUTPUT and QOUTPUT pins when the default Tx pulse shaping filter is engaged. The user may adjust this parameter value to suit the different delay of any other different pulse shaping filter used.

P4.10: Offset tx end sequence start time

Adjusts the tx end sequence start time to be earlier than the default time. Adjustment is in symbols.

Program Block 5 – Burst Tx Sequence. The AuxDAC1-4 Control - $59 to $5C write register, with b12 set, controls the RAMDAC mode of operation when configured as a manually triggered RAMDAC. The RAMDAC ramp rate is controlled by the Internal system clock rate, which changes between active CS/Tx/Rx modes and Idle mode. Therefore it is inadvisable to return to Idle mode prior to RAMDAC ramp completion.

The default profile is a Raised Cosine (see Table 7 in the user manual), but this may be over-written with a user defined profile by writing to Program Block 0. The current profile may be scaled using the Signal Control - $61 write register. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero.

See:

- 10.1.7 AuxDAC1-4 Control - $59 to $5C write
- 10.2.2 Program Block 0 – RAMDAC
- 10.2.3 Program Block 1 – Clock Control
- 0
- P4.8: Set legacy timing mode
-

b0	ADC Sample Delay	0 - minimal delay mode (gives a delay of 1.2 symbol times) 1 - legacy delay mode (gives a delay of 8.2 symbol times)
b1	Tx Done and Tx Last Tail indication timing	0-Selects minimal jitter of +/-0.6 symbol times for Tx Done and Tx Last Tail indication timing. Enables the use of the P4.9 delay adjustment control for Tx Done and Tx Last Tail indication timing. Adjusting these delays enables indication timing to be changed to better match any changes in Tx pulse shaping filter delay or for other user purposes. 1-legacy timing delay mode (delay not specified; delay and jitter behaviours will be consistent so long as the number of data field symbols, number of tail symbols, and other factors are not changed)
b2-15	*Reserved*	Reserved – set to 1

P4.9: Set Tx Done delay
Only if P4.8 b1=0 then this controls the delay in indicating Tx Done and Tx Last Tail indications, in units of 1.2 symbol times. The default value makes Tx Done indication coincide with when the end of the last data field symbol analog signal is produced at the CMX7164 IOUTPUT and QOUTPUT pins when the default Tx pulse shaping filter is engaged. The user may adjust this parameter value to suit the different delay of any other different pulse shaping filter used.

P4.10: Offset tx end sequence start time
Adjusts the tx end sequence start time to be earlier than the default time. Adjustment is in symbols.

- Program Block 5 – Burst Tx Sequence
- 10.1.10 Signal Control - $61 write.

7.4.21 SPI Thru-Port

The CMX7163 offers an SPI Thru-Port which allows the host, using the main C-BUS interface, to command the CMX7163 to read or write up to three external SPI/C-BUS devices attached to the CMX7163. The CMX7163 acts as a SPI/C-BUS master in this mode, controlling three chip selects, clock and data out (MOSI), and receiving data in (MISO).

Each individual SPI/C-BUS device can be independently configured using Program Block 6 – SPI Thru-Port Configuration to have clock speed, inter-frame guard period and clock phase/polarity to match the specification of the slave SPI/C-BUS device attached. In order to offer a simpler, more convenient interface, a device can be designated C-BUS, rather than SPI. This means that data read/written is assumed to be in the format:

Address byte, data byte1 (optional), data byte 2 (optional)

In each case the CMX7163, as the master, drives the address and data for a write operation, or drives the address and receives the data for a read operation. Commands can be called 0, 1 or 2 byte reads or writes – with a 0 byte write typically being a reset command. As the word format is known, then for convenience only the desired read data is returned to the host.

SPI mode is a little more flexible. No assumption is made about the SPI word format, nor any assumption that the length is a whole number of bytes.

See:
- 10.1.11 SPI Thru-Port Control - $62 write
- 10.1.12 SPI Thru-Port Write - $63 write
- 10.1.32 SPI Thru-Port Read - $78 read
- 10.2.8 Program Block 6 – SPI Thru-Port Configuration.

7.4.22 SPI/C-BUS AGC

Using the SPI Thru-Port, the CMX7163 provides a method of controlling an external C-BUS device capable of implementing variable gain steps. When using I/Q receive modes this allows for a fast response to large signals causing clipping and an increase in gain when the signal becomes too small. Controlling the external device requires the host to program a table of eight C-BUS commands that the CMX7163 stores and outputs when a specific gain step is required. The commands may be produced by the AGC function, or the CMX7163 can be commanded to output them manually if required. Commands are programmed using Program Block 7 – AGC Configuration.

AGC is controlled by sensing clipping in the received signal – in which case the gain is backed off. While searching for a frame sync the gain will also be backed off when the signal is considered "large" – this ensures that after frame sync is detected there is headroom for the amplitude to increase a little. If the signal is sensed to be small for a period of time the gain can also be increased. The threshold for what is considered a small (or large) signal - requiring a gain change, the time for which it should remain small and the time to allow a gain adjustment to take effect is programmable. The overall system is shown below:

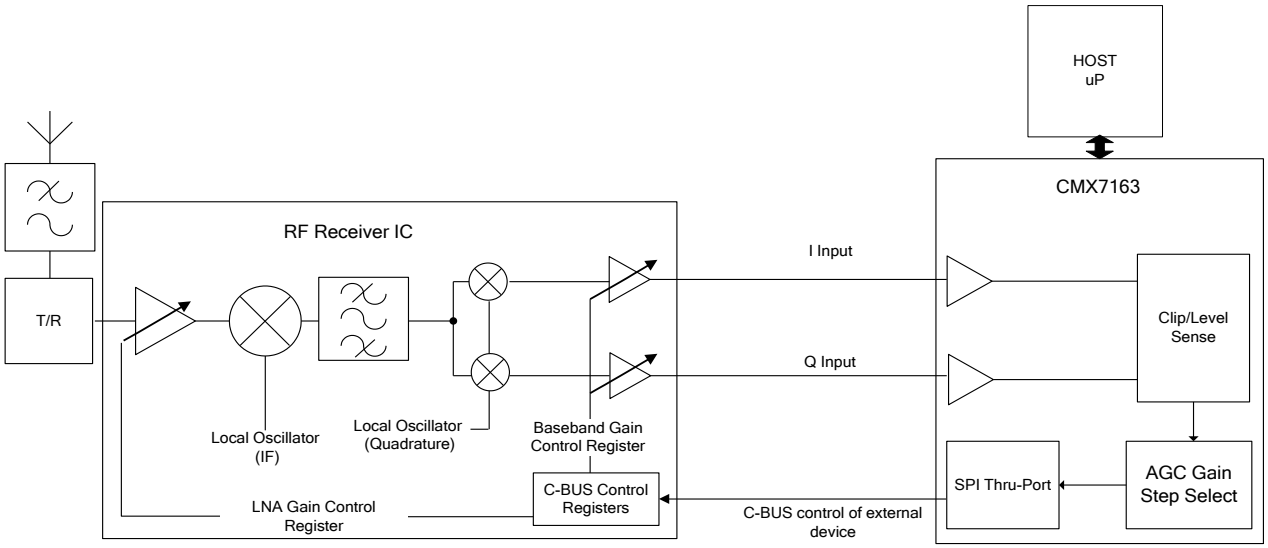


Figure 26 AGC using SPI Thru-Port

Controlling the external device as shown in Figure 26 causes the gain to step suddenly. This in itself may cause a short burst of errors, so once signal is being received it may be desirable to ensure that the gain is not changed unnecessarily. This is typically the case with short bursts of data, where it is likely that the signal amplitude will remain constant throughout the burst. To help achieve this, various AGC automatic modes are provided:

- Manual Gain – Controlled manually always, allowing user control and for control during latching in of I/Q dc corrections
- Full Auto – Gain can increase and decrease during the search for frame sync and during burst reception
- AGC lock on FS – Gain can increase and decrease during the search for frame sync but once a frame sync is detected its level will be fixed
- AGC down after FS – Gain can increase and decrease during the search for frame sync but once a frame sync is detected its level will only decrease.

AGC changes during the frame sync can cause the frame sync to be corrupted and therefore not detected by the CMX7163. To avoid this problem the CMX7163 compares the incoming on-channel signal to a Signal Detect Threshold, the resulting AGC behaviour is as shown in Figure 27:

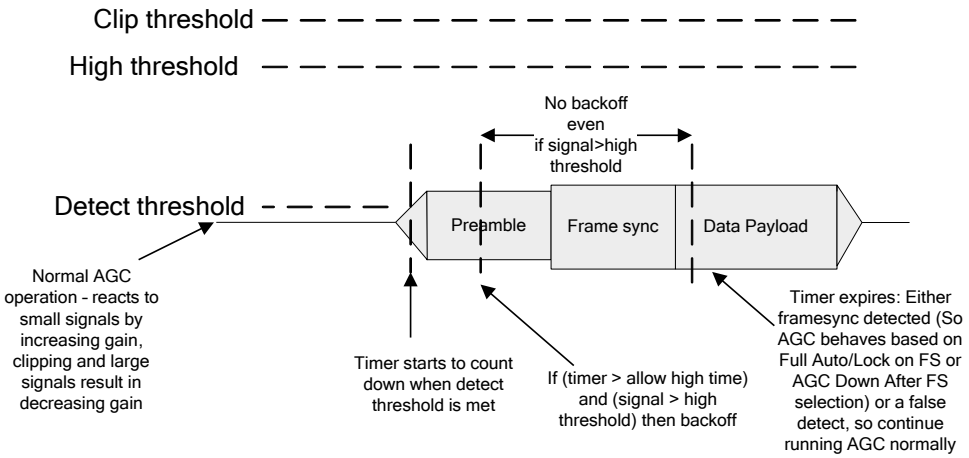


Figure 27 AGC Behaviour During Burst Reception

A general issue with I/Q receivers is that of dc offsets. Offsets are generated by the receiver hardware and typically vary with channel selection, but depending on receiver architecture can also change with gain. The CMX7163 is capable of calculating I/Q dc offset corrections but, if the gain steps suddenly and therefore the dc offset changes suddenly, errors may occur. Once again this may only be an issue for longer bursts when it is necessary to change gain during reception.

To overcome the dc offset issue the CMX7163 allows an I/Q dc offset correction to be latched in for each AGC gain step. When a gain step other than maximum gain is selected the tabulated dc offset correction will become active and tracking will be suspended. Additionally, in receivers with large dc offsets present, a gain change may result in a sufficiently large step in dc offset that the signal will look small/large to the AGC algorithm resulting in unwanted gain changes. The CMX7163 is able to use the I/Q dc offset information to correct for this effect.

AGC thresholds and parameters may be changed during reception for ease of setup and are controlled using the Signal Control - $61 write register. All times are measured in units of 6/5 of a symbol period. All levels or thresholds are compared to the magnitude of signed 16 bit samples, with max range therefore being 32767 to -32768.

See:

- 10.2.8 Program Block 6 – SPI Thru-Port Configuration
- 10.2.9 Program Block 7 – AGC Configuration
- 10.1.14 AGC Control - $65 write
- 10.1.10 Signal Control - $61 write
- 11.2.1 Effect of AGC on DC Offsets.

7.5 Digital System Clock Generators

The CMX7163 includes a two-pin Xtal Oscillator circuit. This can either be configured as an oscillator, as shown in section 4, or the XTAL/CLK input can be driven by an externally generated clock. The crystal (Xtal) source frequency is typically 9.6MHz and if an external oscillator is used the input frequency is typically 9.6 or 19.2 MHz. For both cases reference frequencies in the range specified in 9.1.2 Operating Limits may be used.

7.5.1 Main Clock Operation

A digital PLL is used to create the main clock for the internal sections of the CMX7163. The configuration of the main clock and the internal clocks derived from it is controlled using Program Block 1 – Clock Control.

The CMX7163 defaults to settings appropriate for a 19.2MHz externally generated clock with a baud rate of 9600s/s, however if a different reference frequency is to be used, or a different baud rate required, then Program Block entries P1.1 to P1.6 will need to be programmed appropriately at power-on. A table of preferred values is provided in Table 8 along with details of how to calculate settings for other baud rates and crystal frequencies.

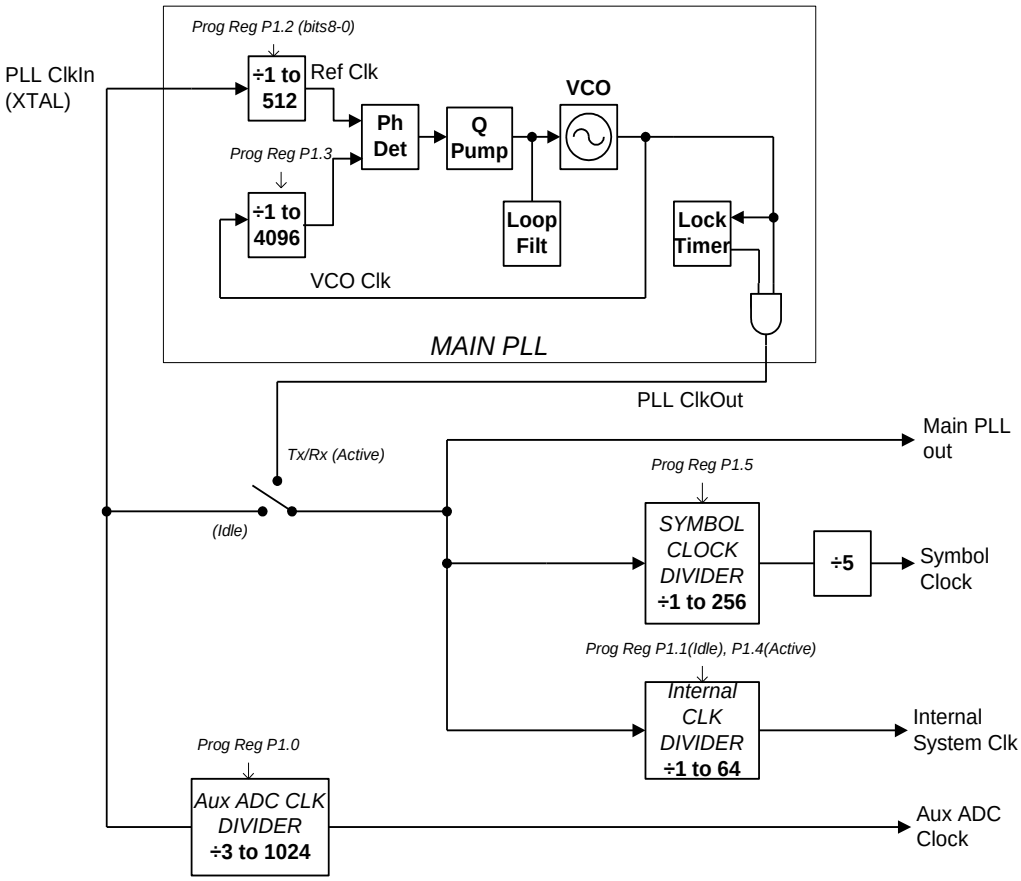


Figure 28 Main Clock Generation

See:

- 10.2.3 Program Block 1 – Clock Control

7.5.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. The System Clock circuitry is shown in Figure 29 Digital System Clock Generation Schemes.

Having chosen the input frequency source, system clock generation may be by simply dividing the input frequency source, or via its own phase locked loop. The system clock PLL does not affect any other internal operation of the CMX7163 - so if a frequency that is not a simple fraction of the Xtal is required, it can be used with no side effects. There is one phase locked loop, with independent output dividers to provide phase locked output signals.

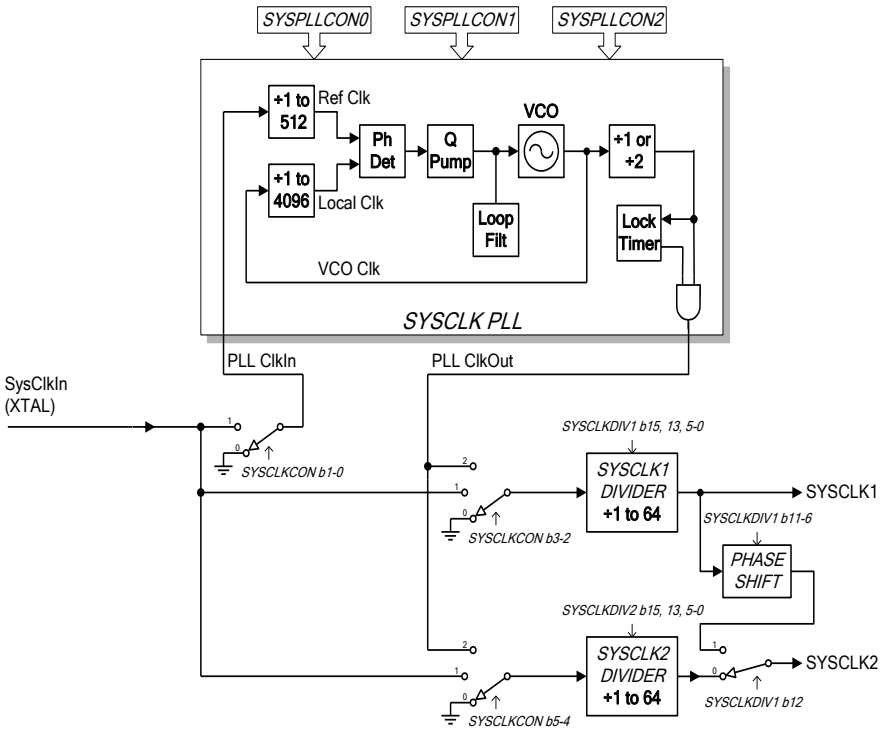


Figure 29 Digital System Clock Generation Schemes

See:

- 10.2.3 Program Block 1 – Clock Control.

7.6 Signal Level Optimisation

The internal signal processing of the CMX7163 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 9.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

7.6.1 Transmit Path Levels

For the maximum signal out of the I/Q Outputs, the signal level at the output of the modem block is set to be 0dB, the Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The signals output from I Output and Q Output may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment. When transmitting I/Q format signals inverting one of the I/Q pair has a similar effect to swapping I with Q.

Dc offsets may be added to the signal, however care must be taken that the combination of gain and dc offset does not cause the signal to clip at any point in the signal processing chain, which is: Fine gain followed by dc offset addition, followed by coarse gain.

See:

- 10.1.8 I/Q Output Control - $5D, $5E write
- 10.1.23 I/Q Output Coarse Gain - $B4, $B5 write.

7.6.2 Receive Path Levels

The Coarse Input has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the I Input or Q Input pins is specified in section 9.1.3 Operating Characteristics.

A Fine Input level adjustment is provided, although the CMX7163 should operate correctly with the default level selected. The primary purpose of the Fine Input level adjustment is to allow independent inversion of the I/Q Input signals. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment. When receiving I/Q format signals inverting one of the I/Q pair has a similar effect to swapping I with Q.

Dc offsets can be removed by the CMX7163, the offset to remove can be selected by the host or calculated automatically by the CMX7163.

It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal dc offset removal or attenuation.

See:

- 10.1.9 I/Q Input Control - $5F, $60 write
- 10.1.20 I/Q Input Configuration - $B0 write.

7.7 C-BUS Register Summary

Table 2 C-BUS Registers

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)
$01	W	C-BUS General Reset	0
$48	W	Modem Command FIFO Data Byte	8
$49	W	Modem Command FIFO Word	16
$4A	W	Modem Command FIFO Control Byte	8
$4B	R	Modem Command FIFO Level	8
$4C	R	Receive FIFO Data Byte	8
$4D	R	Receive FIFO Word	16
$4E	R	Receive FIFO Control Byte	8
$4F	R	Receive FIFO Level	8
$50	W	FIFO Control	16
$51 to $54	W	AuxADC1-4 Control	16
$55 to $58	W	AuxADC1-4 Threshold	16
$59 to $5C	W	AuxDAC1-4 Control	16
$71 to $74	R	AuxADC1-4 Read	16
$5D	W	I Output Control	16
$5E	W	*Q* Output Control	16
$5F	W	I Input Control	16
$60	W	Q Input Control	16
$61	W	Signal Control	16
$65	W	AGC Control	16
$66	W	Rx Tracking	16
$69	W	Reg Done Select	16
$70	R	Internal Buffer Fill Level	16
$75	R	I Offset	16
$76	R	Q Offset	16
$77	R	AGC Gain and RSSI	16
$7A	R	Rx Error Magnitude	16
$7B	R	Frequency Error	16
$62	W	SPI Thru-Port Control	16
$63	W	SPI Thru-Port Write	16
$64	W	GPIO Control	16
$78	R	SPI Thru-Port Read	16
$79	R	GPIO Input	16
$6A	W	Programming	16
$6B	W	Modem Mode and Control	16
$6C	W	IRQ Mask	16
$7D	R	Programming Register Read	16
$7E	R	IRQ Status	16
$7F	R	Modem Mode and Control Readback	16
$B0	W	I/Q Input Configuration	16
$B1	W	I Input Coarse Gain	16
$B2	W	Q Input Coarse Gain	16
$B3	W	I/Q Output Configuration	16
$B4	W	I Output Coarse Gain	16
$B5	W	Q Output Coarse Gain	16
$B7	W	VBIAS Control	16

All other C-BUS addresses are reserved and must not be accessed.

8 CMX7163 FI-4.x Features

The CMX7163 FI-4.x uses a QAM modulation scheme, switchable between 4-, 16- and 64-QAM on a burst by burst basis. The symbol rate is configurable up to 20,000 symbols/sec resulting in 106,000 user bits per second maximum. Raw data can be transferred, in addition to formatted data blocks. Formatted data blocks may be of variable length – from 15 to 416 bytes and support a combination of 16-bit or 32-bit CRC for error detection, plus error correction.

8.1 CMX7163 FI-4.x Modulation

CMX7163 FI-4.x produces QAM modulation, with three options: 4-, 16- or 64-QAM, see Figure 30. In each case, the signal is root raised cosine filtered. The same filter is applied in receive to remove inter-symbol interference. Due to the way the signal is produced, there is no deviation to select, instead only the baud rate may be altered. This has a direct effect on the signal bandwidth. A baud rate of 18ksymbols/second is typical of a 25kHz channel spacing and provides:

QAM Variant	Bits per Symbol	Base Over-air Bit Rate (18,000symbols/s)	Raw Mode Over-air Bit Rate (18,000symbols/s)
4-QAM	2	36,000bps	32,000bps
16-QAM	4	72,000bps	64,000bps
64-QAM	6	108,000bps	96,000bps

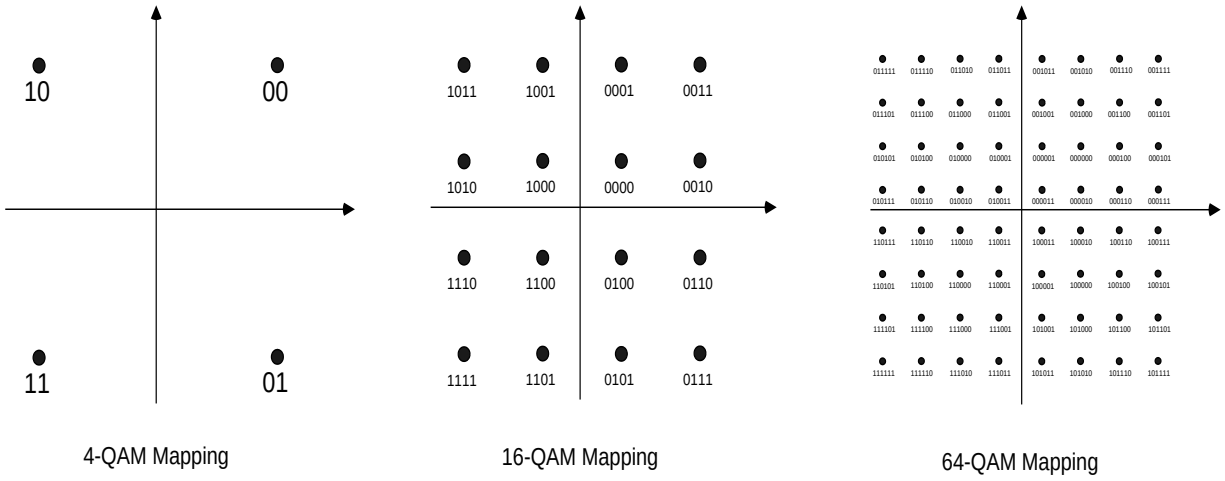


Figure 30 QAM Mappings

The signal spectrum is identical in bandwidth when using 4-, 16- or 64-QAM, however the peak-to-mean of each modulation type does vary.

4-QAM has a peak to mean of 5.3dB (α=0.2) or 3.8dB (α=0.35)
16-QAM has a peak to mean of 7.8dB (α=0.2) or 6.4dB (α=0.35)
64-QAM has a peak to mean of 9dB (α=0.2) or 7.5dB (α=0.35)

The difference between the base over air rate and the raw mode rate (which is the actual user data rate in raw mode at 18ksymbols/second) is due to some symbols being used internally by the modem to perform channel equalisation. A further implication of this is that any transmission must contain a multiple of 16 symbols, the CMX7163 will automatically pad as necessary.

8.2 CMX7163 FI-4.x Radio Interface

QAM modulation requires control of both phase and amplitude in the transmitter, and to measure both phase and amplitude in the receiver. Therefore the CMX7163 FI-4.x offers I/Q transmit and I/Q receive interfaces. This is shown in Figure 31, using the CMX992[3] for reception and the CMX998[4] for transmit – with RF power amplifier linearisation. The internal functions of the CMX7163 when operating in this mode are shown in Figure 2.

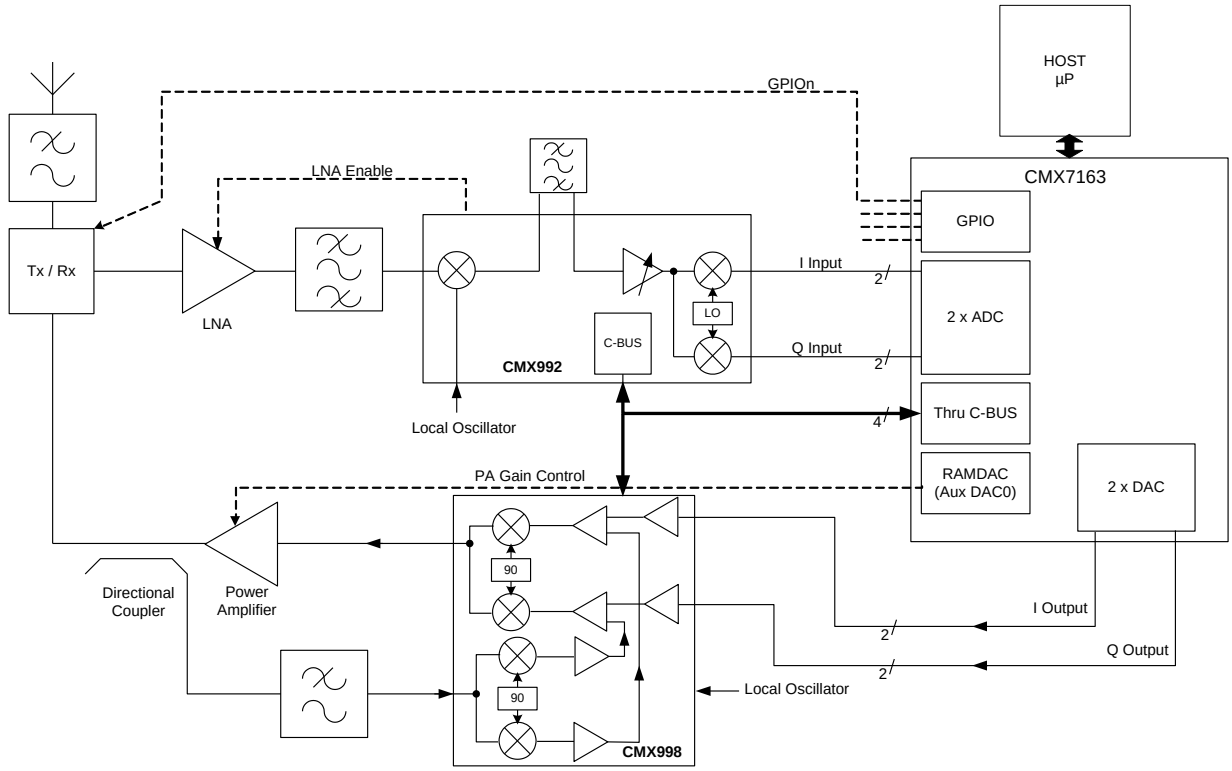


Figure 31 Outline Radio Design (I/Q in/out for QAM)

Use of I/Q receive mode brings with it the problem of I/Q dc offsets. There are dc offsets caused by the radio receiver – resulting in the signal into the CMX7163 having a dc offset other than BIAS. The offset needs to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but will vary if that frequency is changed. Gain within the radio receiver may also affect the dc offset seen by the CMX7163.

I/Q dc offset effects are a radio issue which is beyond the control of the CMX7163. However the CMX7163 does provide dc offset calculation and removal. These are described in detail in the application note section 11.2 DC Offsets in I/Q Receivers.

8.2.1 Control interfaces

As can be seen in Figure 31, the CMX7163 provides control interfaces to assist with controlling the radio transmitter and receiver. These include:

- A SPI Thru-Port– port which may be used to control radio ICs with C-BUS/SPI interfaces
- A RAMDAC which can be used to control PA ramp up and ramp down
- Four GPIO pins which may be used for Tx/Rx switching, LNA off and general device control

[3] CMX992 is an RF Quadrature/IF Receiver

[4] CMX998 is a Cartesian Feedback Loop Transmitter

8.3 CMX7163 FI-4.x Formatted Data

The CMX7163 FI-4.x supports formatted data, which provides the ability to channel code blocks of data using a variety of coding rates and CRCs. A frame structure would typically consist of a 24-symbol frame sync pattern followed by a 'Header Block', one or more 'Intermediate Blocks and a 'Last Block'.

The 'Header' block is self-contained in that it includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any) and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks. This checksum calculation should be reset as required using the “Reset CRC2” block type – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive it must be reset to match the expected input data block sequence.

A variety of different frame formats are possible, some examples are illustrated in Figure 32.

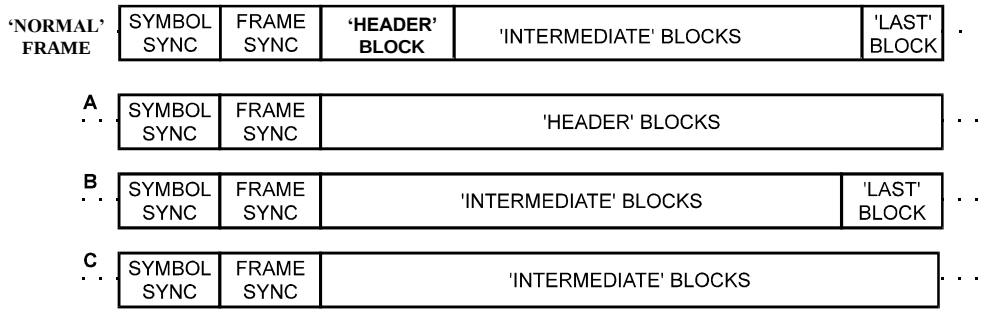


Figure 32 Suggested Frame Structures

The CMX7163 performs all of the block formatting and de-formatting. When receiving header blocks and last blocks the CMX7163 will indicate CRC success or failure and will provide the data regardless.

The size of the data block can be varied, as can the coding rate applied. A lower coding rate (more FEC bits) will improve performance in noisy or faded conditions but will reduce the user data rate available. Small data blocks provide the ability to produce a short burst or granularity in burst size. However to cope with fading conditions longer coded blocks are necessary. The CMX7163 FI-4.x provides blocks with the following formatted block sizes/rates:

Table 3 Formatted Block Types, Sizes and Rates

				User(CRC) bytes for a:		
Block Type	Block Size	Coding Rate (4-/16-QAM)	Coding Rate (64-QAM)	Header Block	Inter Block	Last Block
0	15 bytes	0.75	0.83	13(2)	15	11(4)
1	60 bytes	0.75	0.83	58(2)	60	56(4)
2	33 bytes	0.55	0.61	31(2)	33	29(4)
3	37 bytes	0.62	0.69	35(2)	37	33(4)
4	44 bytes	0.55	0.61	42(2)	44	40(4)
5	176 bytes	0.55	0.61	174(2)	176	172(4)
6	73 bytes	0.52	0.58	71(2)	73	69(4)
7	292 bytes	0.52	0.58	290(2)	292	288(4)
8	88 bytes	0.55	0.61	86(2)	88	84(4)
9	352 bytes	0.55	0.61	350(2)	352	348(4)
10	104 bytes	0.65	0.72	102(2)	104	100(4)
11	416 bytes	0.65	0.72	414(2)	416	412(4)

8.4 Receiver Response Equaliser

When receiving signals using a radio receiver the signal provided to the CMX7163 is likely to be distorted. Considering the architecture of Figure 31 as typical, the distortion will largely be caused by the crystal filter – shown as a bandpass filter in the diagram. The crystal filter operates on the received signal at an intermediate frequency. Its purpose is to attenuate unwanted signals, such as those on adjacent channels, before they get to the CMX7163.[5]

Typically the pass-band of the crystal filter is not flat or perfectly linear phase, resulting in the wanted QAM signal being distorted due to the amplitude/phase response of the filter. The result is usually a significantly degraded receive signal and therefore poor receive performance.

Other radio architectures may provide baseband filtering in order to help reject unwanted adjacent channel signals. Such filtering may also have a pass-band that is not flat, and therefore will degrade reception.

The CMX7163 provides a Receiver Response Equaliser that will compensate for the group delay and variation in gain of the crystal filter, or any other distortions present in the received signal. The equaliser must be trained with a clean, high level 4-QAM signal in order to establish the receiver response and produce a filter which compensates for it. Once this filter is calculated it may be read from the CMX7163 and stored for later use. The CMX7163 can be configured with up to two previously stored Receiver Response Equaliser filters which may, for example, be used to compensate for two different crystal filters in a radio designed to receive in two channel bandwidths.

Although trained using a 4-QAM signal, the resulting filter is suitable to compensate for the receiver response whilst receiving 4, 16 or 64-QAM signals. A suitable training signal may either be produced using another CMX7163 or by using the training sequence described in section 11.8 Receiver Response Equaliser Training Sequence.

The Receiver Response Equaliser has two modes, single mode produces better results when correcting for receivers with a simple baseband roll off (for example in a direct conversion architecture); dual mode produces better results when compensating for a radio receiver which includes a crystal filter. Program Block 11 – Receiver Response Equaliserprovides equaliser mode selection, allows adjustment of the gain used in the feedback path when training the equaliser and allows the training time to be altered. The same program block allows the filter resulting from training to be read for storage and to be programmed back into the CMX7163 later, for use when receiving.

An example of the effect of the receiver crystal filter on a 4 and 16-QAM signals is shown in Figure 33. Once the equaliser has been trained, the resulting received signal is as shown in Figure 34. Each plot is gathered by using the Rx diagnostics mode of the CMX7163, see section 7.4.12 Other Modem Modes for details.

[5] Note that the CMX7163 provides significant channel filtering itself, but further rejection of unwanted signals is desirable in most applications to improve receiver dynamic range and prevent blocking or products generating intermodulation products reaching the low power ‘back-end’ of the receiver.

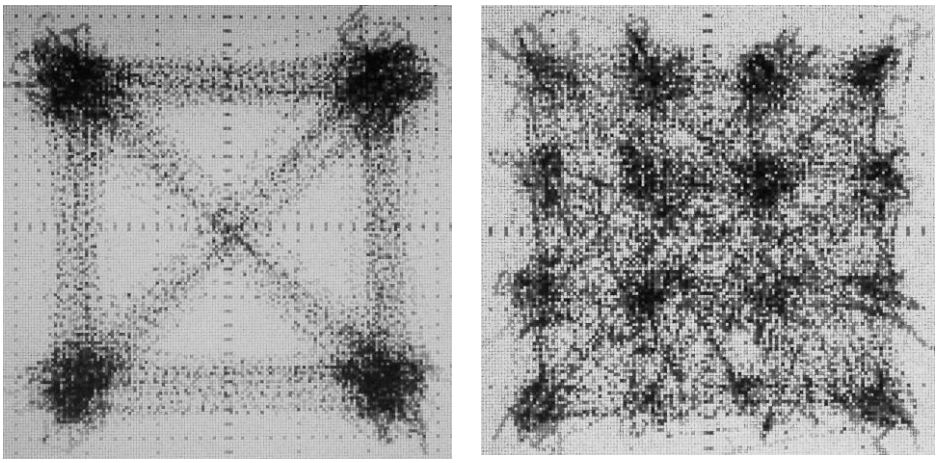


Figure 33 Received 4 and 16-QAM signals, no equalisation

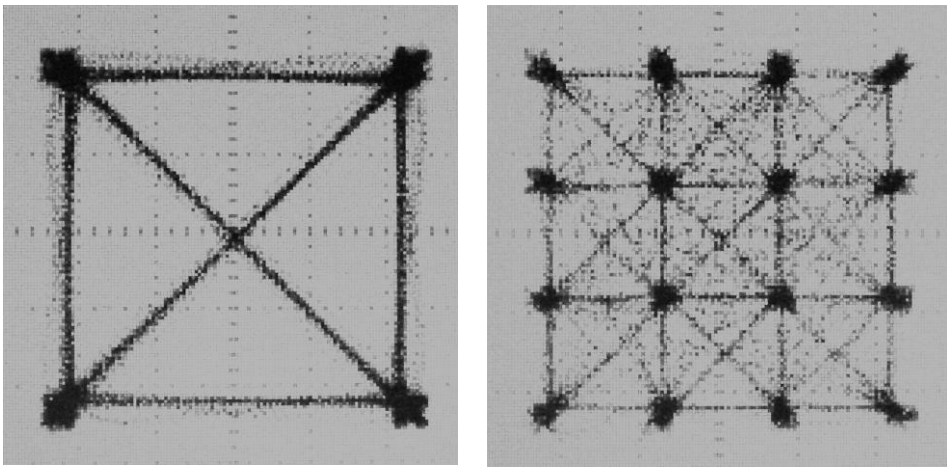


Figure 34 Received 4 and 16-QAM signals with equalisation

Results when using the Receiver Response Equaliser are shown in section 8.6.4 Receiver Response Equaliser Performance.

See:

- 10.1.18 Modem Mode and Control - $6B write
- 10.2.12 Program Block 11 – Receiver Response Equaliser
- 11.8 Receiver Response Equaliser Training Sequence

8.5 CMX7163 FI-4.x Typical Transmit Performance

The CMX7163 FI-4.x transmits QAM modulation using an I/Q interface. The modulation may be evaluated using a test system as illustrated in Figure 35 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation.

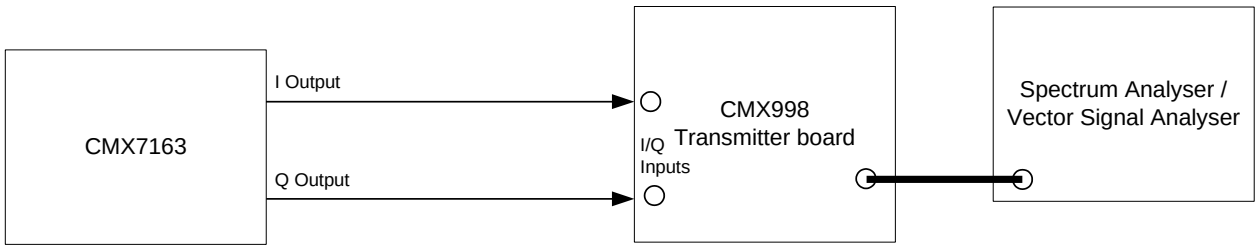
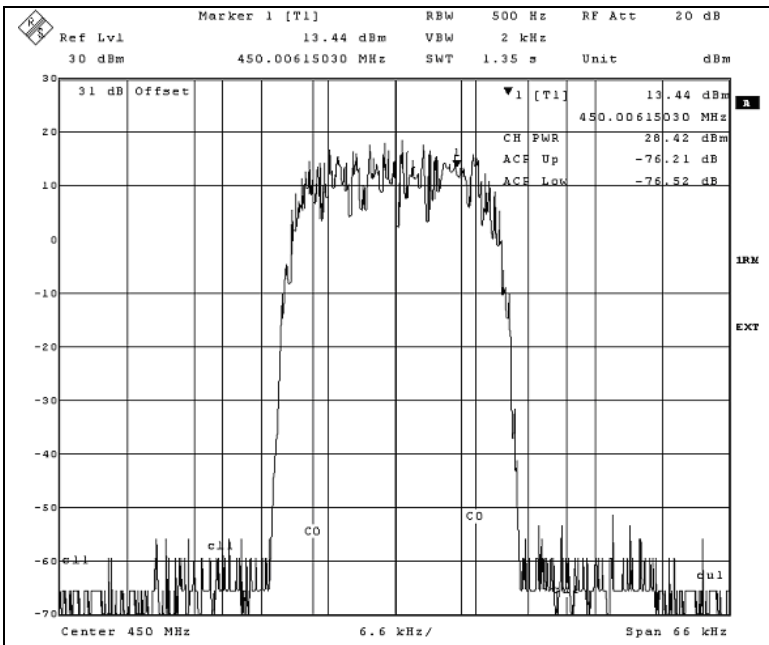


Figure 35 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation

Some typical results are shown in the following figures. The internal PRBS generator was used to generate the data in all the results shown. Two baud rates are demonstrated – 18k symbols/second which is typical of a 25kHz channel and 9k symbols/second which is typical of a 12.5kHz channel. In all cases the transmit filter selected had α=0.2. Depending on transmitter requirements (e.g. applicable standards) faster baud rates may be possible.

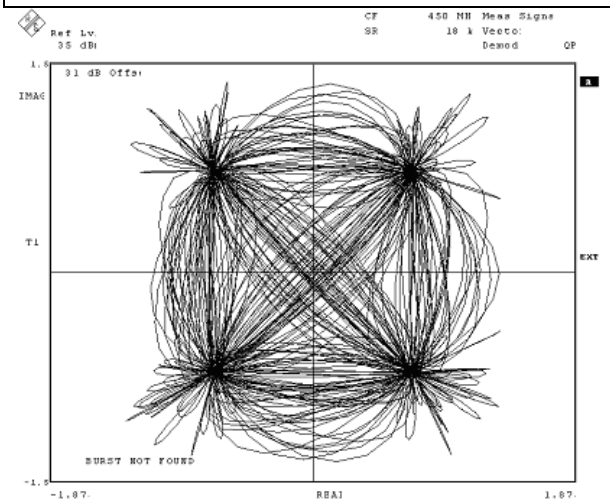


4-QAM Modulation spectrum with 18k symbols/second

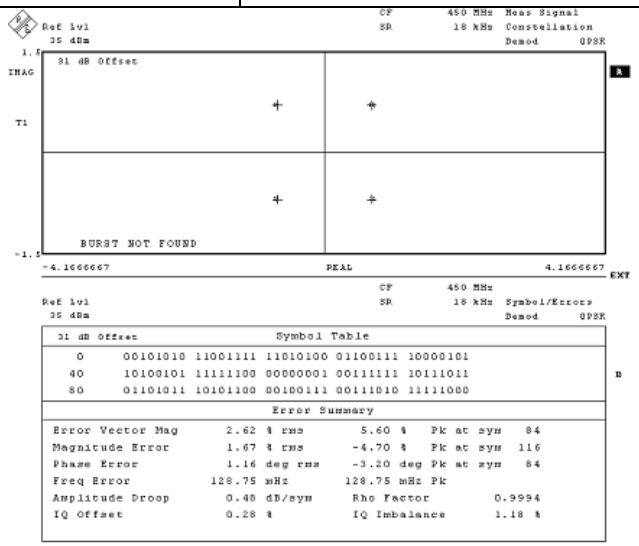
Adjacent Channel measurement for 25kHz channel:

ACP = -76dB

(Integration window = 16kHz)

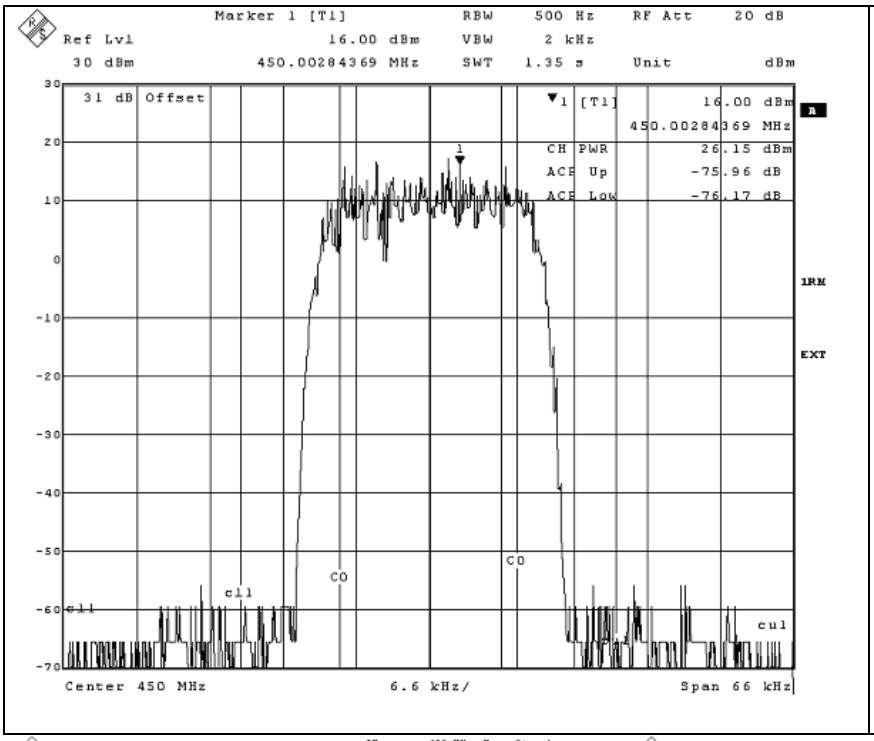


Constellation Diagram (Receiver filtered)



Error Vector

Figure 36 Tx Modulation Spectra (4-QAM), 18ksymbols/sec I/Q Modulation into CMX998

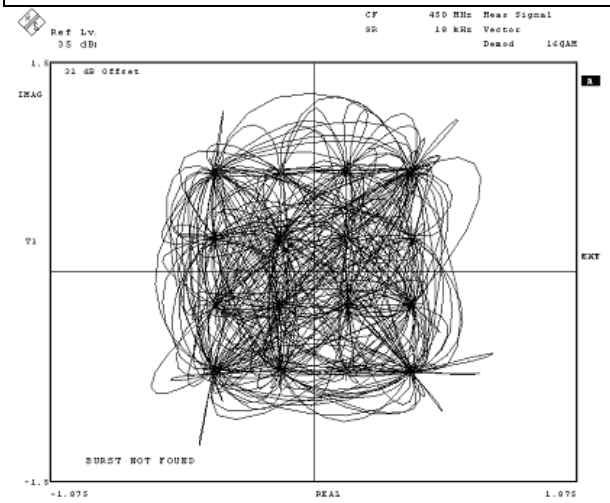


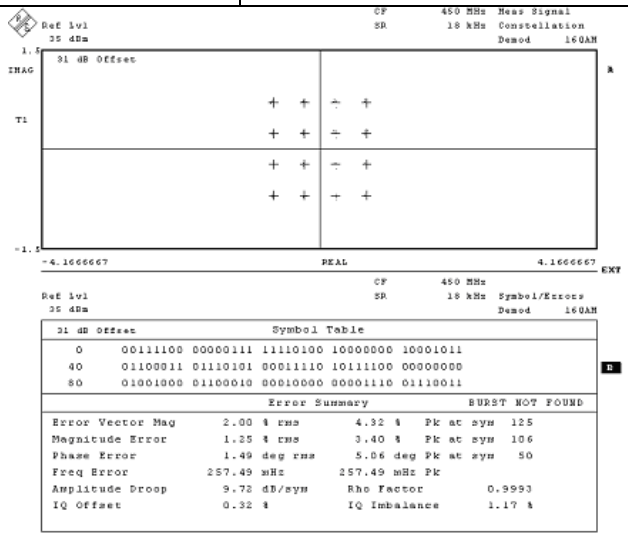
16-QAM Modulation spectrum with 18k symbols/second

Adjacent Channel measurement for 25kHz channel:

ACP = -75dB

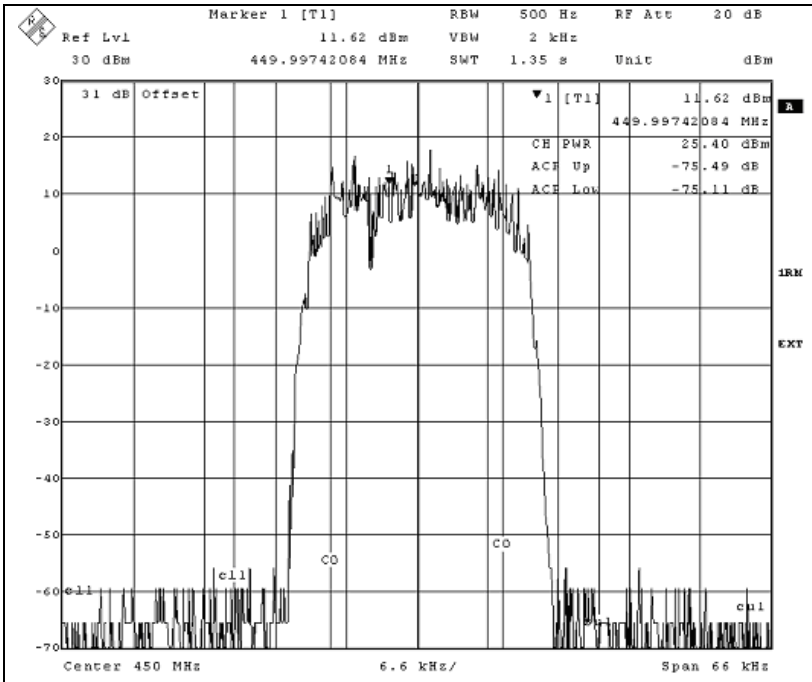
(Integration window = 16kHz)





Constellation Diagram (Receiver filtered) Error Vector

Figure 37 Tx Modulation Spectra (16-QAM), 18ksymbols/sec I/Q Modulation into CMX998



64-QAM Modulation spectrum with 18k symbols/second

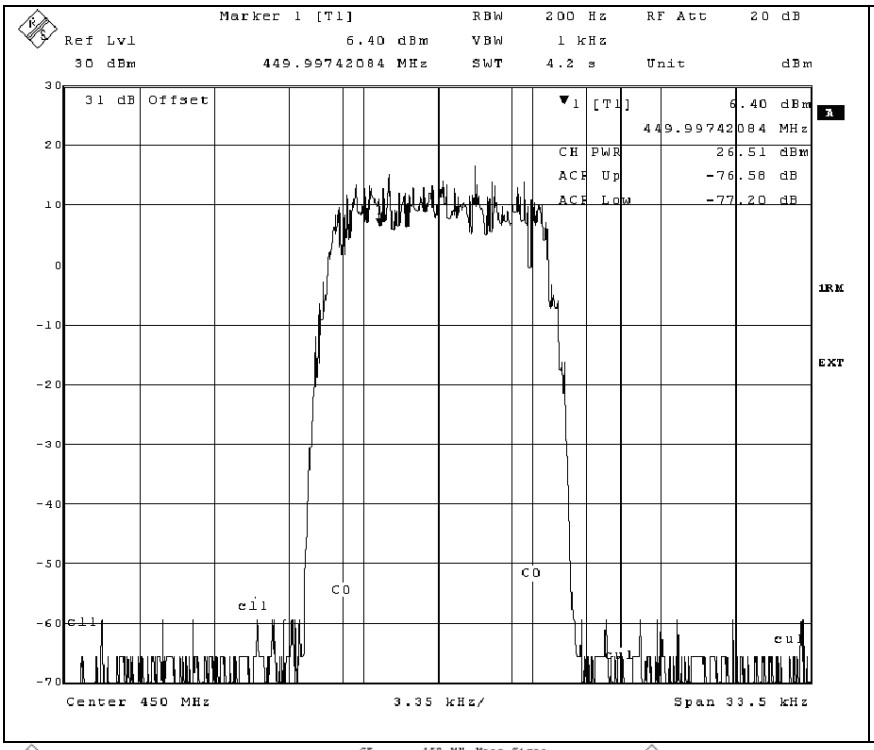
Adjacent Channel measurement for 25kHz channel:

ACP = -75dB

(Integration window = 16kHz)

Figure 38 Tx Modulation Spectra (64-QAM), 18ksymbols/sec I/Q Modulation into CMX998

For a particular baud rate we can see that the spectral shape, and adjacent channel power measurements for each QAM type are almost identical. This is to be expected, as each is generated using the same filters. The average power generated will vary though, as each type of QAM used has a different peak–to-mean ratio– and the CMX7163 transmits each with the same peak power.

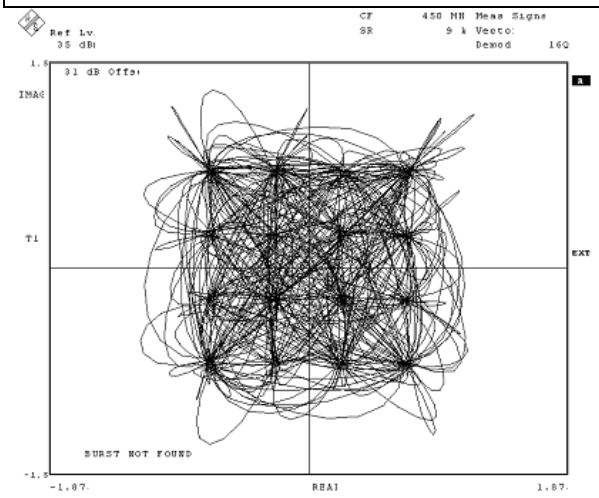


16-QAM Modulation spectrum with 9k symbols/second

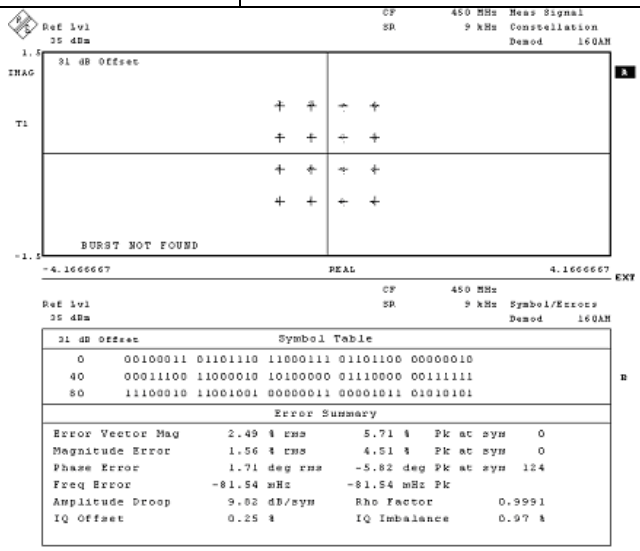
Adjacent Channel measurement for 12.5kHz channel:

ACP = -76dB

(Integration window = 8kHz)



Constellation Diagram (Receiver filtered)



Error Vector

Figure 39 Tx Modulation Spectra (16-QAM), 9k symbols/sec I/Q Modulation into CMX998

Comparing Figure 37 and Figure 39 demonstrates that changing baud rate simply scales the transmitted spectrum – halving baud rate will halve the bandwidth occupied. This relationship can be used to select the maximum baud rate for a given channel bandwidth.

8.6 CMX7163 FI-4.x Typical Receive Performance

8.6.1 Signal to Noise and Co-channel

The performance of the CMX7163 FI-4.x when receiving is shown in the following graphs. It should be noted that error rate performance depends on the modulation rate; whether 4-QAM, 16-QAM or 64-QAM is in use; the coding type selected and the block size. The CMX7163 FI-4.x supports multiple combinations of these factors and it is beyond the scope of this document to provide data for every combination, however graphs are provided showing a selection of representative cases ranging from best case performance (maximum coding and block size) to worst case where no coding is used (raw mode). Formatted block types 0, 6 and 7 (See Table 3 and section 8.3 CMX7163 FI-4.x Formatted Data, for details) show different levels of error correction performance, formatted block type 7 giving the best performance (see Table 3).

In all of the following graphs (Figure 40 - Figure 47) the data rate is 18 ksymbols/s, which is typical of the rate that may be achieved in a 25kHz RF channel. The selected transmit and receive filters had α=0.2. The signal to noise ratio is calculated as:

SNR = Mean signal power -174 + NF + 10 $\log_{10}$(RxBW)

Where:

NF = receiver noise figure in dB
RxBW = receiver noise bandwidth, which in Figure 40 - Figure 47 is 18kHz
Mean signal power is in dBm
SNR = Signal to Noise Ratio in dB

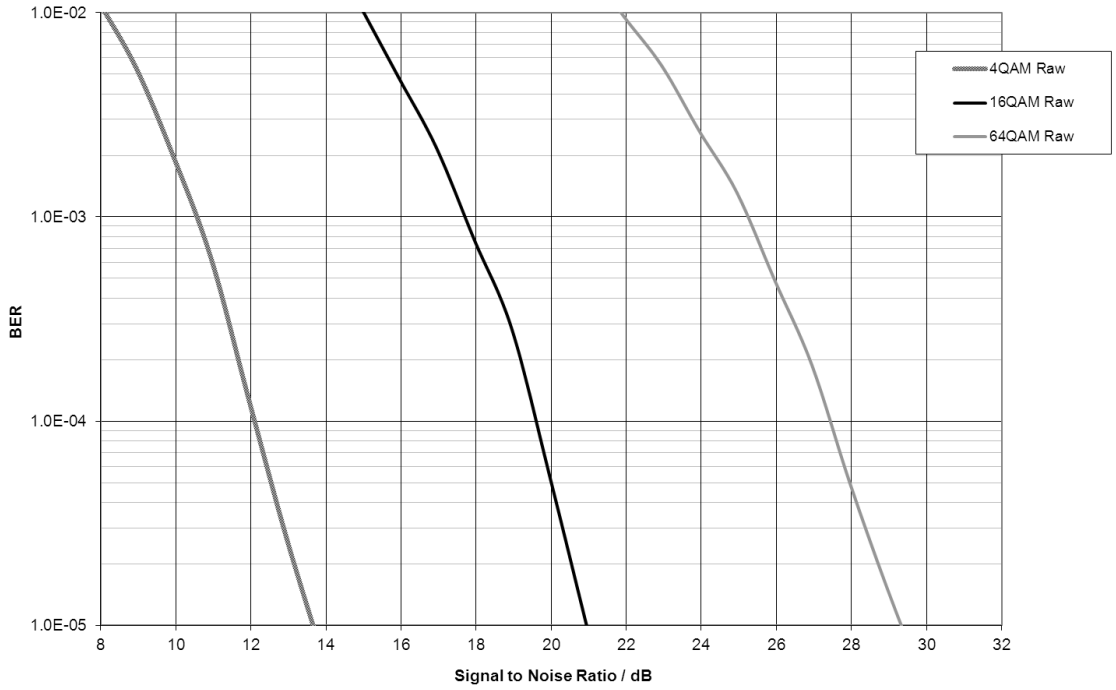


Figure 40 Modem Sensitivity Performance

The co-channel rejection ratio (Figure 41) is measured with an interferer modulated with 400Hz FM and having a deviation of 3kHz; which is 12% of the nominal 25kHz channel bandwidth. This particular interfering signal is used as it is specified in ETSI standard EN 300 113 for co-channel tests. The measurement is taken at approximately 20dB above sensitivity and although this is not in line with

EN 300 113- it means that the data presented here gives a true representation of the performance of the CMX7163 FI-4.x modem rather than being partially influenced by the thermal noise level. The methodology is in line with standards for 6.25kHz channel spaced systems (EN 301 166).

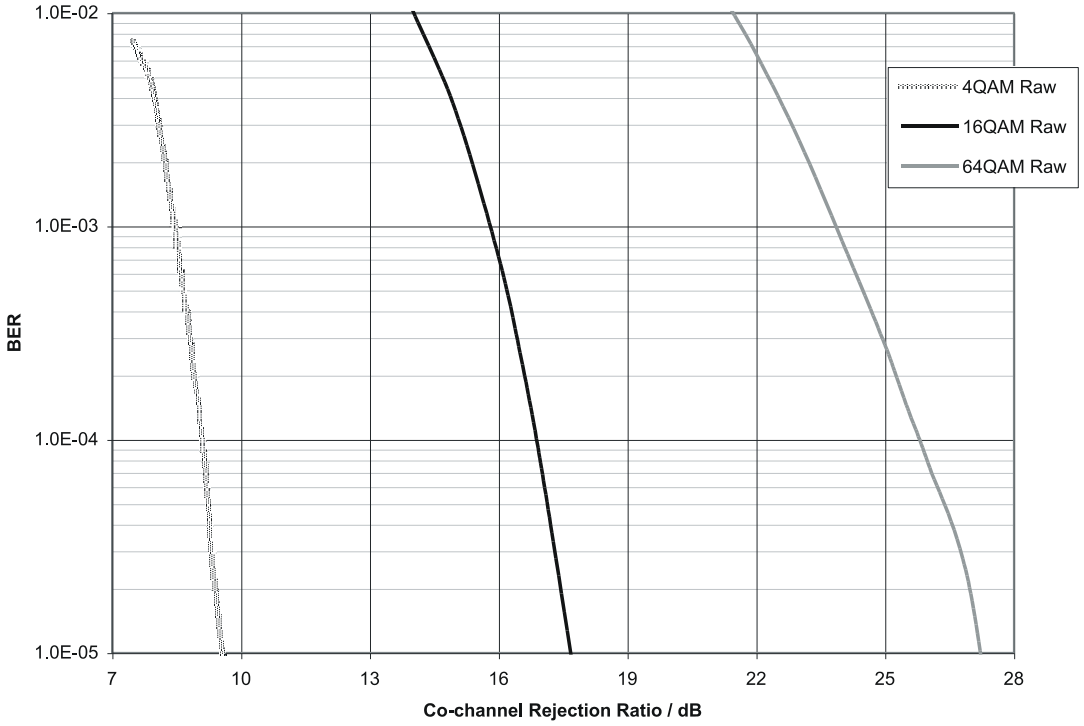


Figure 41 Modem Co-Channel Rejection with FM Interferer (as EN 300 113)

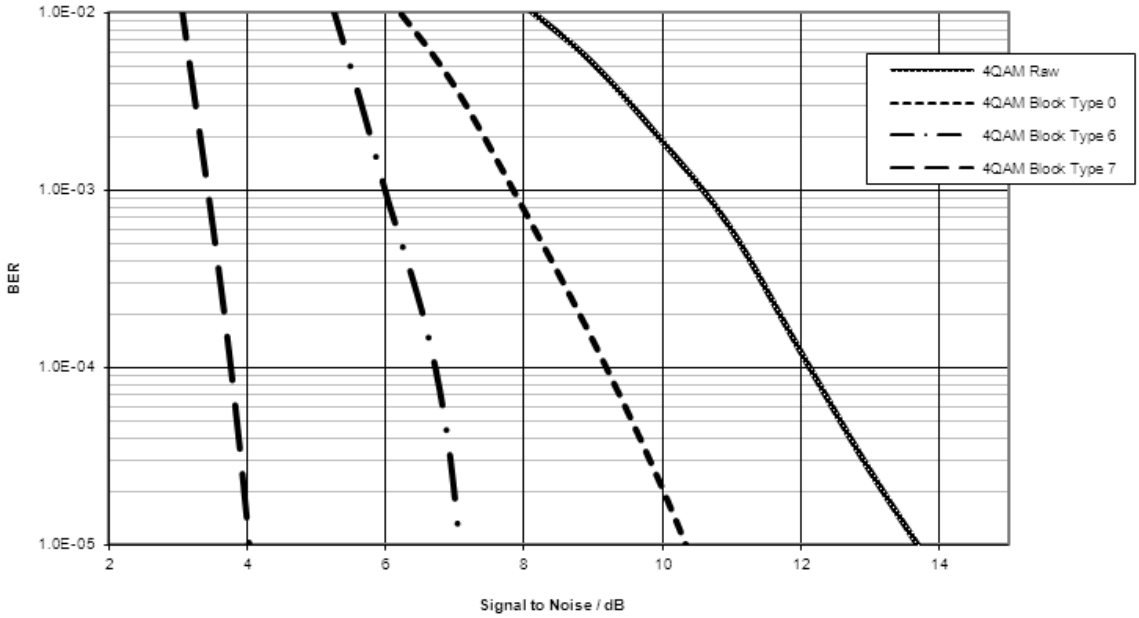


Figure 42 4-QAM Performance with Different Coding Schemes

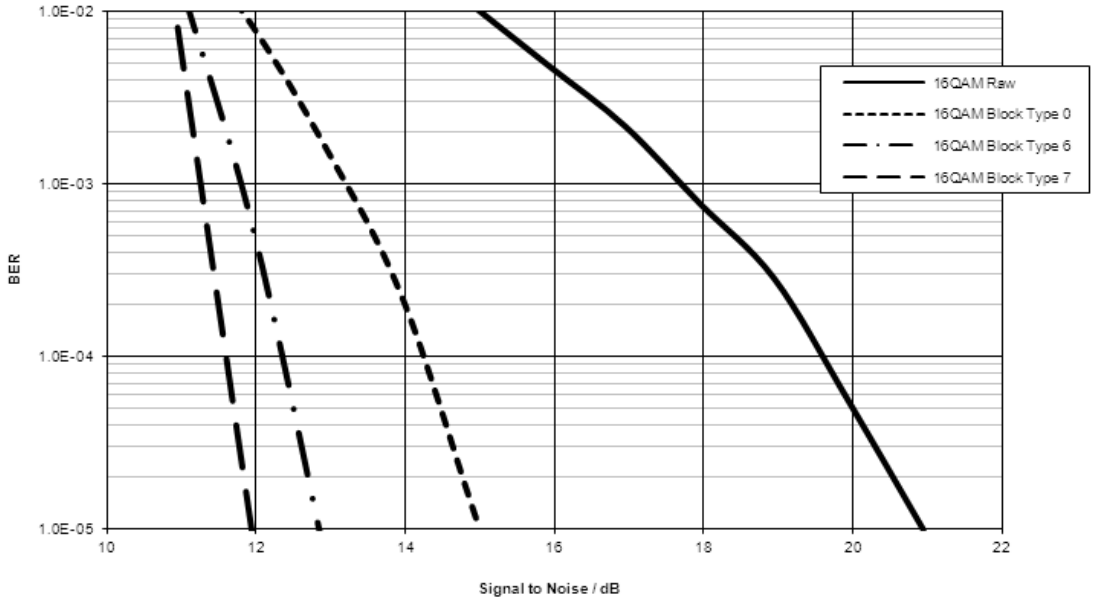


Figure 43 16-QAM Performance with Different Coding Schemes

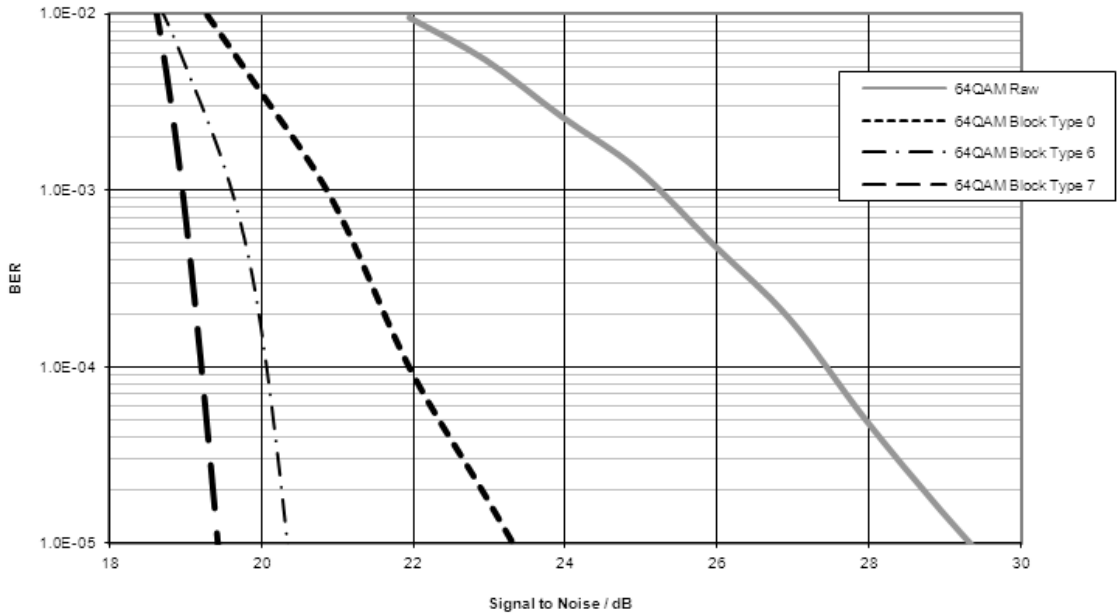


Figure 44 64-QAM Performance with Different Coding Schemes

The required performance of a modem may be assessed in terms of either Bit Error Rate (BER) or Packet Error Rate (PER). The performance of both measures is affected by coding type and block size but the PER also depends on the size of the packet. Short packets with strong coding will exhibit a much lower

PER then a long packet with no coding. A comparison of PER vs BER for 4-QAM modulation is shown in Figure 45 based on packets of 182 bytes. The same comparisons for 16-QAM and 64-QAM are shown in Figure 46 and Figure 47 respectively.

Regulatory standards for radio modem designs using the CMX7163 FI-4.x commonly use either BER or PER to assess the receiver performance. Typical BER assessment values are 5%, 1% or 0.1% whereas PER is most often assessed at 20%. It will be observed from Figure 45 that a 4-QAM modem using no coding (raw mode) with 182-byte packets will achieve 20% PER at just over 13dB SNR while 1% BER is achieved at 9.5dB SNR. With formatted block type 6 (see Table 3), approximately 7dB SNR gives 1% BER and 20% PER.

It is recommended that designers assess the performance of the CMX7163 FI-4.x with the correct bit rate, coding, packet size etc. for their particular application having in mind the regulatory requirements that may apply and paying careful attention to the test methods that will be used.

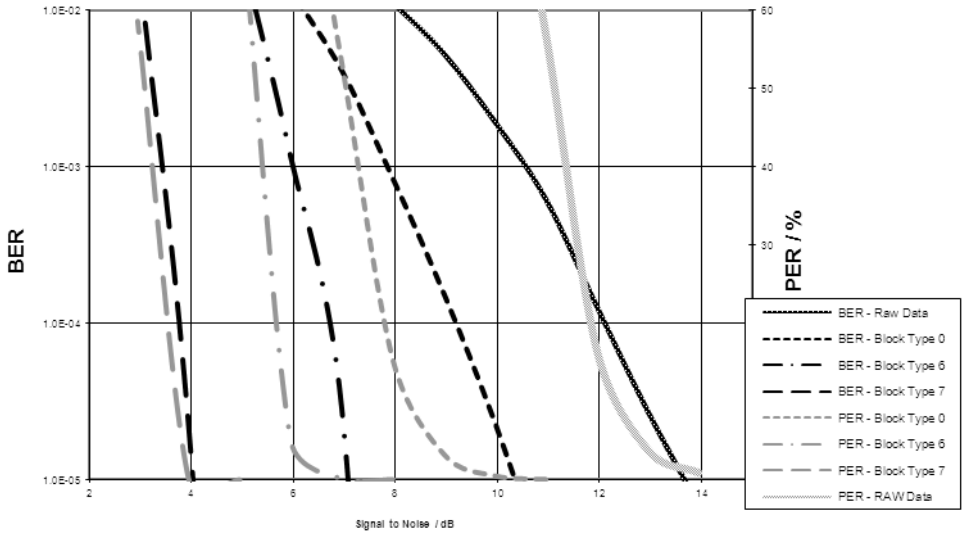


Figure 45 Comparison of BER and PER for 4-QAM Modulation

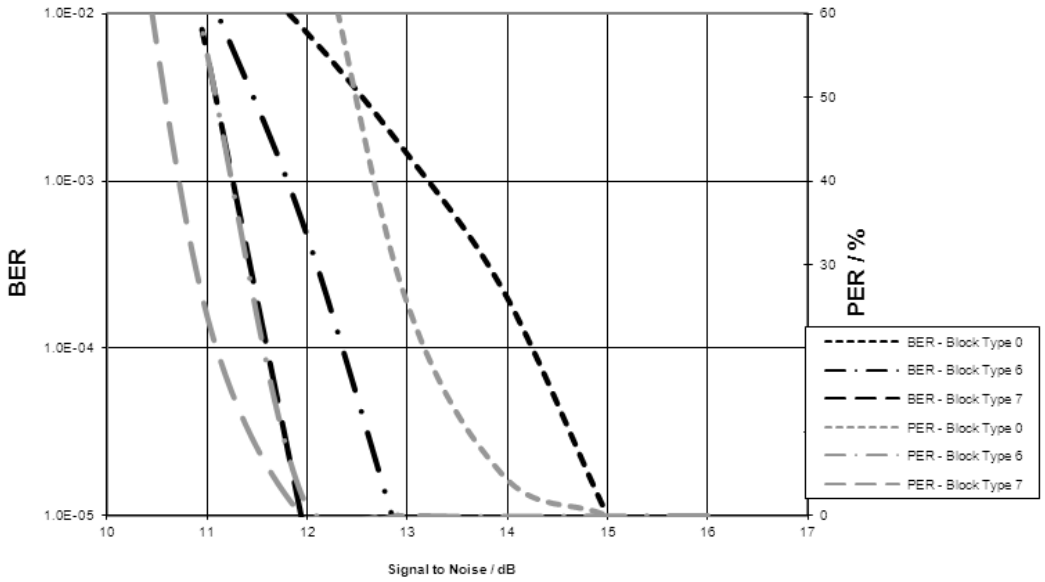


Figure 46 Comparison of BER and PER for 16-QAM Modulation

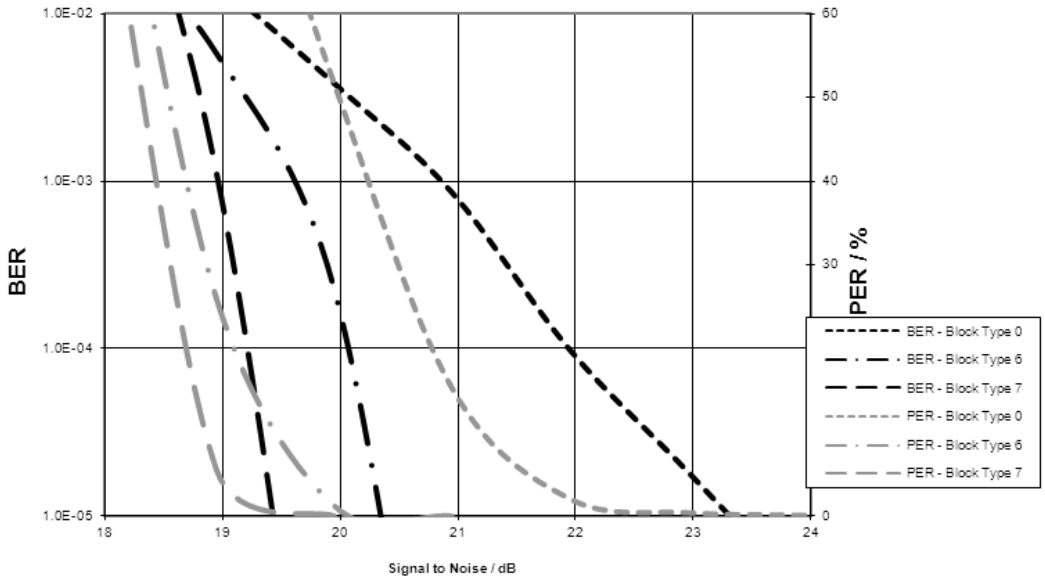


Figure 47 Comparison of BER and PER for 64-QAM Modulation

8.6.2 Adjacent Channel

The CMX7163 FI-4.x provides excellent rejection of adjacent signals present on the I/Q inputs. Assessment of the adjacent channel rejection (ACR) performance of the modem is normally made in terms of BER or PER for a given ratio between the wanted signal (on channel) and larger interferer on the adjacent channel. Detailed measurement methods vary depending on the standards in use, in particular whether the wanted signal is raised above the sensitivity limit and where the reference is taken. The figures quoted here are based on the measurement method from EN 300 113, which tends to give lower

figures than some other methods. In these tests the adjacent channel signal is close to the maximum input signal amplitude allowed by the CMX7163 FI-4.x. The figures quoted in Table 4 are based on the difference between the interferer (400Hz FM modulation, 3kHz deviation) and the mean power of the wanted signal for less than 20% PER (182 byte packets), for 18 ksymbols/s.

It has been observed that adjacent channel rejection is limited by the headroom offered by the I/Q Inputs above the sensitivity level of the input signal. This means that when the adjacent channel interferer reaches the maximum allowed input level of the I/Q Inputs, a rapid transition from almost zero BER to a large BER is observed. Given the relative sensitivity levels of the 4-QAM, 16-QAM and 64-QAM signals the result is a measured adjacent channel rejection of:

Table 4 ACR Rejection Performance

	4-QAM	**16-QAM**	**64-QAM**
Raw Data	62dB (less than 1e-3 BER)	55dB (less than 1e-3 BER)	48dB (less than 1e-3 BER)
Formatted Block Type 0	65dB for 6% PER	62dB (0% PER)	58dB (19% PER)
Formatted Block Type 6	65dB for 0% PER	62dB (0% PER)	58dB (0% PER)
Formatted Block Type 7	65dB for 0% PER	62dB (0% PER)	58dB (0% PER)

The figures in Table 4 are typical of what may be achieved with CMX7163 FI-4.x and a typical I/Q radio receiver with no adjacent channel selectivity in the radio circuits. In a more normal RF architecture some adjacent channel selectivity will be provided making system results better than the measured values for the CMX7163 FI-4.x alone. Furthermore, the results observed are not necessarily the maximum that the CMX7163 can achieve but are limited by the practical dynamic range of the CMX7163 combined with the system gain and noise figure of the receiver used in these tests.

8.6.3 Receiver Dynamic Range

The adjacent channel rejection results in section 8.6.2 also indicate that a wanted signal can be successfully received over the dynamic range stated in Table 4 without any need for an AGC. Note that this is limited at the top end by the maximum allowed signal amplitude into the CMX7163, but performance at the bottom end is affected by noise added by the test receiver – so these figures are not the absolute limit of CMX7163 FI-4.x performance.

8.6.4 Receiver Response Equaliser Performance

The performance of the CMX7163 when receiving a signal through a typical IF crystal filter as used in EV9910B/EV9920B[6] is shown in the following graphs. The nominal bandwidth of the filter is 15kHz, however its response within that bandwidth is not flat, both amplitude and group delay distortion is introduced into the signal.

The following tests were carried out using a 16 ksymbols/s 4-QAM, 16-QAM or 64-QAM signal. Where the results are quoted as using no equalisation the Receiver Response Equaliser was disabled. Where the results are quoted as Equalised the Receiver Response Equaliser was provided with a 4-QAM training sequence of level –70dBm which produced 400mV (differential) on the I and Q inputs. Equaliser gain was set to 3000 and training lasted for 800 symbol periods. While training the received signal had less than 100Hz frequency error. Once trained the resulting equaliser coefficients were used for the remaining tests.

Firstly the signal to noise performance of equalised and non equalised received signals are compared. The test is similar to that described in 8.6.1 Signal to Noise and Co-channel, except that as the baud rate is 16 ksymbols/s the RxBW parameter is 16000. Applying this factor also means that the results in section 8.6.1 may be directly compared to those below in Figure 48.

[6] Evaluation card for CMX991 / CMX992 RF Quadrature Transceiver / Receiver ICs.

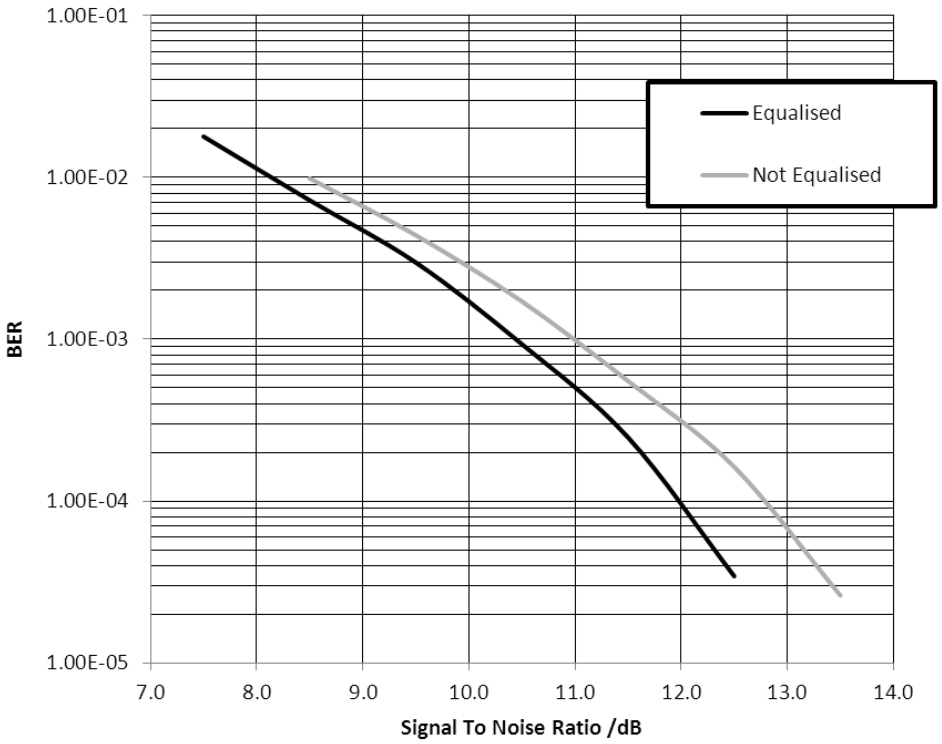


Figure 48 4-QAM Signal to Noise Performance, Equalised and Not Equalised

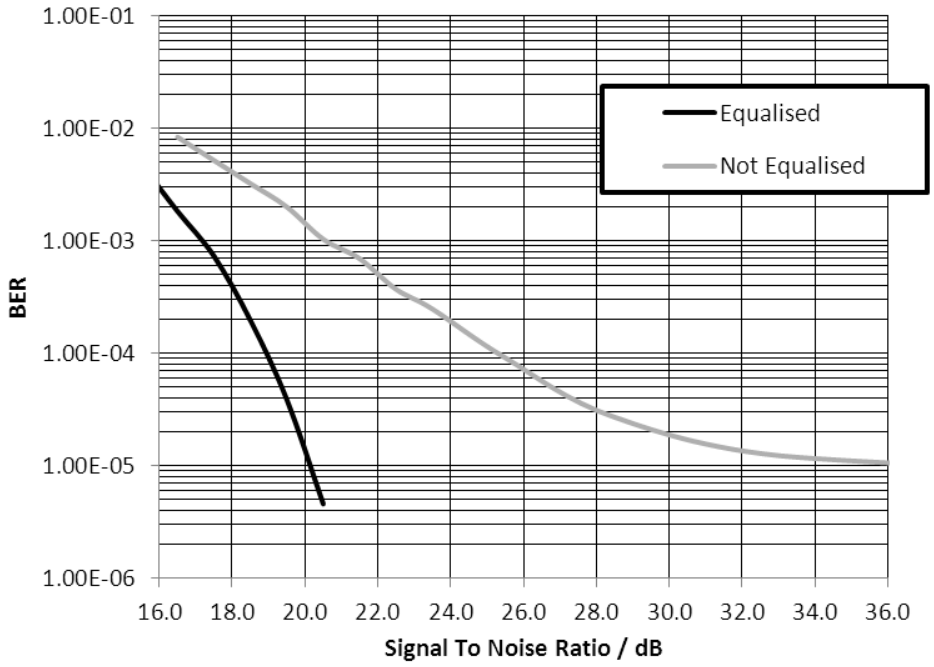


Figure 49 16-QAM Signal to Noise Performance, Equalised and Not Equalised

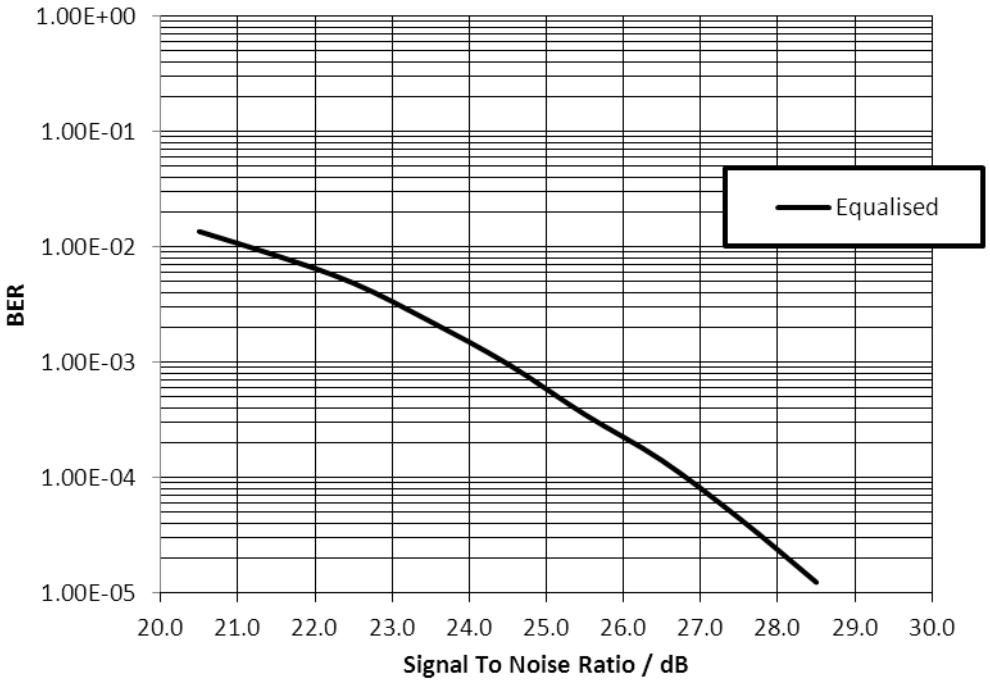


Figure 50 64-QAM Signal to Noise Performance, Equalised

Figure 48, Figure 49 and Figure 50 show that equaliser training improves the received signal performance in all cases: 4-QAM, 16-QAM and 64-QAM. We can see that without equalisation 16-QAM signals have a residual bit error rate even with a high signal level, as the non equalised curve flattens off. 64-QAM is unusable without equalisation, producing a residual bit error rate of greater than 1e-2 regardless of signal to noise ratio. This is not plotted in Figure 50. The 4-QAM curves show that 4-QAM is less affected by the receiver response, therefore the improvement made by equalisation is less. Once equalisation is present the measured figures compare well to the results (with no crystal filter in the receive path) in section 8.6.1 Signal to Noise and Co-channel.

The response of crystal filters varies with temperature. This will affect the ability of an equaliser which is trained at room temperature to compensate effectively for filter distortions at a different temperature. Measurements showing the degradation in signal to noise performance over temperature when the equaliser was trained at room temperature are shown in Figure 51.

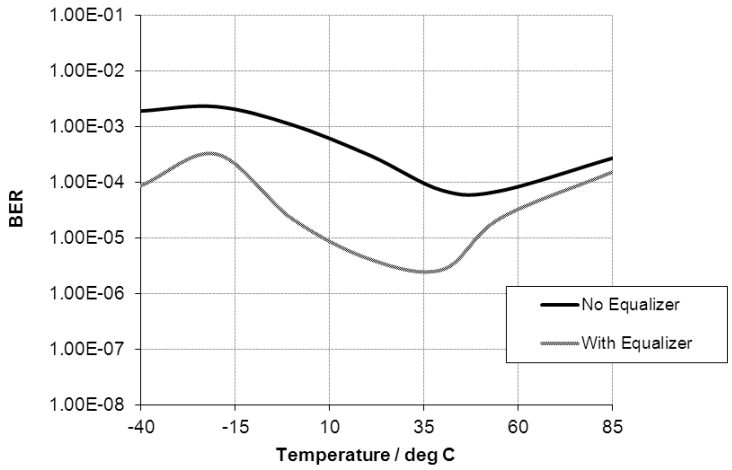


Figure 51 Performance of 16-QAM equalised signals with temperature variation

Equaliser performance with temperature variation was measured by calibrating the receiver response equaliser at room temperature. Tests were carried out using 16-QAM modulation with a signal level of -103dBm (Figure 51) and a signal level of –95dBm for 64-QAM (Figure 52), in both cases using the EV9910B[7]. BER performance was measured with and without equalisation being applied then the temperature was varied and the equalised and non-equalised bit error rate measurements repeated.

The results are shown in Figure 51 and Figure 52. The results show that equalisation is most effective at the temperature at which calibration was carried out and that performance degrades outside of this temperature. For all results a frequency error between transmitter and receiver of less than 100Hz magnitude was observed.

As the crystal filter was that used in the EV9910B/EV9920B, it should be noted that its specified range of operation is -20 to +55 deg C. It was also observed that a re-calibration at a given temperature would result in equalisation coefficients capable of producing a much improved BER at that temperature.

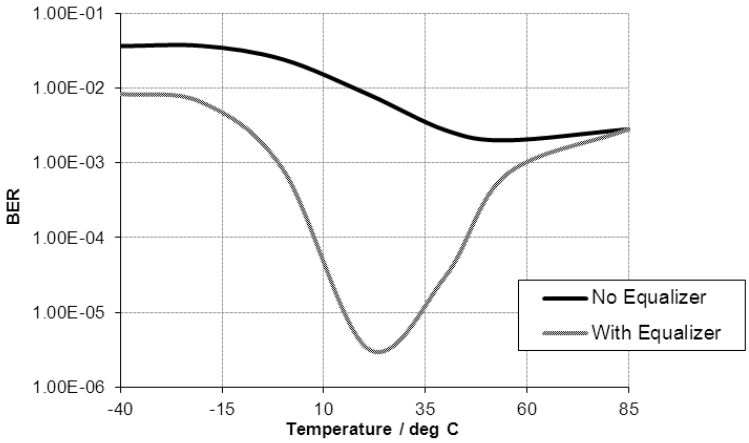


Figure 52 Performance of 64-QAM equalised signals with temperature variation

[7] Evaluation card for CMX991 / CMX992 RF Quadrature Transceiver / Receiver ICs.

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25ºC		1690	mW
... Derating		16.9	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25ºC		3500	mW
... Derating		35.0	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
Voltage differential between power supplies:				
DV_{DD} and AV_{DD}	0	–	0.3	V
DV_{SS} and AV_{SS}	0	–	50	mV
Operating Temperature	-40	–	+85	°C
Xtal Frequency	3.0	–	12.288	MHz
External Clock Frequency	3.0	–	24.576	MHz

9.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

External components as recommended in Section 5, External Components.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz±0.002% (20ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.

Current consumption figures quoted in this section apply to the device when loaded with FI-4.x only. Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current (see also section 9.1.4)	11				
All Powersaved					
AI_{DD} + DI_{DD}	10,15	–	1.0	–	µA
Idle Mode	12,15				
DI_{DD}	13	–	550	–	µA
AI_{DD}		–	17	–	µA
Additional Current for one Auxiliary System Clock (output running at 5MHz – SYSCLKPLL active)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	900	–	µA
Additional Current for one Auxiliary System Clock (output running at 4.8MHz – SYSCLKPLL not required)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	675	–	µA
Additional Current for each Auxiliary ADC	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	190	–	µA
Additional Current for each Auxiliary DAC	14,15				
AI_{DD} (AV_{DD} = 3.3V)		–	210 to 370	–	µA

Notes:
10 Idle mode with V_{BIAS} disabled.
11 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
12 System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled and V_{BIAS} enabled.
13 Using a 19.2MHz external clock input, Xtal oscillator circuit powered down.
14 A lower current is measured when outputting the smallest possible dc level from an AuxDAC, a higher current is measured when outputting the largest possible dc value.
15 Using a 19.2MHz external clock input.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	11	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	11	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes:

20 Characteristics when driving the XTAL/CLK pin with an external clock source.

21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor, as shown in section 4 PCB Layout Guidelines and Power Supply Decoupling.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
SYSCLK1/2 Outputs						
SYSPLL Operating Frequency			38	–	250	MHz
SYSCLK1/2 Output Frequency			–	–	20	MHz
Rise Time			–	–	13.5	ns
Fall Time			–	–	6	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Differential I and Q Inputs						
Input Impedance, Enabled		31	10	–	140	kΩ
Input Impedance, Muted or Powersaved				200		kΩ
Maximum Input Voltage Excursion		32	–	–	20 to 80	%AV_{DD}
Programmable Input Gain Stage						
Gain (at 0dB)		33	−0.5	0	+0.5	dB
Cumulative Gain Error (w.r.t. attenuation at 0dB)		33	−1.0	0	+1.0	dB

Notes:

30 Timing for an external input to the XTAL/CLOCK pin.

31 With no external components connected.

32 For each input pin and for AV_{DD} = 3.3V, the maximum allowed signal swing is: (3.3 x 0.8) - (3.3 x 0.2) = 2.0V.

33 Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
Modulator I/Q Outputs (I Output, Q Output)						
Power-up to Output Stable		40	–	50	100	µs
I/Q Output coarse gain Attenuators						
Attenuation (at 0dB)		42	–0.2	0	+0.2	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		42	–0.6	0	+0.6	dB
Output Impedance	Enabled	41	–	600	–	Ω
	Disabled	41	–	TBD	–	kΩ
Output Voltage Range		43, 44	0.3	–	AV_{DD}-0.3	V
Load Resistance			20	–	–	kΩ

Notes:

40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

42 Figures relate to attenuator block only. Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

43 For each output pin. With respect to the output driving a 20kΩ load to $AV_{DD}/2$.

44 The levels of I/Q Output Fine Gain and Offset (registers $5D and $5E) should be adjusted so that the output voltage remains between 20% and 80% of AV_{DD} on each output pin (when 0dB of coarse output gain is used). This will produce the best performance when the device operates with AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AuxADC1-4)					
Source Output Impedance	50	–	–	24	kΩ
Auxiliary 10-Bit ADCs					
Resolution		–	10	–	Bits
Conversion Time	51	–	225	–	µs
Sample Rate		1	-	512	Hz
Input Impedance					
Resistance		–	TBD	–	MΩ
Capacitance		–	5	–	pF
Offset Error	54, 55	–	–	±18	mV
Integral Non-linearity	54, 55	–	–	±2	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs
Auxiliary 10-Bit DACs					
Resolution		–	10	–	Bits
Conversion Time	51		60		µs
Settling Time to 0.5 LSB			10		µs
Offset Error	54, 55	–	–	±20	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity	54, 55	–	–	±4	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs

Notes:

50 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

51 Typical – based on 9.6MHz Xtal or external oscillator

52 Guaranteed monotonic with no missing codes.

54 Specified between 2.5% and 97.5% of the full-scale range.

55 Calculated from the line of best fit of all the measured codes.

9.1.4 CMX7163 FI-4.x Parametric Performance

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

External components as recommended in section 5.
Maximum load on digital outputs = 30pF.
Clock source = 19.2MHz ±0.002% (20ppm) clock input; Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-4.x only. The use of other Function Images™, can modify the parametric performance of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (9600symbols/s – search for FS)	60	–	15.7 to 21.0	–	mA
DI_{DD} (18000symbols/s – search for FS)	60	–	24.1 to 34.1	–	mA
DI_{DD} (9600symbols/s – FS found)		–	11.0	–	mA
DI_{DD} (18000symbols/s – FS found)		–	15.4	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	7.7	–	mA
Tx Mode	61				
DI_{DD} (9600 symbols/s)		–	7.5	–	mA
DI_{DD} (18000 symbols/s)		–	11.1	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	8.0	–	mA

Notes:

60 A lower current is measured when searching for Framesync1, a higher current is measured when doing automatic modulation detection.

61 Transmitting continuous 16-QAM PRBS, all GPIOs and RAMDAC set to manual.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2000		20000	sym s^{-1}
Modulation			QAM		
Filter RRC Alpha	76		0.2 or 0.35		
Tx Bit-rate Accuracy	70		-		ppm
Tx Output Level (I Output, Q Output)	71		TBD		Vp-p
Tx Adjacent Channel Power (I Output, Q Output, PRBS)	72	-	-	-	dB
Rx Frequency Error Tolerated	75		+/- 1.0		kHz
Rx Co-channel Rejection	73	-	-	-	dB
Rx Adjacent Channel Rejection	73	-	-	-	dB

Notes:

70 Determined by the accuracy of the Xtal oscillator provided.

71 Transmitting continuous default preamble.

72 See section 8.5 CMX7163 FI-4.x Typical Transmit Performance

73 See section 8.6 CMX7163 FI-4.x Typical Receive Performance

75 Optimum performance is achieved with 0Hz frequency error. The figure quoted is for a symbol rate of 18ksymbols/s. The frequency error tolerated is proportional to the symbol rate.

76 A user programmable filter option is also provided, allowing for compensation for external hardware and different α values than those provided.

9.2 C-BUS Timing

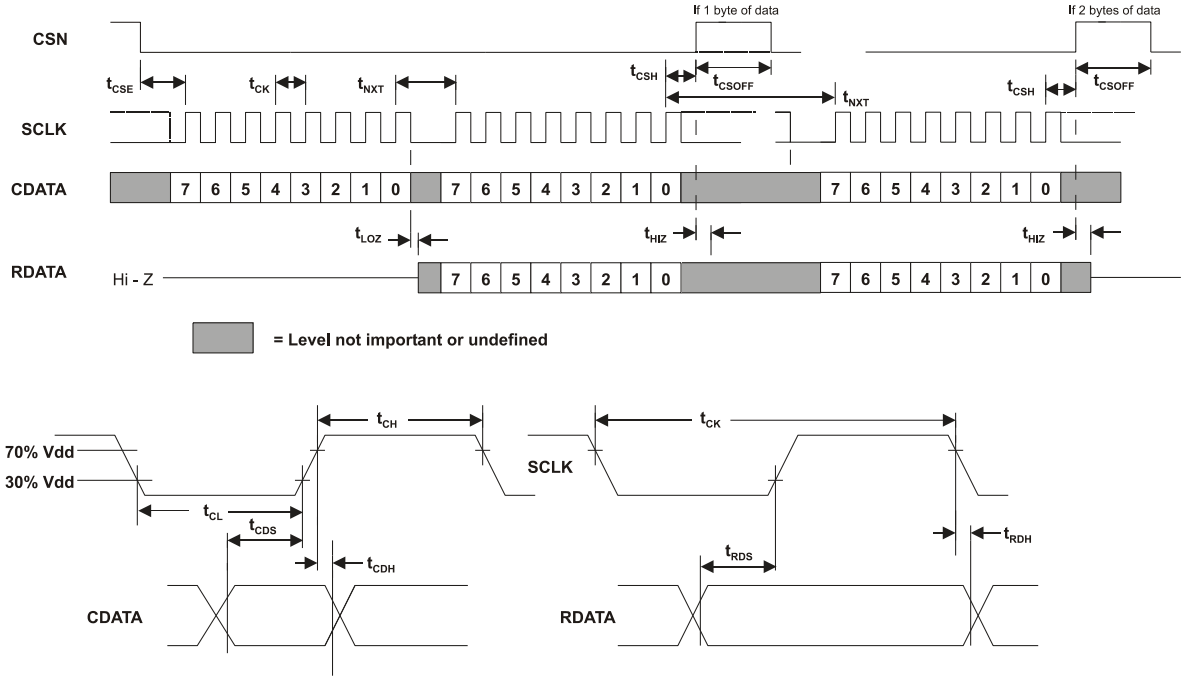


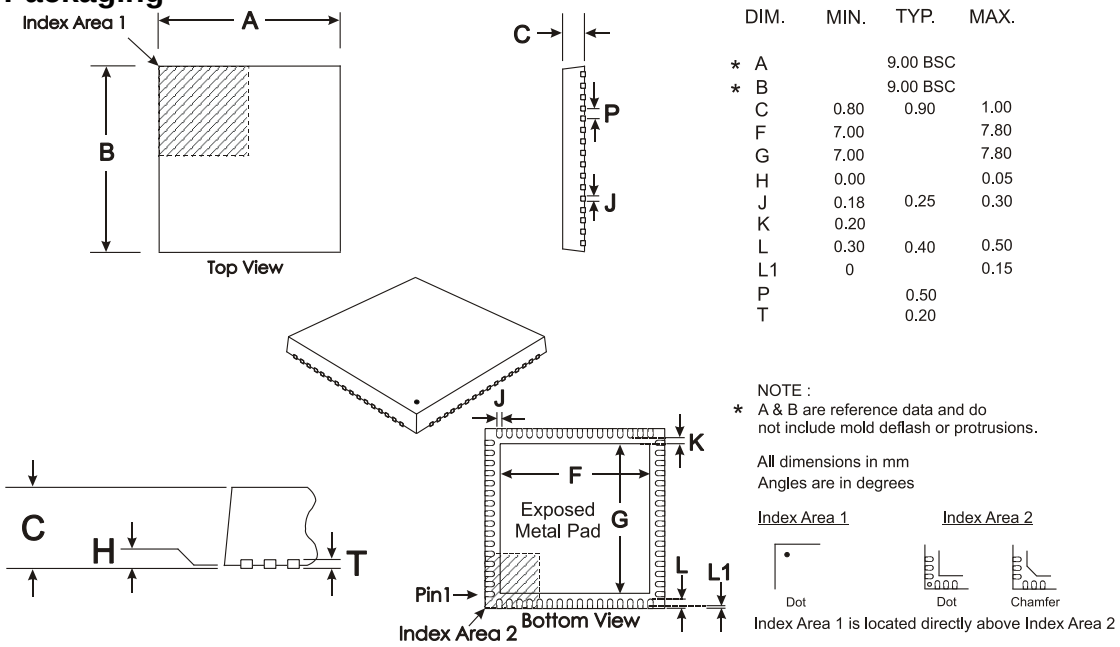
Figure 53 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		100	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA set-up time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA set-up time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7163 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

9.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

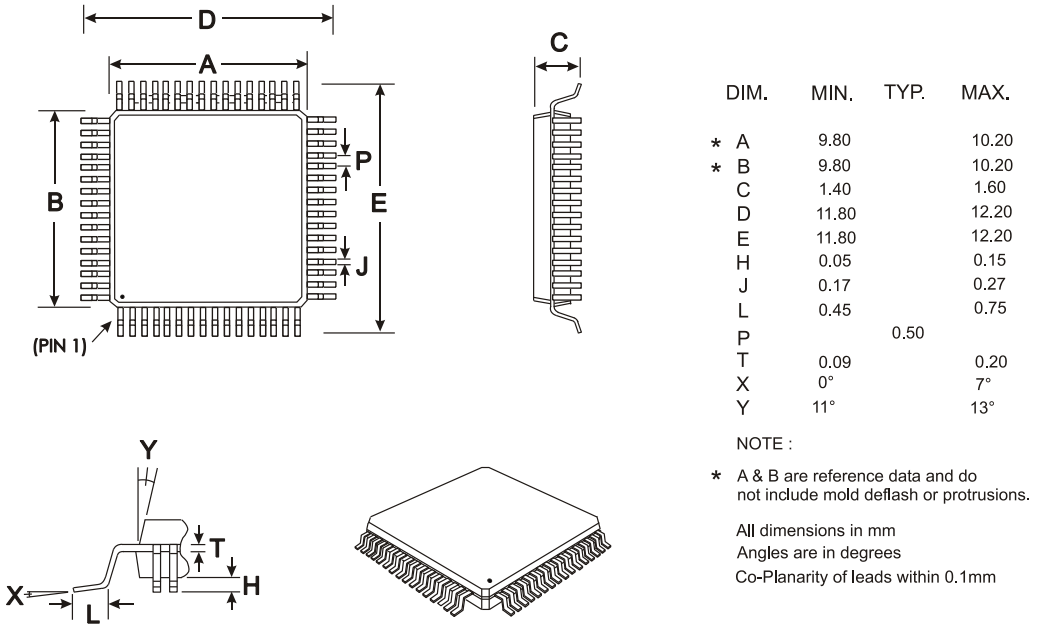
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 54 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7163Q1



DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 55 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7163L9

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

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