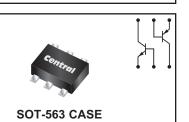
#### **CMLT4413**

## SURFACE MOUNT SILICON **DUAL, COMPLEMENTARY TRANSISTOR**



Semiconductor Cor

www.centralsemi.com

## **DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMLT4413 consists of one isolated 2N4401 NPN silicon transistor and one complementary isolated 2N4403 PNP silicon transistor, manufactured by the epitaxial planar process and epoxy molded in an SOT-563 surface mount package. This device is designed for small signal general purpose amplifier and switching applications.

DND (O2)

**MARKING CODE: PC3** 

•	Device	İS	Hal	logen	Free	by	design
---	--------	----	-----	-------	------	----	--------

MAXIMUM RATINGS: (T <sub>A</sub> =25°C)	SYMBOL	NPN (Q1)	PNP (Q2)	UNITS
Collector-Base Voltage	$V_{CBO}$	60	40	V
Collector-Emitter Voltage	VCEO	40	40	V
Emitter-Base Voltage	$V_{EBO}$	6.0	5.0	V
Continuous Collector Current	l <sub>C</sub>	60	00	mA
Power Dissipation (Note 1)	$P_{D}$	35	50	mW
Power Dissipation (Note 2)	$P_{D}$	30	00	mW
Power Dissipation (Note 3)	$P_{D}$	15	50	mW
Operating and Storage Junction Temperature	T <sub>J</sub> , T <sub>stg</sub>	-65 to	+150	°C
Thermal Resistance	$\Theta_{JA}$	35	57	°C/W

# ELECTRICAL CHARACTERISTICS: (T<sub>A</sub>=25°C unless otherwise noted) NPN (Q1)

		NPN	(Q1)	PNP	' (Q2)	
SYMBOL	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNITS
ICEV	$V_{CE} = 35V, V_{EB} = 0.4V$	-	0.1	-	0.1	μΑ
I <sub>BEV</sub>	$V_{CE} = 35V, V_{EB} = 0.4V$	-	0.1	-	0.1	μΑ
BVCBO	I <sub>C</sub> =100μA	60	-	40	-	V
<b>BVCEO</b>	I <sub>C</sub> =1.0mA	40	-	40	-	V
<b>BV</b> EBO	I <sub>E</sub> =100μA	6.0	-	5.0	-	V
V <sub>CE</sub> (SAT)	I <sub>C</sub> =150mA, I <sub>B</sub> =15mA	-	0.40	-	0.40	V
VCE(SAT)	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA	-	0.75	-	0.75	V
V <sub>BE</sub> (SAT)	I <sub>C</sub> =150mA, I <sub>B</sub> =15mA	0.75	0.95	0.75	0.95	V
V <sub>BE</sub> (SAT)	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA	-	1.2	-	1.3	V
h <sub>FE</sub> ` ′	V <sub>CE</sub> =1.0V, I <sub>C</sub> =0.1mA	20	-	30	-	
h <sub>FE</sub>	V <sub>CE</sub> =1.0V, I <sub>C</sub> =1.0mA	40	-	60	-	
hFE	V <sub>CE</sub> =1.0V, I <sub>C</sub> =10mA	80	-	100	-	
hFE	V <sub>CE</sub> =1.0V, I <sub>C</sub> =150mA	100	300	-	-	
h <sub>FE</sub>	V <sub>CE</sub> =2.0V, I <sub>C</sub> =150mA	-	-	100	300	
hFE	V <sub>CE</sub> =2.0V, I <sub>C</sub> =500mA	40	-	20	-	
f <sub>T</sub>	V <sub>CE</sub> =10V, I <sub>C</sub> =20mA, f=100MHz	250	-	200	-	MHz
C <sub>ob</sub>	V <sub>CB</sub> =5.0V, I <sub>E</sub> =0, f=1.0MHz	-	6.5	-	8.5	pF
C <sub>ib</sub>	V <sub>BE</sub> =0.5V, I <sub>C</sub> =0, f=1.0MHz	-	30	-	30	pF

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm<sup>2</sup>

R3 (29-June 2015)

<sup>(2)</sup> FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm<sup>2</sup>
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm<sup>2</sup>

## **CMLT4413**

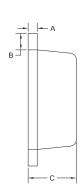
## SURFACE MOUNT SILICON DUAL, COMPLEMENTARY TRANSISTOR

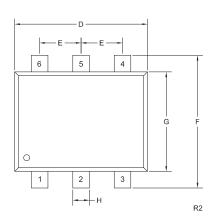


ELECTRICAL CHARACTERISTICS - Continued: (T<sub>A</sub>=25°C)

LLLOTINO	LEEGTHOAL GHANAGTERIOTIOG - Continued. (TA-25 O)					
		NPN	l (Q1)	PNP	(Q2)	
SYMBOL	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNITS
h <sub>ie</sub>	$V_{CE}$ =10V, $I_{C}$ =1.0mA, f=1.0kHz	1.0	15	1.5	15	kΩ
h <sub>re</sub>	$V_{CE}$ =10V, $I_{C}$ =1.0mA, f=1.0kHz	0.1	8.0	0.1	8.0	x10 <sup>-4</sup>
h <sub>fe</sub>	$V_{CE}=10V, I_{C}=1.0mA, f=1.0kHz$	40	500	60	500	
h <sub>oe</sub>	$V_{CE}$ =10V, $I_{C}$ =1.0mA, f=1.0kHz	1.0	30	1.0	100	μS
$t_{d}$	$V_{CC}$ =30V, $V_{BE}$ =2.0V, $I_{C}$ =150mA, $I_{B1}$ =15mA	-	15	-	15	ns
t <sub>r</sub>	$V_{CC}$ =30V, $V_{BE}$ =2.0V, $I_{C}$ =150mA, $I_{B1}$ =15mA	-	20	-	20	ns
$t_{S}$	$V_{CC}$ =30V, $I_{C}$ =150mA, $I_{B1}$ = $I_{B2}$ =15mA	-	225	-	225	ns
t <sub>f</sub>	V <sub>CC</sub> =30V, I <sub>C</sub> =150mA, I <sub>B1</sub> =I <sub>B2</sub> =15mA	-	30	-	30	ns

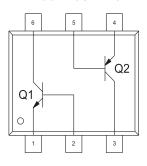
#### **SOT-563 CASE - MECHANICAL OUTLINE**





DIMENSIONS					
	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	
Α	0.0027	0.007	0.07	0.18	
В	0.0	800	0.20		
С	0.017	0.024	0.45	0.60	
D	0.059	0.067	1.50	1.70	
E	0.020		0.50		
F	0.059	0.067	1.50	1.70	
G	0.043	0.051	1.10	1.30	
Н	0.006	0.012	0.15	0.30	
SOT-563 (REV: R2)					

# PIN CONFIGURATION



# LEAD CODE:

- 1) Emitter Q1
- 2) Base Q1
- 3) Collector Q2
- 4) Emitter Q2
- 5) Base Q2
- 6) Collector Q1

MARKING CODE: PC3

R3 (29-June 2015)

#### **CMLT4413**





#### **SERVICES**

- · Bonded Inventory
- · Custom Electrical Screening
- Custom Electrical Characteristic Curves
- SPICE Models
- Custom Packaging
- Package Base Options
- Custom Device Development/Multi Discrete Modules (MDM™)
- · Bare Die Available for Hybrid Applications

**LIMITATIONS AND DAMAGES DISCLAIMER:** In no event shall Central be liable for any collateral, indirect, punitive, incidental, consequential, or exemplary damages in connection with or arising out of a purchase order or contract or the use of products provided hereunder, regardless of whether Central has been advised of the possibility of such damages. Excluded damages shall include, but not be restricted to: cost of removal or reinstallation, rework, ancillary costs to the procurement of substitute products, loss of profits, loss of savings, loss of use, loss of data, or business interruption. No claim, suit, or action shall be brought against Central more than two (2) years after the related cause of action has occurred.

In no event shall Central's aggregate liability from any warranty, indemnity, or other obligation arising out of or in connection with a purchase order or contract, or any use of any Central product provided hereunder, exceed the total amount paid to Central for the specific products sold under a purchase order or contract with respect to which losses or damages are claimed. The existence of more than one (1) claim against the specific products sold to Buyer under a purchase order or contract shall not enlarge or extend this limit.

Buyer understands and agrees that the foregoing liability limitations are essential elements of a purchase order or contract and that in the absence of such limitations, the material and economic terms of the purchase order or contract would be substantially different.

R3 (29-June 2015)