SONY

CXD2719Q

DOLBY SURROUND PRO • LOGIC

Single-Chip Dolby Pro Logic Surround Decoder

Description

The CXD2719Q is a CMOS LSI developed for Dolby Pro Logic Surround. A SRAM for short delay and AD/DA converters are built in, and all functions necessary for Dolby Pro Logic Surround such as an adaptive matrix, a passive decoder including BNR, auto input balance, a noise sequencer and center channel mode control are contained on a single chip.

Features

- Dolby Pro Logic Surround decoding with a single chip
- 2-channel 1-bit AD converter, decimation filter and prefilter operational amplifier
- 4-channel 1-bit DA converter, oversampling filter and post filter
- Analog switch for DSP bypass
- Analog electronic attenuator (+1.5 to –29.5dB) for center/surround channel trim
- 24K-bit SRAM for short delay
- No separation or other variance for digital processing
- External parts reduced by incorporating analog circuits

Functions

- Adaptive matrix
- Center channel mode control (Normal/Phantom/Wide)
- Dolby 3 Stereo
- Auto input balance control (ON/OFF)
- Noise sequencer
- Variable delay time (0 to 34.8ms)
- 7 kHz low-pass filter (12dB/Oct)
- Modified Dolby B-type NR
- Simple SFC function
- SFC mode
- DSP bypass mode (L, R-channel through)

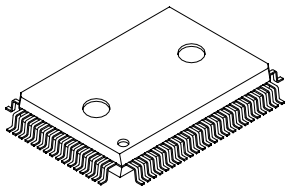
Structure

Silicon gate CMOS

Applications

Equipment having Dolby Pro Logic Surround function such as AV amplifiers, receivers and compact music systems

80 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +70	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}		
Analog system		4.75 to 5.25 (5.0 typ.)	V
Digital system		4.50 to 5.25 (5.0 typ.)	V
• Operating temperature	Ta	–20 to +70	°C

Input/Output Capacitance

• Input capacitance	C_{IN}	9 (max.)	pF
• Output capacitance	C_{OUT}	11 (max.)	pF
• Input/output capacitance	$C_{I/O}$	11 (max.)	pF

* Measurement conditions: V_{DD} = V_I = 0V, F = 1MHz

Maximum Current Consumption

(Ta = 25°C, V_{DD} = 5.25V)

- Digital/analog block total: 166.7mA

Dolby level

- During analog input: 200 to 300mVrms
- During digital input: –20dBFS

Analog characteristics

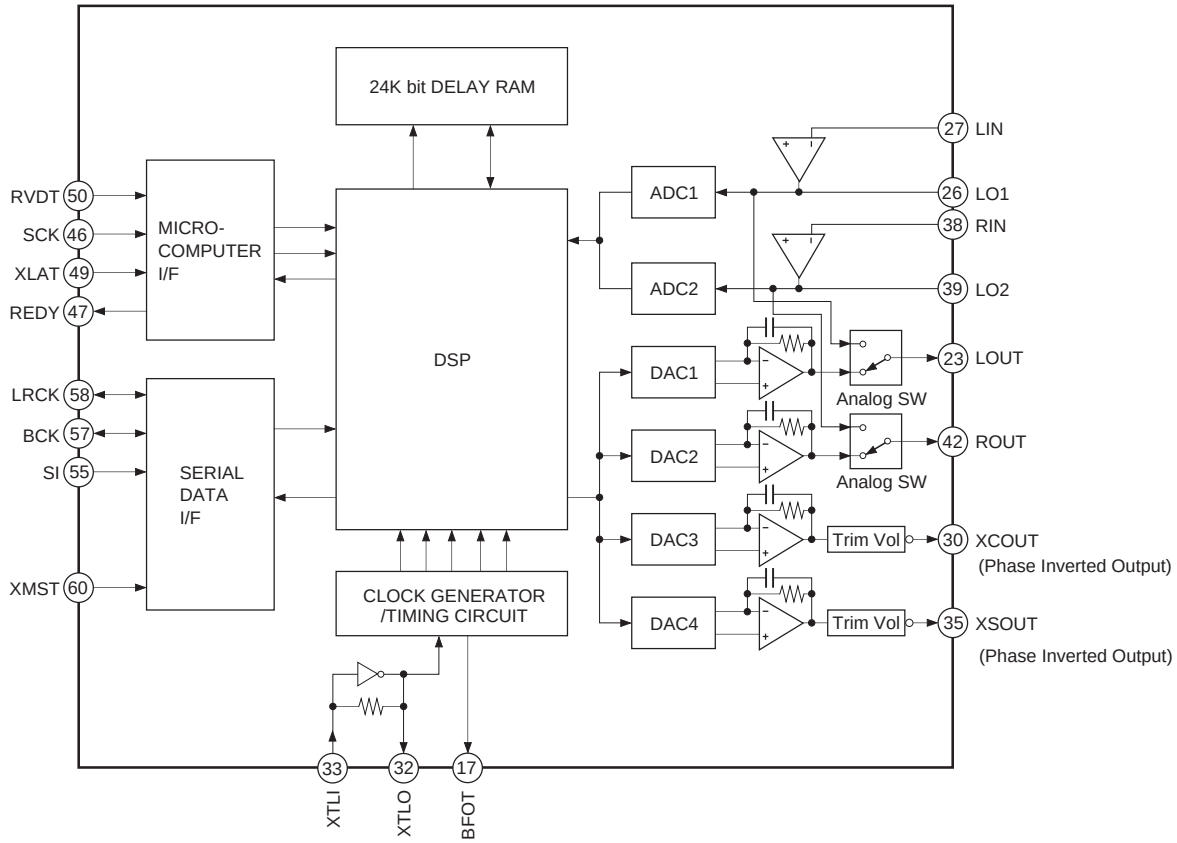
Pro Logic ON: Dolby level = 300mVrms
Prefilter gain = –3.52dB

- S/N: L, Rch = 80dB, C, Sch = 72dB
- THD + N: L, Rch = 0.015%, C, Sch = 0.03%

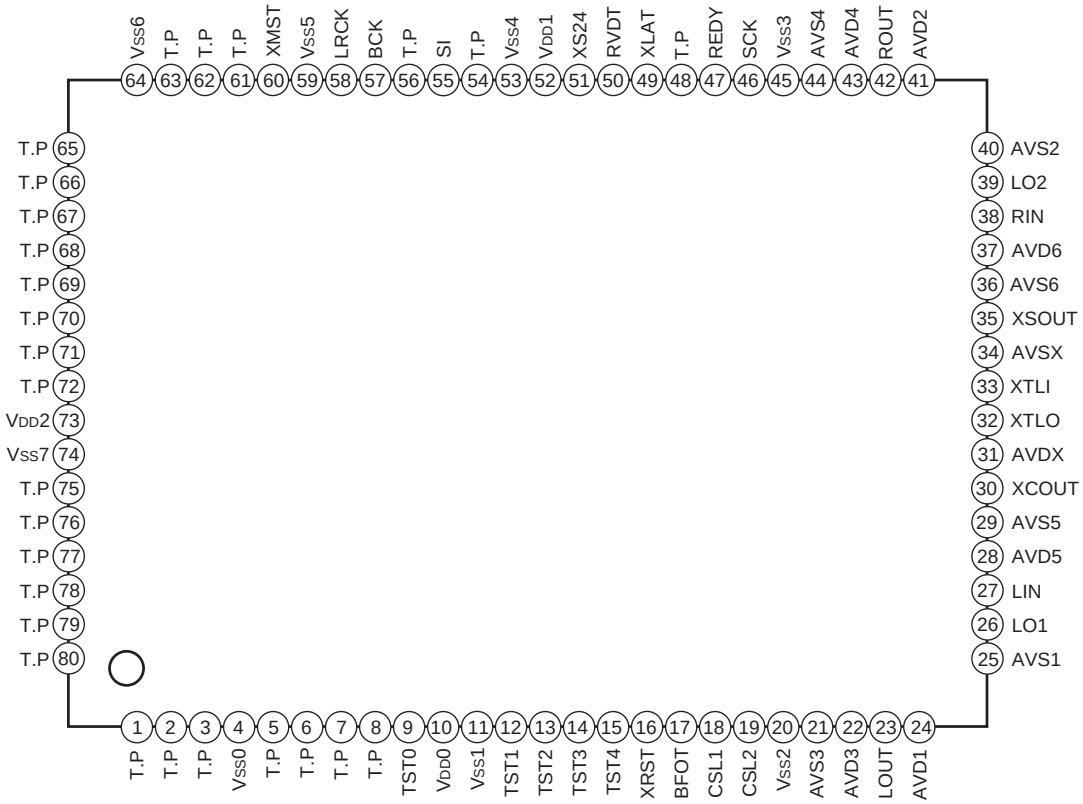
* All values for typ.

E98944-PS

Block Diagram



Pin Configuration



Pin Description Notations in parentheses indicate the fixed pin connection status.

Pin No.	Symbol	I/O	Description
1 to 3	T.P	O	Test monitor. Normally outputs Low. (OPEN)
4	$V_{SS}0$	—	Digital GND. (V_{SS})
5 to 8	T.P	O	Test monitor. Normally outputs Low. (OPEN)
9	TST0	I	Test. Normally fixed Low. (V_{SS})
10	$V_{DD}0$	—	Digital power supply. (V_{DD})
11	$V_{SS}1$	—	Digital GND. (V_{SS})
12	TST1	I	Test. Normally fixed Low. (V_{SS})
13	TST2	I	Test. Normally fixed Low. (V_{SS})
14	TST3	I	Test. Normally fixed Low. (V_{SS})
15	TST4	I	Test. Normally fixed Low. (V_{SS})
16	XRST	I	System reset input. Reset when Low.
17	BFOT	O	Clock, frequency-division output. [384/768/256/512fs]
18	CSL1	I	Test. Normally fixed High. (V_{DD})
19	CSL2	I	Test. Normally fixed Low. (V_{SS})
20	$V_{SS}2$	—	Digital GND. (V_{SS})
21	AVS3	—	L-ch DA converter GND. (AV_{SS})
22	AVD3	—	L-ch DA converter power supply. (AV_{DD})
23	LOUT	O	L-ch DA converter output.
24	AVD1	—	L-ch AD converter power supply. (AV_{DD})
25	AVS1	—	L-ch AD converter GND. (AV_{SS})
26	LO1	O	L-ch AD converter LPF operational amplifier inverted output.
27	LIN	I	L-ch AD converter analog input.
28	AVD5	—	C-ch DA converter power supply. (AV_{DD})
29	AVS5	—	C-ch DA converter GND. (AV_{SS})
30	XCOUT	O	C-ch DA converter output.
31	AVDX	—	Analog power supply for master clock. (AV_{DD})
32	XTLO	O	Crystal oscillator circuit output.
33	XTLI	I	Crystal oscillator circuit input.
34	AVSX	—	Analog GND for master clock. (AV_{SS})
35	XSOUT	O	S-ch DA converter output.
36	AVS6	—	S-ch DA converter GND. (AV_{SS})
37	AVD6	—	S-ch DA converter power supply. (AV_{DD})

(OPEN): Open, (V_{DD}): +5V digital power supply, (AV_{DD}): +5V analog power supply,
(V_{SS}): Digital GND, (AV_{SS}): Analog GND

Notations in parentheses indicate the fixed pin connection status.

Pin No.	Symbol	I/O	Description
38	RIN	I	R-ch AD converter analog input.
39	LO2	O	R-ch AD converter LPF operational amplifier inverted output.
40	AVS2	—	R-ch AD converter GND. (AVSS)
41	AVD2	—	R-ch AD converter power supply. (AVDD)
42	ROUT	O	R-ch DA converter output.
43	AVD4	—	R-ch DA converter power supply. (AVDD)
44	AVS4	—	R-ch DA converter GND. (AVSS)
45	VSS3	—	Digital GND. (VSS)
46	SCK	I	Shift clock input for microcomputer interface.
47	REDY	O	Transfer enabling signal output for microcomputer interface. Transfer prohibited when Low.
48	T.P	O	Test monitor. Normally outputs Hi-Z. (OPEN)
49	XLAT	I	Latch input for microcomputer interface.
50	RVDT	I	Data input for microcomputer interface.
51	XS24	I	Serial data 24-/32-bit slot selection. 24-bit slot when Low. (valid for slave mode)
52	VDD1	—	Digital power supply. (VDD)
53	VSS4	—	Digital GND. (VSS)
54	T.P	O	Test monitor. Normally outputs Low. (OPEN)
55	SI	I	1-sampling 2-channel serial data input.
56	T.P	I	Test input. Normally inputs Low. (VSS)
57	BCK	I/O	Serial bit transfer clock for serial I/O data SI and SO.
58	LRCK	I/O	Sampling frequency clock for serial I/O data SI and SO.
59	VSS5	—	Digital GND. (VSS)
60	XMST	I	BCK, LRCK master/slave mode switching input. Master mode when Low.
61 to 63	T.P	O	Test monitor. Normally outputs Low. (OPEN)
64	VSS6	—	Digital GND. (VSS)
65 to 72	T.P	O	Test monitor. Normally outputs Low. (OPEN)
73	VDD2	—	Digital power supply. (VDD)
74	VSS7	—	Digital GND. (VSS)
75 to 80	T.P	O	Test monitor. Normally outputs Low. (OPEN)

(OPEN): Open, (VDD): +5V digital power supply, (AVDD): +5V analog power supply,
(VSS): Digital GND, (AVSS): Analog GND

* There are three digital and seven analog power supplies, but the power-on sequence is not specified.

DC Characteristics

(AVD1 to 6 = AVDX = V_{DD}0 to 2 = 5V ± 5%, AVS1 to 6 = AVSX = V_{SS}0 to 7 = 0V, Ta = –20 to +70°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH}	CMOS input	0.7V_{DD}			V	*1, *2, *7
	Low level	V_{IL}				0.3V_{DD}	V	*1, *2, *7
Input voltage (2)	High level	V_{IH}	Schmitt input	0.8V_{DD}			V	*5
	Low level	V_{IL}				0.2V_{DD}	V	*5
Input voltage (3)	High level	V_{IH}	TTL input	2.2			V	*3, *6
	Low level	V_{IL}				0.8	V	*3, *6
Input voltage (4)		V_{IN}	Analog input	V_{SS}		V_{DD}	V	*4
Output voltage (1)	High level	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.8			V	*8, *9
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	*8, *9, *10
Output voltage (2)	High level	V_{OH}	I_{OH} = –12.0mA	V_{DD}/2			V	*11
	Low level	V_{OL}	I_{OL} = 12.0mA			V_{DD}/2	V	*11
Input leak current (1)		I_I	V_{IH} = V_{DD}, V_{SS}	–10		10	µA	*1, *5, *7
Input leak current (2)		I_I	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*2, *3, *6
Output leak current		I_{OZ}	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*9, *10
Feedback resistance		R_{FB}		250k	1M	2.5M	Ω	Resistance between *7 and *11

*1 CSL2, CSL1, TST0 to TST4, XMST

*2 XLAT, RVDT, XS24, SCK

*3 SI

*4 LIN, RIN

*5 XRST

*6 During input to bidirectional pins BCK, LRCK

*7 XTLI

*8 During output from bidirectional pins BCK, LRCK

*9 BFOT

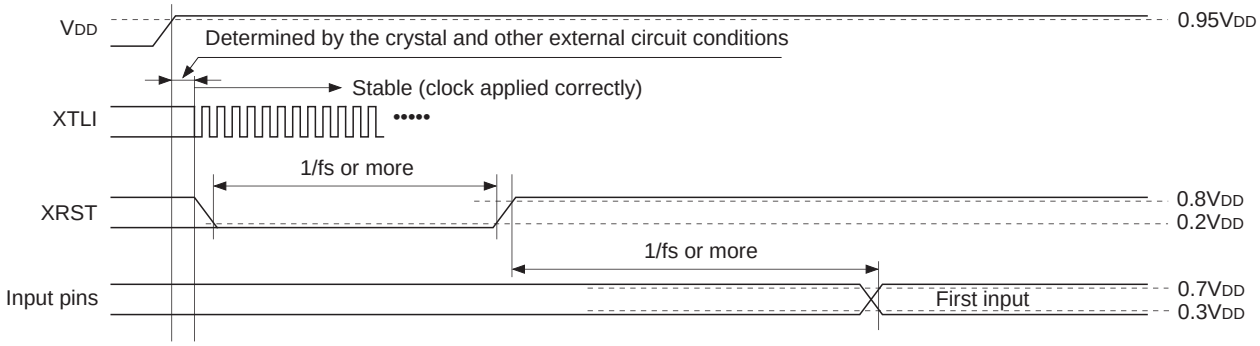
*10 REDY

*11 XTLO

AC Characteristics

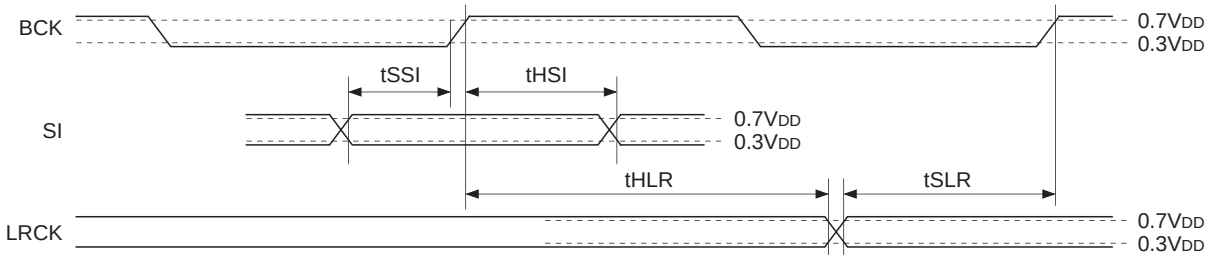
(AVD1 to 6 = AVDX = V_{DD}0 to 2 = 5V ± 5%, AVS1 to 6 = AVDX = V_{SS}0 to 7 = 0V, Ta = –20 to +70°C)

Input Timing from Power-on to Input Pin

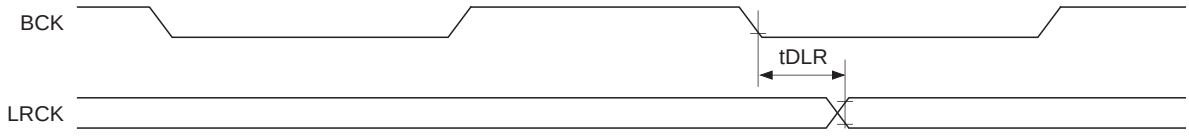


Serial Audio Interface Timing

[Slave mode]



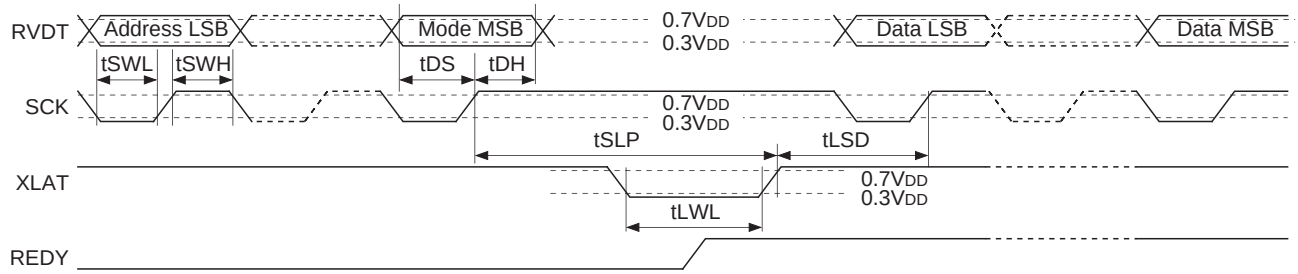
[Master mode]



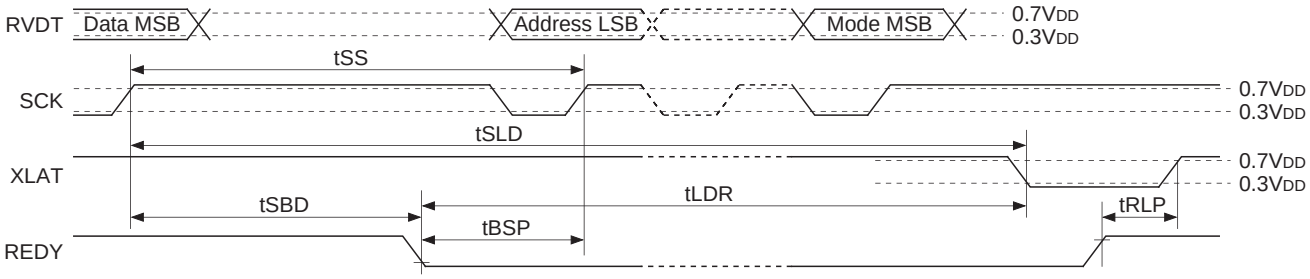
Item	Symbol	Conditions	Min.	Max.	Unit
SI setup time	t_{SSI}	Slave mode	20		ns
SI hold time	t_{HSI}	Slave mode	40		ns
LRCK setup time	t_{SLR}	Slave mode	20		ns
LRCK hold time	t_{HLR}	Slave mode	40		ns
LRCK delay time	t_{DLR}	Master mode, C_L = 120pF		50	ns

Microcomputer Interface Timing

Transfer timing for address section, transfer mode section and data section LSB



Transfer timing from data section MSB to address section and transfer mode section



Item	Symbol	Min.	Max.	Unit
RVDT data setup time relative to SCK rise	tDS	20		ns
RVDT data hold time from SCK rise	tDH	1t + 20		ns
SCK Low level width	tSWL	1t + 20		ns
SCK High level width	tSWH	1t + 20		ns
XLAT Low level width	tLWL	1t + 20		ns
XLAT High level width	tLWH	1t + 20		ns
SCK rise preceding time relative to XLAT rise	tSLP	20		ns
SCK rise wait time relative to XLAT rise	tLSD	3t + 20		ns
Delay time to REDY fall relative to SCK rise	tSBD		4t + 50	ns
REDY fall preceding time relative to SCK rise	tBSP	20		ns
REDY rise preceding time relative to XLAT rise	tRLP	20		ns
REDY rise preceding time relative to SCK fall	tRSDP	20		ns
XLAT fall wait time relative to SCK rise	tSLD	3t + 20		ns
XLAT fall delay time relative to REDY fall	tLDR	20		ns
SCK rise wait time for next transfer	tSS	2t + 40		ns

Notes) 1. t is the cycle of 2/3 the clock frequency applied to the XTLI pin. (512fs)

2. The REDY pin is the value for C_L = 60pF.

Analog Characteristics

(AVD0 to 6 = V_{DD}0 to 2 = AVDX = 5.0V, AVS0 to 6 = V_{SS}0 to 7 = AVSX = 0.0V, fs = 44.1kHz, Ta = 25°C)

When Pro Logic mode is on, the input signal level while measuring the center (C) and surround (S) channels should be –3dB smaller than the input level while measuring the left (L) and right (R) channels. Note that the C channel is input in-phase to the L channel, and the S channel is input at reversed phase to the R channel.
The input level is the same for all measurement items when Pro Logic mode is off.

1. ADC + DAC Connection Total Characteristics

In addition to the ADC and DAC, the total characteristics include the prefilter with built-in operational amplifier, built-in post filter, and trim volume. Use the analog I/O circuits in the Application Circuit for the measurement circuit.

1-1. When Pro Logic mode is on

Unless otherwise specified, the measurement conditions are as given below.
- V_{IN} (L, R) = 300mVrms, V_{IN} (C, S) = 212mVrms (= 0dB)
- f_{IN} = 1kHz

Item	Measurement conditions	Channels	Min.	Typ.	Max.	Unit
S/N ratio*1	CCIR/ARM filter	L, R	70	80		dB
		C, S	65	72		
	10Hz to 500kHz	L, R		60		
		C		56		
		S		64		
THD + N	10Hz to 20kHz V_{IN} = 16.5dB*2	L, R		0.04	1.00	%
		C, S		0.007	1.00	
	10Hz to 20kHz V_{IN} = 0dB*3	L, R		0.015		
		C, S		0.03		
	10Hz to 20kHz V_{IN} = –3.52dB*4	L, R		0.02		
		C, S		0.04		
	10Hz to 500kHz	L, R		0.12		
		C		0.18		
		S		0.04		
Head room	10Hz to 20kHz, THD + N = 1%			16.5		dB
Matrix rejection	*5	L, R	25	60		dB
		C, S	25	40		
Output level		(all)	250	280	310	Vrms
Level difference between channels		(all)		±0.2		dB
Current consumption	Analog system (including oscillator circuit)			36		mA
	Digital system			91		
Power supply rejection ratio*6	1mVrms, 100Hz sine wave	L, R		3.9		dB
		C, S*7		–13.2		

*1 When V_{IN} = 200mVrms (= –3.52dB), the S/N ratio is 3.52dB smaller than the values noted in the table above.
*2 V_{IN} (L, R) = 2.0Vrms, V_{IN} (C, S) = 1.414Vrms
*3 V_{IN} (L, R) = 300mVrms, V_{IN} (C, S) = 212mVrms
*4 V_{IN} (L, R) = 200mVrms, V_{IN} (C, S) = 141mVrms
*5 When the L and R channel gain deviation is 0.1dB or less for the ADC front-end prefilter output.
*6 Includes the amplification (L/Rch...5.27dB, C/Sch...13.72dB) of the external amplifier.
*7 The trim volume is set to 0dB.

1-2. When Pro Logic mode is off

Unless otherwise specified, the measurement conditions are as given below.

- V_{IN} (L, R, C, S) = 2.0Vrms (= 0dB)
- f_{IN} = 1kHz

Item	Measurement conditions	Channels	Min.	Typ.	Max.	Unit
S/N ratio	EIAJ (with "A" weighting filter)	L, R		97		dB
		C, S		90		
THD + N*11	EIAJ (0dB)	(all)		0.03	1.00	%
	EIAJ (–3dB)	L, R		0.004		
		C, S		0.01		
Dynamic range*12	EIAJ (–60dB)	L, R		93		dB
		C, S		83		
ADC maximum input level*13	(Full-scale output)	(all)		1.33		Vrms
Output level*14		(all)	1.7	1.85	2.0	Vrms

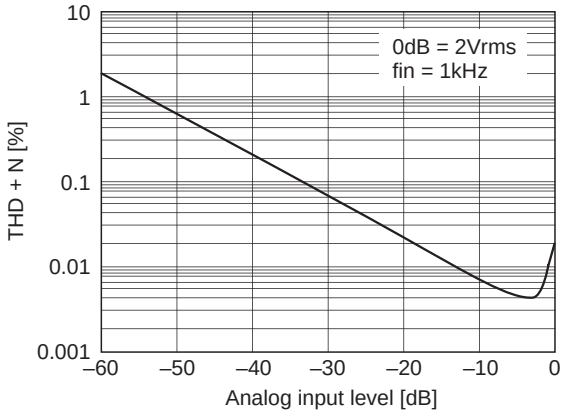
*11 See Graphs 1a and 1b.

*12 THD + N during –60 dB input

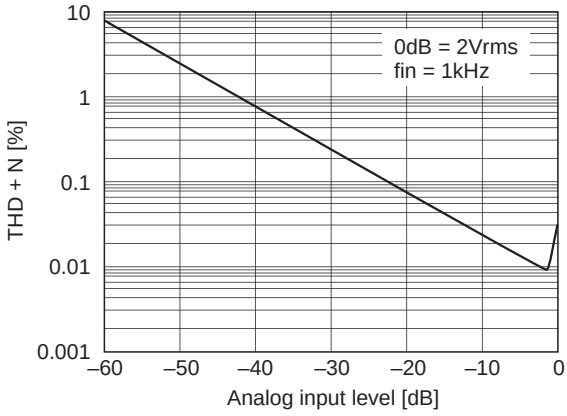
*13 The analog input level at which the ADC outputs full scale varies according to supply voltage AVDn. When supply voltage AVDn contains deviation, calculate the maximum input level from (Formula 1) below and adjust the level with the ADC front-end prefilter, etc., so that the waveform is not clipped at the minimum voltage.

$$\text{ADC maximum input level [Vrms]} = 1.33\ \text{[Vrms]} \times \frac{\text{Minimum supply voltage [V]}}{5.0\ \text{[V]}} \quad \text{(Formula 1)}$$

*14 Like the ADC, the DAC conversion gain also varies according to supply voltage AVDn. However, the DAC has the reverse characteristics of the ADC, so the total gain between the ADC and DAC is constant.



Graph 1a. L, R Channel Characteristics



Graph 1b. C, S Channel Characteristics

2. DAC Characteristics

In addition to the DAC, these characteristics include the built-in post filter and trim volume. Use the digital input and analog output circuits in the Application Circuit for the measurement circuit.

2-1. When Pro Logic mode is on

Unless otherwise specified, the measurement conditions are as given below.

- Digital data = –20dBFS
- f_{IN} = 3kHz

Item	Measurement conditions	Channels	Min.	Typ.	Max.	Unit
S/N ratio	CCIR/ARM filter Data = –20dBFS	L, R		77		dB
		C, S		68		
	10Hz to 500kHz Data = –20dBFS	L, R		60		
		C		52		
		S		65		
THD + N	10Hz to 20kHz Data = –20dBFS	L, R		0.05		%
		C		0.08		
		S		0.06		
	10Hz to 500kHz Data = –20dBFS	L, R		0.15		
		C		0.3		
		S		0.08		
Dolby level				–20		dBFS
Output level*31	Data = –20dBFS			200		mVrms
Matrix rejection	f_{IN} = 3kHz	L, R-in		62		dB
		C-in		87		
		S-in		79		
Level difference between channels		(all)		±0.2		dB

*31 The output level depends on supply voltage AVDn as shown in (Formula 2) below.

$$\text{Output level [mVrms]} = 285\ \text{[mVrms]} \times \frac{\text{Supply voltage AVDn [V]}}{5.0\ \text{[V]}} \quad \text{(Formula 2)}$$

2-2. When Pro Logic mode is off

Unless otherwise specified, the measurement conditions are as given below.

- Digital data = Full scale (0dBFS)
- f_{IN} = 1kHz

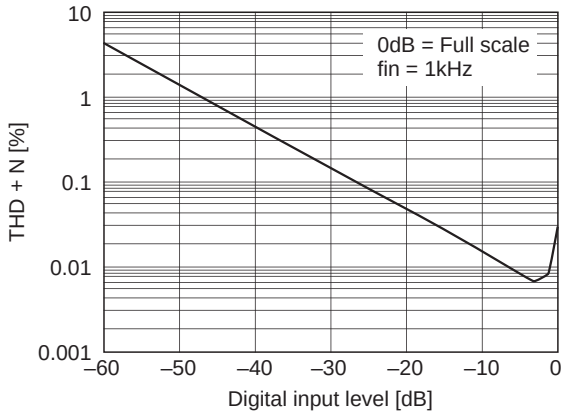
Item	Measurement conditions	Channels	Min.	Typ.	Max.	Unit
S/N ratio	EIAJ (with "A" weighting filter)	L, R		100		dB
		C, S		91		
THD + N*41	EIAJ (0dB)	L, R		0.03		%
		C, S		0.007		
	EIAJ (–3dB)	L, R		0.007		
		C, S		0.01		
Dynamic range*42	EIAJ (–60dB)	L, R		87		dB
		C, S		83		
Output level*43		(all)		2.0		Vrms

*41 See Graphs 2a and 2b.

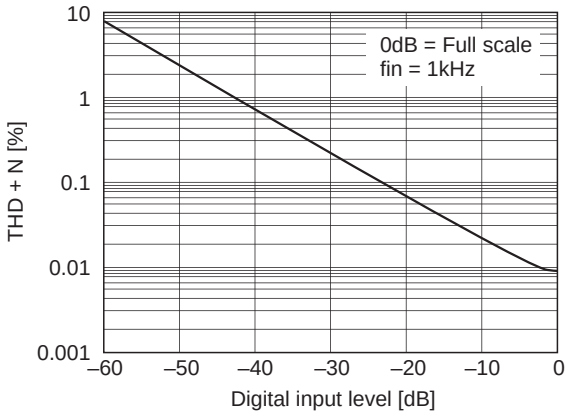
*42 THD + N during –60dB input

*43 The output level depends on supply voltage AVDn as shown in (Formula 3) below.

$$\text{Output level [Vrms]} = 1.9\ \text{[Vrms]} \times \frac{\text{Supply voltage AVDn [V]}}{5.0\ \text{[V]}} \quad \text{(Formula 3)}$$



Graph 2a. L, R Channel Characteristics



Graph 2b. C, S Channel Characteristics

3. Bypass Mode Characteristics (L, R channels only)

These are the characteristics without passing through the DSP, and including the prefilter with built-in operational amplifier and the built-in post filter. Use the analog I/O circuits in the Application Circuit for the measurement circuit. Unless otherwise specified, the measurement conditions are as given below.

- f_{IN} = 1kHz
- V_{IN} (L, R) = 2.0Vrms (= 0dB)

Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	CCIR/ARM filter		97		dB
	10Hz to 20kHz, "A" weighting filter		100		
	10Hz to 500kHz		80		
THD + N	10Hz to 500kHz		0.008		%
	10Hz to 20kHz		0.005		
Dynamic range*51	10Hz to 20kHz, V_{IN} = –60dB		95		dB
Maximum input level	THD + N = 0.05%		2.5		Vrms
Output level			2.0		Vrms
Level difference between channels			±0.2		dB
Channel separation			105		dB
Power supply rejection ratio*52	1mVrms, 100Hz sine wave		7.5		dB

*51 THD + N during –60dB input

*52 Includes the amplification (5.27dB) of the external amplifier.

4. Filter Characteristics

Item	Measurement conditions	Min.	Typ.	Max.	Unit
Prefilter	Feedback resistance value	10			kΩ
	Maximum amplification rate (100kHz or less)			20	dB
Post filter	Load resistance value	10			kΩ
	Cut-off frequency (= fc)		104		kHz

5. Trim Volume Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Maximum gain	TRIMmax		1.5		dB
Minimum gain	TRIMmin		–29.5		dB
Variable step	TRIMstep		1.0		dB

Description of Functions

1. Master/Slave Modes

[Relevant pins] XMST, LRCK, BCK

When using the CXD2719Q alone without digital input, set the CXD2719Q to master mode.
When using digital input, the CXD2719Q may be set to either master mode or slave mode.
The clock applied to LRCK and BCK in slave mode must be synchronized to either the crystal oscillator clock of the XTLI and XTLO pins or the external clock input from the XTLI pin.

XMST	Mode	LRCK, BCK I/O
H	Slave mode	Input
L	Master mode	Output

Table 1-1. LRCK, BCK Mode Setting

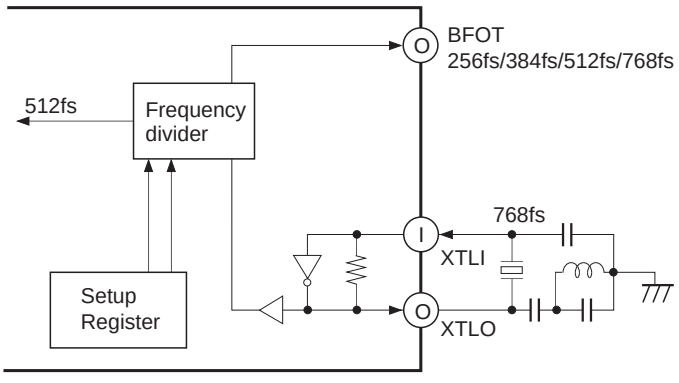
2. Master Clock System

[Relevant pins] XTLI, XTLO, BFOT

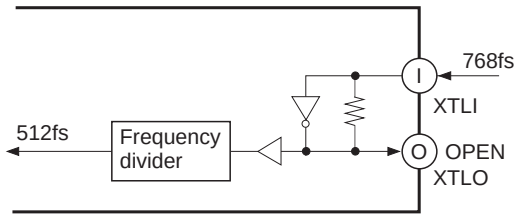
768fs (fs = 32 to 44.1kHz) is assumed for the master clock system, and the connection is as shown below. BFOT outputs the clock obtained by frequency dividing the master clock. The frequency division ratio can be changed by the setup register (SQC04, SQC05). (See "6. Setup Register".)

SQC05	SQC04	BFOT
0	0	384fs
0	1	256fs
1	0	512fs
1	1	768fs

(1) Master



(2) Slave



Note) Oscillation circuits may differ according to peripheral circuit and substrate. Consult with crystal oscillator manufacturers about the selecting oscillation circuits.

Fig. 2-1.

3. Reset Circuit

[Relevant pins] XRST, XTLI, XTLO

This LSI must be reset after the power is turned on.

Reset is done by setting the XRST pin Low for 1/fs or more after the supply voltage satisfies the recommended operating condition, and the crystal oscillator clock of the XTLI and XTLO pins or the external clock input from the XTLI pin is correctly applied. (See "AC Characteristics".)

4. Serial Audio Interface (SIF)

[Relevant pins] SI, BCK, LRCK, XS24, XMST

Serial data is used for the external communication of the digital audio data. The CXD2719Q has only one input system, and 2 channels of data are input each sampling cycle. Either the 32-bit clock mode or the 24-bit clock mode can be selected. In master mode, the mode is fixed to the 32-bit clock mode.

(1) Pin Configuration (The pins shown in the table below are assigned to the SIF.)

Symbol	I/O	Function
SI	I	Serial input; taken with synchronized to BCK.
BCK	I/O	BCK I/O; either 32-bit clock mode (64fs) or 24-bit clock mode (48fs). BCK output supports 32-bit clock mode only.
LRCK	I/O	LRCK I/O (1fs).
XS24	I	SIO slot number (24/32) selection input. Low: 24-bit slot; High: 32-bit slot. Valid only in slave mode. Set High in master mode. Do not switch between High and Low during DSP operation.
XMST	I	BCK, LRCK master mode/slave mode switching input. Low: master mode; High: slave mode.

Table 4-1. Pin Configuration

(2) Operation Modes

The LRCK/BCK mode can be selected by the setup register settings as follows. (See "6. Setup Register".)

LRCK/BCK Mode Setting

Setup register	Function	Contents
SQC15	LRCK format	"0": normal, "1": IIS
SQC14	LRCK polarity selection	"0": Lch "H", "1": Lch "L"
SQC13	BCK polarity selection relative to LRCK edge Valid only in slave mode. Fix to "0" in master mode.	"0": edge ↓, "1" : edge ↑

Table 4-2. LRCK/BCK Mode Setting

(3) SIF Format

The serial audio interface has only one input system, and except for the slot number, the following formats can be set by setting the setup register. The serial audio interface can also support IIS format to enable connection to Philips and other company's devices.

The timing charts for each data format are given on the following page.

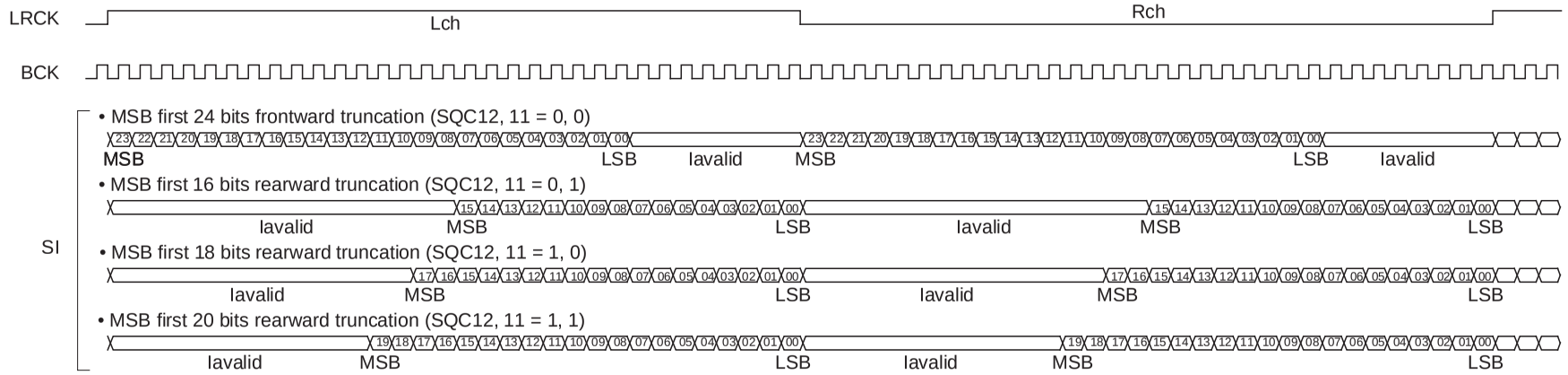
SQC12	SQC11	Data arrangement/Frontward or rearward truncation/Data word length
0	0	MSB first/Frontward truncation/24 bits
0	1	MSB first/Rearward truncation/16 bits
1	0	MSB first/Rearward truncation/18 bits
1	1	MSB first/Rearward truncation/20 bits

* All formats support either the 24- or 32-bit slot in slave mode.

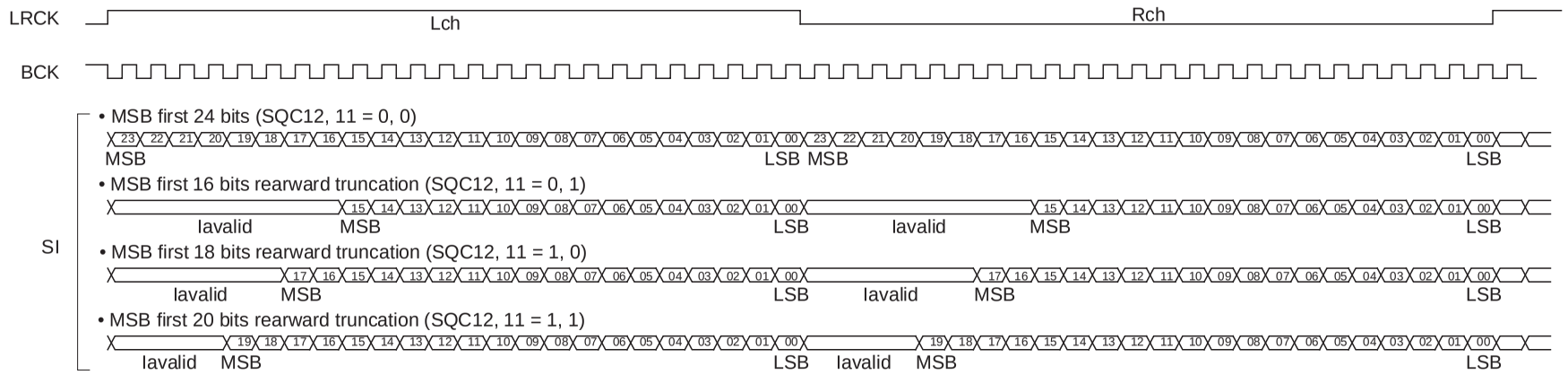
Table 4-3. Setup Register Settings

Digital Audio Data Input Timing (with polarities: SQC15 = 0, SQC14 = 0, SQC13 = 0)

32-bit slot



24-bit slot



5. Microcomputer Interface

[Relevant pins] RVDT, SCK, XLAT, REDY

The CXD2719Q performs the serial audio interface format setting and the coefficient settings such as volume and filter by serial data from the microcomputer.

(1) Pin Configuration

The four external pins indicated in the table below are assigned to the microcomputer interface.

Symbol	I/O	Function
RVDT	I	Serial data input from microcomputer.
SCK	I	Shift clock for serial data. Input data from RVDT is taken according to the SCK rise.
XLAT	I	Interprets the 8 bits of RVDT before this signal rises as transfer mode data, and the bits before that as address data.
REDY	O	Transfer prohibited while at Low level. Transfer enabled at High. This pin is an open drain, and must be pulled up externally.

Table 5-1. Microcomputer Interface External Pins

(2) Description of Communication Formats

The internal data transfer timing from the microcomputer interface to the coefficient RAM and setup register is called the SV cycle, and is generated once per 1 LRCK.

The SV cycle is generated immediately preceding the signal processing program, so it has absolutely no effect on signal processing, and there is no risk of the sound being cut.

Address section + Mode section + Data section

act as one package of data to transfer data from the microcomputer to the CXD2719Q.

[Write] * For coefficient RAM

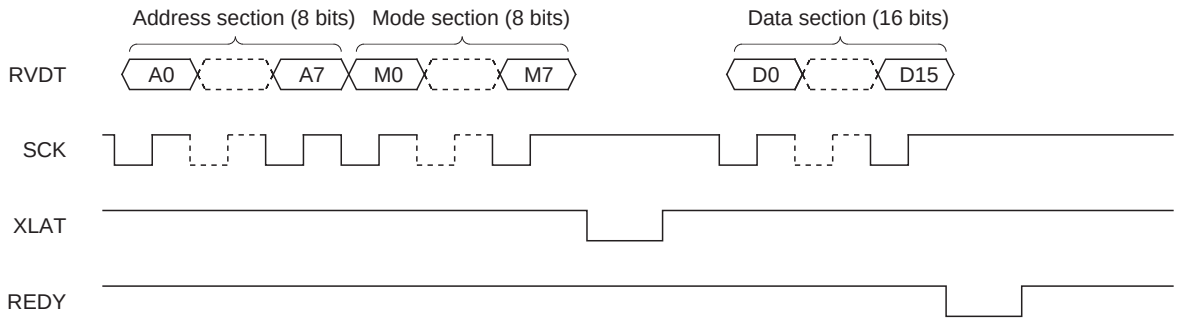


Fig. 5-1. Example of Communication

(3) Data Structure

The data structure is classified into three types, as shown in the table below. All data communication is done with LSB first.

Symbol	Bit length	Contents	Remarks
A0 to A7	8	Address section	
M0 to M7	8	Transfer mode section	
D0 to D15/SQ00 to SQ15	16	Data section	Coefficient RAM and setup register are both 16 bits

Table 5-2. Data Structure

(3)-1. Transfer Mode Section

The transfer mode section is 8 bits and has the following functions.

Bit	Symbol	Function	
M7		Reserve	Normally fixed to "0"
M6	SU1	Setup Reg. type	SU1 SU0 0 0 Field A 0 1 Field B 1 0 Field C 1 1 Field D
M5	SU0		
M4	VS1	Data type	VS1 VS0 0 0 Setup register 1 0 Coefficient RAM
M3	VS0		
M2		Reserve	Normally fixed to "0"
M1			
M0			

Table 5-3. Transfer Mode Section

(3)-2. Address Section

The coefficient RAM has a 256-word structure, so the address section is 8 bits. The setup register has a 4-word structure and the field (address) is specified by the mode section, so the address section data may be optional.

(3)-3. Data Section

The coefficient RAM and setup register both have a 16-bit structure, so 16 SCK are required.

(4) Details of Communication Methods

The definitions of signal timing required for control from the microcomputer are given below.

(4)-1. Initializing the Microcomputer Interface

The microcomputer interface must be initialized after resetting the IC.

After resetting the IC (t1 ≥ 1/fs), input 16 SCK rising edges. After that, REDY goes Low within 4t + 50ns (t2), and initialization is completed when REDY goes High again. Set RVDT Low while inputting SCK.
Note that the REDY Low time (t3) is a maximum of 1/fs. See the following page for the SCK restrictions. The same restrictions apply as during data transfer.

When REDY goes Low due to initialization:

- The SCK for the first transfer can rise.
- The XLAT for the first transfer can fall.

However, the XLAT for the first transfer must rise after REDY goes High.

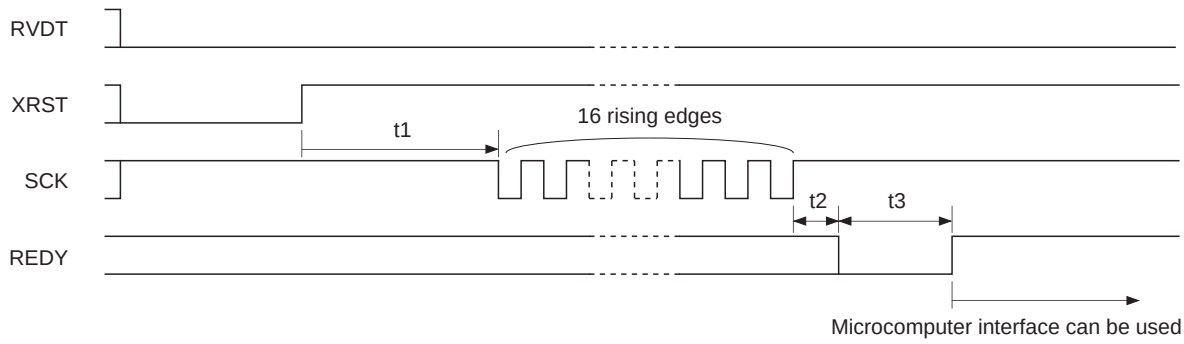


Fig. 5-2. Initialize Specifications

(4)-2. Signal Timing

First, address section data and mode section data are sent from the microcomputer, synchronized to SCK, to the RVDT pin.

The address section data is 8 bits for both the coefficient RAM and setup register, and the setup register has a length of one word, so optional data can be transferred. Address section data is sent with LSB first.

Mode section data is fixed at 8 bits regardless of the transfer contents.

The phase relationship between SCK and RV data (data applied to the RVDT pin) has the following restrictions:

- RV data must be established before SCK rises (tDS ≥ 20ns).
- RV data must be held for 1t + 20ns or more after SCK rises (tDH).

SCK itself has the following restrictions:

- SCK Low level must be 1t + 20ns or more (tSWL).
- SCK High level must be 1t + 20ns or more (tSWH).

After the SCK rise which corresponds to the mode section final data, XLAT rises (tSLP ≥ 20ns).

The XLAT Low level width must be maintained at 1t + 20ns or more (tLWL). The fall timing is restricted in that even if REDY falls due to SCK during the preceding transfer, 3t + 20ns or more (tSLD) is required from the SCK rise which corresponds to the data section final data.

Further, if preceding transfers have been performed and REDY = Low, XLAT must rise after REDY = High.

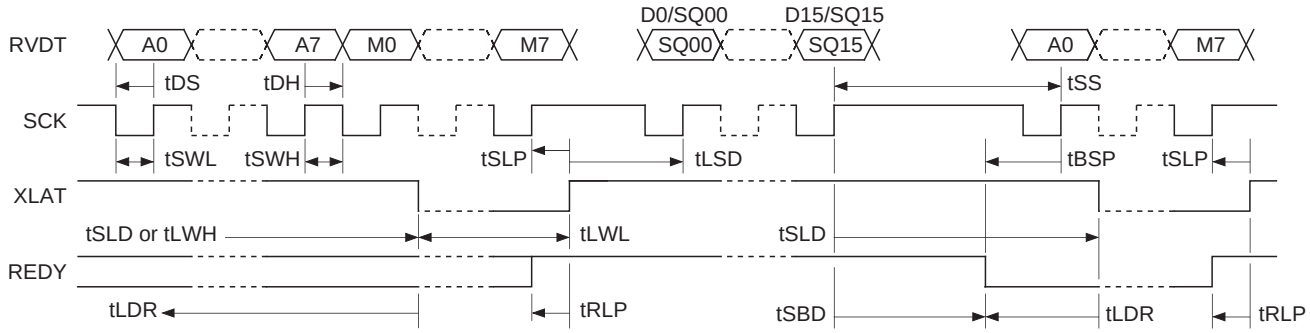


Fig. 5-3. Write Timing

* t is the cycle of 2/3 the clock frequency applied to the XTLI pin. (512fs)

Data section write begins after XLAT rises, and here also transfer must be performed with LSB first, with tDS and tDH restrictions. In addition, after XLAT rises at the starting point for sending the data section, wait for 3t + 20ns or more for the first SCK rise (tLSD).

When 16 bits of this write is repeated, REDY goes Low within 4t + 50ns, and the microcomputer is informed of waiting status for the SV cycle, which is the dedicated data rewrite cycle, by the microcomputer interface (tSBD).
When REDY goes High again, the corresponding data is written.

The next communication can be restarted by using the REDY signal as follows.

- When REDY = Low, the SCK for the next transfer can rise (tBSP ≥ 20ns).
- In the same way, when REDY = Low, the XLAT for the next transfer can fall (tLDR ≥ 20ns).

REDY will fall due to this communication, but it is prohibited for XLAT to rise for the next transfer before REDY rises. Make sure that the next XLAT rises after REDY rises (tRLP ≥ 20ns).

In order to restart the next transfer without using the REDY signal, the following conditions must be observed:

- There should be 2t + 40ns or more left between the SCK rise for the final data section and the SCK rise for the next transfer (tSS).
- In the same way, the XLAT for the next transfer can fall after waiting for 3t + 20ns or more after the final data section SCK rise (tSLD).

The tSS and tSLD here are shorter times than tSBD ≤ 4t + 50ns, so these are rather loose restrictions. However, even in this case the XLAT rise for the next transfer must come after REDY rises (tRLP ≥ 20ns).

Further, the restriction for the XLAT fall at the starting point of this transfer from tSLD can be:

tSLD ≥ 3t + 20ns

6. Setup Register

When the setup register is selected in microcomputer interface transfer mode, the following settings are possible for hardware such as the serial audio interface and DAC, and for software such as the Dolby Pro Logic Surround decoder.

The setup register has a total of four fields, and 16 bits of setup information can be stored per field. However, when this LSI is reset, the setup register contents are also reset to the settings shown in the "When reset" column in Tables 6-1 to 6-4 below.

(1) Field A

Data section bit	Control contents	When reset
SQA15	DSP bypass mode 0: OFF 1: ON	OFF
SQA14	Noise sequencer 0: OFF 1: ON	OFF
SQA13	Reserve bit Be sure to set both bits Low when changing the setup register Field A se	all "L"
SQA12	Compensation filter 0: OFF 1: ON	OFF
SQA11, SQA10	Decimation ratio setting (SFC mode only) Be sure to also set SQC07 and SQC06. SQA11 SQA10 0 0 : 1/1 (No decimation) 0 1 : 1/2 decimation 1 0 : 1/3 decimation	1/1 (No decimation)
SQA09, SQA08	Dolby 3 Stereo SQA09 SQA08 0 0 : OFF 0 1 : ON	OFF
SQA07, SQA06	Reserve bit Be sure to set both bits Low when changing the setup register Field A settings.	all "L"
SQA05, SQA04	SFC mode SQA05 SQA04 0 0 : OFF 0 1 : ON	OFF
SQA03 to SQA00	Reserve bit Be sure to set both bits Low when changing the setup register Field A settings.	all "L"

Table 6-1. Setup Register Field A

* Bit names are indicated by the field name and the bit number. The bit names for Field A are SQA00 to SQA15, and the first three letters of the bit names for Fields B, C and D are SQB, SQC and SQD, respectively.

(2) Field B

Data section bit	Control contents		When reset
SQB15 to SQB11	Center channel trim volume (5 bits, analog)	00000: 0dB 00001: –1dB 00010: –2dB ↓ 11101: –29dB 11110: –30dB 11111: –31dB	0dB
SQB10 to SQB06	Center channel trim volume (5 bits, analog)	00000: 0dB 00001: –1dB 00010: –2dB ↓ 11101: –29dB 11110: –30dB 11111: –31dB	0dB
SQB05 to SQB00	Reserve bit	Be sure to set all of these bits Low when changing the setup register Field B settings.	all "L"

Table 6-2. Setup Register Field B

(3) Field C

Data section bit	Control contents	When reset
SQC15	LRCK format 0: normal 1: IIS	normal
SQC14	LRCK polarity selection 0: Lch "H" 1: Lch "L"	Lch "H"
SQC13	BCK polarity selection relative to LRCK edge 0: Falling edge 1: Rising edge	Falling edge
SQC12, SQC11	Serial audio interface setting SQC12 SQC11 0 0 : MSB first/Frontward truncation/24 bits 0 1 : MSB first/Rearward truncation/16 bits 1 0 : MSB first/Rearward truncation/18 bits 1 1 : MSB first/Rearward truncation/20 bits	MSB first/Frontward truncation/24 bits
SQC10	DAC forced mute 0: ON 1: OFF	ON
SQC09, SQC08	Reserve bit Be sure to set both bits Low when changing the setup register Field C settings.	all "L"
SQC07, SQC06	Decimation ratio setting (SFC mode only) Be sure to also set SQA11 and SQA10. SQC07 SQC06 0 0 : 1/1 (No decimation) 0 1 : 1/2 decimation 1 * : 1/3 decimation	1/1 (No decimation)
SQC05, SQC04	BFOT output clock frequency division ratio setting SQC05 SQC04 0 0 : 384Fs 0 1 : 256Fs 1 0 : 512Fs 1 1 : 768Fs	384Fs
SQC03 to SQC00	Reserve bit Be sure to set all of these bits Low when changing the setup register Field C settings.	all "L"

Table 6-3. Setup Register Field C

Note) BCK polarity selection (SQC13) is valid only in slave mode. Fix to "0" in master mode.

(4) Field D

Data section bit	Control contents	When reset
SQD15 to SQD03	Reserve bit Be sure to set all of these bits Low when changing the setup register Field D settings.	all "L"
SQD02 to SQD00	Be sure to set all of these bits Low	all "L"

Table 6-4. Setup Register Field D

7. Coefficient RAM

When the coefficient RAM is selected in microcomputer interface transfer mode, the various application functions can be turned on and off, and the coefficient parameters such as each section's volume and delay time can be set.
Coefficient RAM addresses other than those given in these specifications are "don't care". However, the RAM is not cleared entirely when this LSI is reset, so there are no initial values as for the setup register. Be sure to set all of the necessary data; otherwise misoperation may result.

The coefficient RAM has the capacitance of 256 words x 16 bits and the data transferred differs for each mode. (See "8. Applications" for the detailed contents.)

8. Applications

The CXD2719Q is equipped with various applications such as Dolby Pro Logic Surround mode (Pro Logic mode), Dolby 3 Stereo mode, noise sequencer mode, SFC mode, and DSP bypass mode.
The methods of setting each mode and of changing the mode are described below.

Note) The filter and other parameter values for each application assume a sampling frequency (fs) of 44.1 [kHz]. Consult your Sony representative with regard to use at other fs.

8-1. Dolby Pro Logic Surround Mode (Pro Logic Mode)

Pro Logic mode is realized using the adaptive matrix, passive decoder including BNR, auto input balance, center channel mode control, simple SFC and other functions.

(1) Setting Pro Logic Mode

Pro Logic mode must be set by the following procedures in order to achieve stable adaptive matrix operation. Setting Pro Logic mode by procedures other than those given below may aggravate the decoder characteristics.

- Immediately after power-on reset
  - i) Transfer the following setup data.
    SQA = 0030H (Field A)
    SQD = 7ee7H (Field D)

Note) Field C is "All 0", so the DAC forced mute is applied.

  - ii) Transfer the Pro Logic mode coefficient data.
  - iii) Transfer the setup data set in Pro Logic mode.
- Changing to Pro Logic mode from a different mode (other than Virtual mode)
  - i) Apply the soft mute*1 in the current mode.
  - ii) Set the coefficients at the following addresses to "0000H".
    Addresses: 6eH to 7fH
  - iii) Transfer the following setup data.
    SQA = 0030H (Field A)
    SQD = 7ee7H (Field D)

Note) The DAC forced mute is not applied by Field C.

  - iv) Transfer the Pro Logic mode coefficients for the soft mute status.
  - v) Transfer the setup data set in Pro Logic mode.
  - vi) Cancel the Pro Logic mode soft mute.

*1 Soft mute: See "Appendix 1. Soft Mute".

(2) Setting Data

(2)-1. Setup Data

Table 8-1-1 lists the registers most closely related to Pro Logic mode.

Setup data not listed in Table 8-1-1 may be set as desired, with due consideration given to the contents of Fields A to D noted in "6. Setup Register".

Register name	Setting value	Remarks
SQA14	"0"	1: Noise sequencer mode
SQA09, 08	"00"	01: Dolby 3 Stereo mode
SQA05, 04	"00"	01: SFC mode
SQB15 to 11	Don't care	Center channel (C-ch) trim volume
SQB10 to 06	Don't care	Surround channel (S-ch) trim volume

Table 8-1-1. Pro Logic Mode Setup Register Settings

(2)-2. Coefficient Data

The coefficient data consists of "fixed values" shown in Table 8-1-2 and "setting values" shown in Table 8-1-3 which can be set by the user. All coefficient values must be sent to the coefficient RAM via the microcomputer interface.

- **Fixed values during Pro Logic mode initialization**

  The following fixed values must be set in the coefficient RAM to ensure proper internal operation.

Address	Fixed value	Address	Fixed value	Address	Fixed value	Address	Fixed value
27H	0000H	90H	7f18H	baH	43b9H	e6H	0000H
6dH	051eH	91H	0400H	bbH	0400H	e7H	0000H
6eH	ff86H	92H	001eH	bcH	401eH	e8H	0000H
6fH	02a0H	93H	7fc5H	bdH	ec00H	e9H	0000H
70H	f6c0H	94H	0002H	beH	8000H	eaH	0000H
71H	2715H	95H	7ffdH	bfH	a000H	ebH	0000H
72H	4000H	96H	8000H	c0H	0024H	ecH	0000H
73H	5149H	97H	dd1eH	c1H	ff92H	edH	0000H
74H	e571H	98H	da82H	c2H	010aH	eeH	0000H
75H	0f4eH	99H	109cH	c3H	fce2H	efH	0000H
76H	f5b8H	9aH	2641H	c4H	097bH	f0H	7fffH
77H	075cH	9bH	3441H	c5H	e38dH	f9H	8000H
78H	fa97H	9cH	dd1eH	c6H	1555H	feH	b800H
79H	0402H	9dH	109cH	c7H	0400H	ffH	0001H
7aH	fd0bH	9eH	da82H	c8H	1400H		
7bH	0225H	9fH	2641H	c9H	2000H		
7cH	fe7cH	a0H	3441H	caH	c000H		
7dH	01d3H	a1H	0bbfH	cbH	ffe4H		
7eH	f312H	a2H	e755H	ccH	febcH		
7fH	4b85H	a3H	4000H	cdH	f520H		
80H	850fH	a4H	f619H	ceH	c144H		
81H	7d6bH	a5H	e57eH	cfH	a57eH		
82H	7d72H	a6H	36dcH	d0H	0757H		
83H	22b6H	a7H	5a82H	d1H	0012H		
84H	3a94H	a8H	10c9H	d2H	7f00H		
85H	0074H	a9H	2641H	d3H	7fffH		
86H	7f18H	aaH	7f18H	d5H	fc00H		
87H	a000H	abH	7e30H	d7H	68a9H		
88H	8000H	acH	4cbaH	d8H	5121H		
89H	febfH	adH	c216H	daH	7ff4H		
8aH	04f9H	aeH	0aa4H	dbH	7fe8H		
8bH	eb83H	b3H	27b4H	deH	8000H		
8cH	7b01H	b4H	7e14H	dfH	c400H		
8dH	cae0H	b6H	7ff9H	e3H	0000H		
8eH	0400H	b8H	0063H	e4H	0000H		
8fH	0074H	b9H	0000H	e5H	0000H		

Table 8-1-2. Pro Logic Mode Fixed Value Coefficients

• **Pro Logic mode user setting coefficients**

The relationships between the coefficient RAM and each function during Pro Logic mode operation are as follows.

Address	Symbol	Function	Setting value
00H	KLV	Simple SFC: L-ch dry → L-ch mix volume	See Table 8-1-13.
01H	KRV	Simple SFC: R-ch dry → R-ch mix volume	See Table 8-1-13.
02H	KCV	Simple SFC: C-ch → C-ch volume	See Table 8-1-13.
03H	KSV	Simple SFC: S + L/R (HPF1) → S-ch mix volume	See Table 8-1-13.
04H	KLm1	Simple SFC: L-ch → LPF1 mix volume	See Table 8-1-13.
05H	KRm1	Simple SFC: R-ch → LPF1 mix volume	See Table 8-1-13.
06H	a0	Simple SFC: LPF1 coefficient	See Table 8-1-16.
07H	a1	Simple SFC: LPF1 coefficient	See Table 8-1-16.
08H	b	Simple SFC: LPF1 coefficient	See Table 8-1-16.
09H	KLm2	Simple SFC: L-ch → HPF1 mix volume	See Table 8-1-13.
0aH	KRm2	Simple SFC: R-ch → HPF1 mix volume	See Table 8-1-13.
0bH	a0	Simple SFC: HPF1 coefficient	See Table 8-1-16.
0cH	a1	Simple SFC: HPF1 coefficient	See Table 8-1-16.
0dH	b	Simple SFC: HPF1 coefficient	See Table 8-1-16.
0eH	KLd	Simple SFC: L-ch → Delay RAM mix volume	See Table 8-1-13.
0fH	KRd	Simple SFC: R-ch → Delay RAM mix volume	See Table 8-1-13.
10H	KCd	Simple SFC: C-ch → Delay RAM mix volume	See Table 8-1-13.
11H	KSd	Simple SFC: S-ch → Delay RAM mix volume	See Table 8-1-13.
12H	Kfb	Simple SFC: Delay RAM feedback volume	See Table 8-1-13.
13H	a0	Simple SFC: HPF2 coefficient	See Table 8-1-16.
14H	a1	Simple SFC: HPF2 coefficient	See Table 8-1-16.
15H	b	Simple SFC: HPF2 coefficient	See Table 8-1-16.
16H	a0	Simple SFC: LPF2 coefficient	See Table 8-1-16.
17H	a1	Simple SFC: LPF2 coefficient	See Table 8-1-16.
18H	b	Simple SFC: LPF2 coefficient	See Table 8-1-16.
19H	KDin	Simple SFC: Delay RAM write address	See Table 8-1-15.
1aH	TP1	Simple SFC: Delay RAM read Tap1 address	See Table 8-1-15.
1bH	TP2	Simple SFC: Delay RAM read Tap2 address	See Table 8-1-15.
1cH	TP3	Simple SFC: Delay RAM read Tap3 address	See Table 8-1-15.
1dH	TP4	Simple SFC: Delay RAM read Tap4 address	See Table 8-1-15.
1eH	TP5	Simple SFC: Delay RAM read Tap5 address	See Table 8-1-15.
1fH	TP6	Simple SFC: Delay RAM read Tap6 address	See Table 8-1-15.
20H	KDout	Simple SFC: Delay RAM feedback Tap address	See Table 8-1-15.
21H	KDV1	Simple SFC: Delay RAM → S-ch mix volume	See Table 8-1-13.
22H	KDV2	Simple SFC: Delay RAM → R-ch mix volume	See Table 8-1-13.
23H	KDV3	Simple SFC: Delay RAM → L-ch mix volume	See Table 8-1-13.
24H	KLRm1	Simple SFC: LPF1 → L-ch mix volume	See Table 8-1-13.

Table 8-1-3 (1). Pro Logic Mode Setting Value Coefficients

Address	Symbol	Function	Setting value
25H	KLRm2	Simple SFC: LPF1 → R-ch mix volume	See Table 8-1-13.
26H	KLRm3	Simple SFC: HPF1 → S-ch mix volume	See Table 8-1-13.
28H	KTP1	Simple SFC: Tap1 volume	See Table 8-1-13.
29H	KTP2	Simple SFC: Tap2 volume	See Table 8-1-13.
2aH	KTP3	Simple SFC: Tap3 volume	See Table 8-1-13.
2bH	KTP4	Simple SFC: Tap4 volume	See Table 8-1-13.
2cH	KTP5	Simple SFC: Tap5 volume	See Table 8-1-13.
2dH	KTP6	Simple SFC: Tap6 volume	See Table 8-1-13.
afH	b2	7K LPF parameter	0000 = OFF, df66 = ON
b0H	b1	7K LPF parameter	0000 = OFF, 5723 = ON
b1H	a	7K LPF parameter	0000 = OFF, 125e = ON
b2H	–a	7K LPF parameter	8000 = OFF, eda2 = ON
b5H	aslw	Passive decoder M-BNR	See Table 8-1-12.
b7H	2D	Passive decoder M-BNR	See Table 8-1-12.
d4H	Kx	Auto input balance ON/OFF	0000 = OFF, 00ff = ON
d6H	KiA	Serial audio interface input volume	See Table 8-1-5.
d9H	Ke	De-emphasis ON/OFF	0000 = OFF, ac19 = ON
dcH	Kia	Analog input mix volume	See Table 8-1-4.
ddH	Kis	Digital input mix volume	See Table 8-1-5.
f2H	KL	Center mode control volume	See Tables 8-1-7, 8.
f3H	KR	Center mode control volume	See Tables 8-1-7, 8.
f4H	KH	Center mode control volume	See Tables 8-1-7, 8.
f5H	KP	Center mode control volume	See Tables 8-1-7, 8.
f6H	KCH	Center mode control volume	See Tables 8-1-7, 8.
f7H	KCP	Center mode control volume	See Tables 8-1-7, 8.
f8H	KS	Passive decoder volume	See Table 8-1-8.
faH	Kdlb	Passive decoder M-BNR ON/OFF	0000 = OFF, 2000 = ON
fbH	Dly	Passive decoder delay time adjustment	See Table 8-1-9.

Table 8-1-3 (2). Pro Logic Mode Setting Value Coefficients

(2)-3. Signal Flow for Dolby Pro Logic Mode

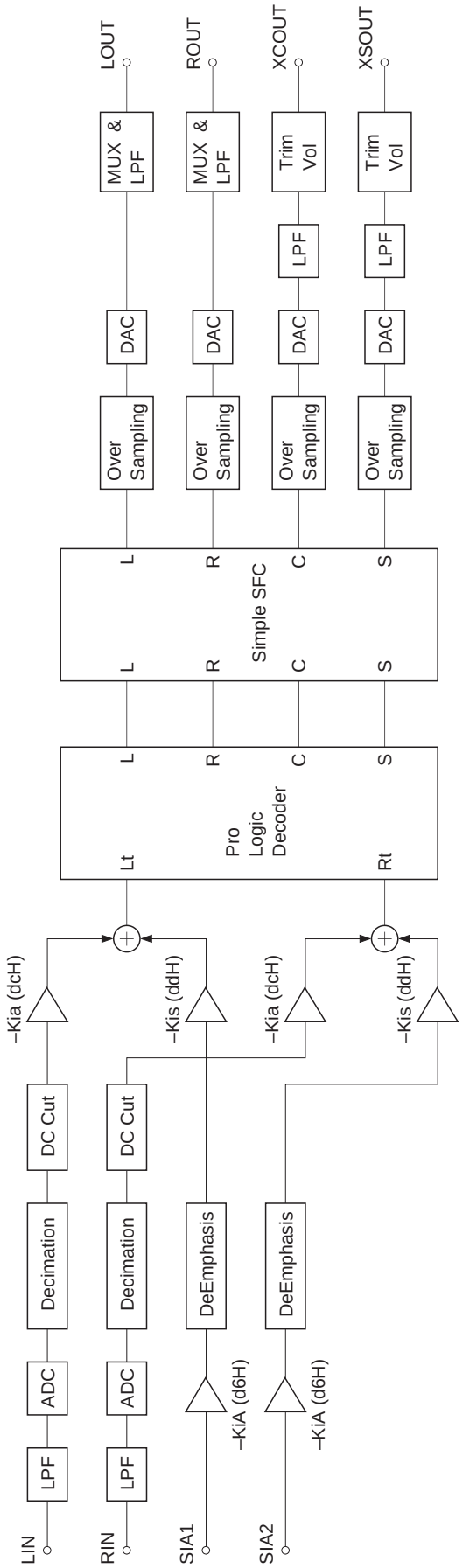


Fig. 8-1-1

(3) Volume Coefficient Settings

[Relevant data] Coefficients: KiA (d6H), Kia (dcH), Kis (ddH)

The I/O levels and volumes are 2's complement format with a decimal point between D15 and D14, and hexadecimal notation with D15 as MSB and D0 as LSB.

The coefficient and level relationships are as follows.

* D15 to D0 are negative values, but the DSP calculation is (–1) × (D15 to D0).

(3)-1. Kia (dcH): 0dB = c000H

The I/O levels for 8000H to ffffH are obtained by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})] \times (-2)$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
8000H	+6.02
a599H	+3.00
c000H	0.00
d2b2H	–3.00
e000H	–6.02
eff6H	–12.00
ffffH	–84.29
0000H	–∞

Table 8-1-4. Kia (dcH) Setting Value Examples

(3)-2. KiA (d6H), Kis (ddH): 0dB = 8000H

The I/O levels for 8000H to ffffH are obtained by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})] \times (-1)$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
8000H	0.00
a563H	–3.00
c000H	–6.02
e000H	–12.04
ffffH	–90.31
0000H	–∞

Table 8-1-5. KiA (d6H), Kis (ddH) Setting Value Examples

* Unless otherwise specified, subsequent setting examples (Pro Logic mode) in these specifications assume either:

  Kia = d2b2H, KiA = 0000H, Kis = 0000H

  or:

  Kia = 0000H, KiA = 8000H, Kis = a563H

(4) Auto Input Balance Control

[Relevant data] Coefficient: Kx (d4H)

The auto input balance function is turned on and off by coefficient Kx (d4H).

Coefficient Kx (d4H)	ON = 00ffH
	OFF = 0000H

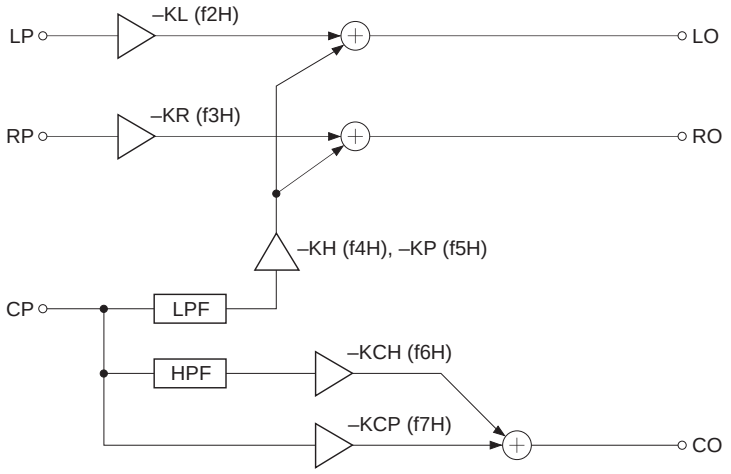
Table 8-1-6. Auto Input Balance ON/OFF

(5) Center Mode Control

[Relevant data] Coefficients: KP (f5H), KH (f4h), KL (f2H), KR (f3H), KCP (f7H), KCH (f6H)
The center channel output mode can be set to Normal, Wide or Phantom mode as shown in Table 8-1-7 below.

Mode / Coefficient	KP (f5H)	KH (f4H)	KL (f2H)	KR (f3H)	KCP (f7H)	KCH (f6H)
Normal	e000H	e000H	d2cdH	d2cdH	0000H	e000H
Wide	0000H	0000H	d2cdH	d2cdH	e000H	0000H
Phantom	e000H	0000H	d2cdH	d2cdH	0000H	0000H

Table 8-1-7. Center Mode Control Setting Value Examples



Note) If KH is set to 0000H in Phantom center channel mode, the LPF is set to data through status and the data added to the L and R channels is CP × KP.

Fig. 8-1-2. Signal Flow for Center Mode Control (L, R, C-ch)

Note) In Phantom center channel mode, the center channel information is divided equally between the left and right speakers.

The level of each channel can be adjusted by changing the KP, KH, KL, KR, KCP and KCH setting values. In these cases, be sure to change only the shaded portions for each mode in Table 8-1-7.
However, make sure that KP = KH in Normal mode. In Phantom mode, set KH to 0000H and adjust the mix level to the left and right channels using KP.

The I/O levels for 8000H to ffffH are obtained by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})] \times (-4)$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
8000H	+12.04
c000H	+6.02
d2cdH	+3.00
e000H	0
e959H	–3.00
eff6H	–6.00
f7f6H	–12.00
ffffH	–78.27
0000H	–∞

Table 8-1-8. KP, KH, KL, KR, KCP, KCH and KS Setting Value Examples

* In Table 8-1-7, lowering the input level by 3dB using Kia (dcH) or Kis (ddH) raises the output level of the L and R channels by 3dB. In this case, attaching external parts as shown in the Application Circuit is recommended to increase the C and S channel gains.

(6) Passive Decoder (Surround Channel)

The surround channel is processed according to the flow shown in Fig. 8-1-3.
The setting method for each section is described below.

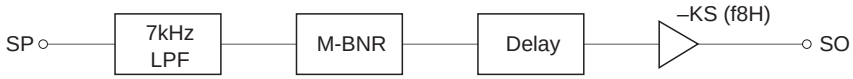


Fig. 8-1-3. Passive Decoder Signal Flow (S-ch)

(6)-1. Delay Time Setting

[Relevant data] Coefficient: Dly (fbH)

The surround channel delay time can be varied by setting the coefficient Dly value. (Dly is the delay line read address.)
Only the upper 11 of the 16 coefficient bits are used. The lower 5 bits are not used, and are ignored even if set.
That is to say, Dly can be set in 0020H increments, and the delay time can be set in approximately 0.022 ms increments.
The following condition also applies.

- 0020H ≤ Dly ≤ bfa0H

The coefficient value is calculated as follows.

$(Dly)_{Decimal} = (Delay\ [s] \times fs\ [Hz] \times 32$

Example) For 20ms (fs = 44100 [Hz])

$0.02 \times 44100 \times 32 = 28224 \xrightarrow{\text{Hexadecimal conversion}} 6e40H$

Setting value Dly (fbH)	Delay (fs = 44.1kHz)
0020H	0.022ms
0040H	0.045ms
.	.
.	.
52b0H	15.000ms
.	.
6e40H	20.000ms
.	.
89d0H	25.000ms
.	.
a560H	30.000ms
.	.
.	.
bf80H	34.739ms
bfa0H	34.762ms

Table 8-1-9. Surround Channel (S-ch) Delay Time Setting Value Examples

(6)-2. 7kHz Low-Pass Filter

[Relevant data] Coefficients: b2 (afH), b1 (b0H), a (b1H), –a (b2H)

The 7kHz LPF of the passive decoder can be turned on and off by setting the coefficients in Table 8-1-10.

	b2	b1	a	–a
ON	df66	5723	125e	eda2
OFF	0000	0000	0000	8000

Table 8-1-10. Passive Decoder 7kHz LPF ON/OFF Setting

(6)-3. Modified Dolby B-type NR

[Relevant data] Coefficients: aslw (b5H), 2D (b7H), KiA (d6H), Kia (dcH), Kis (ddH), Kdlb (faH)

The aslw and 2D coefficients and the ON/OFF coefficient Kdlb must be set for Modified Dolby B-type NR.

This function is turned on and off by setting Kdlb as shown in Table 8-1-11. The aslw and 2D coefficient values differ according to the Dolby level, prefilter and coefficient Kia/Kis (KiA) conditions. Table 8-1-12 shows typical setting value examples based on these three conditions. The prefilter gain (= –3.52dB) is the value when using the Application Circuit given in these specifications.

Consult your Sony representative with regard to use under conditions other than those noted in Table 8-1-12.

Coefficient Kdlb (faH)	ON = 2000H
	OFF = 0000H

Table 8-1-11. Modified Dolby B-type NR ON/OFF Setting

Prefilter	Dolby level	Kia (dcH)	Kis (ddH)	aslw (b5H)	2D (b7H)
–3.52dB	300mVrms	d2b2H	0000H	00caH	0033H
–3.52dB	300mVrms	c000H	0000H	009eH	004aH
–3.52dB	200mVrms	d2b2H	0000H	00caH	0023H
(Digital input)	–20dBFS	0000H	a563H	00caH	0023H

Table 8-1-12. Modified Dolby B-type NR Coefficient Value Examples for Different Input Level Conditions (during digital input: KiA (d6H) = 8000H)

(6)-4. Volume

[Relevant data] Coefficient: KS (f8H)

The KS (f8H) volume values are as shown in Table 8-1-8. See "5. Center Mode Control" for the calculation method.

(7) Simple SFC

Simple SFC effects can be added after Dolby Pro Logic Surround decoder processing. (See Fig. 8-1-1.)
Fig. 8-1-4 shows the signal flow for the simple SFC block.

When not using simple SFC, set the coefficients as follows to set the simple SFC block to through status.
KLV (00H), KRV (01H), KCV (02H), KSV (03H) = 8000H
KDV1 (21H), KDV2 (22H), KDV3 (23H), KLRm1 (24H), KLRm2 (25H), KLRm3 (26H) = 0000H

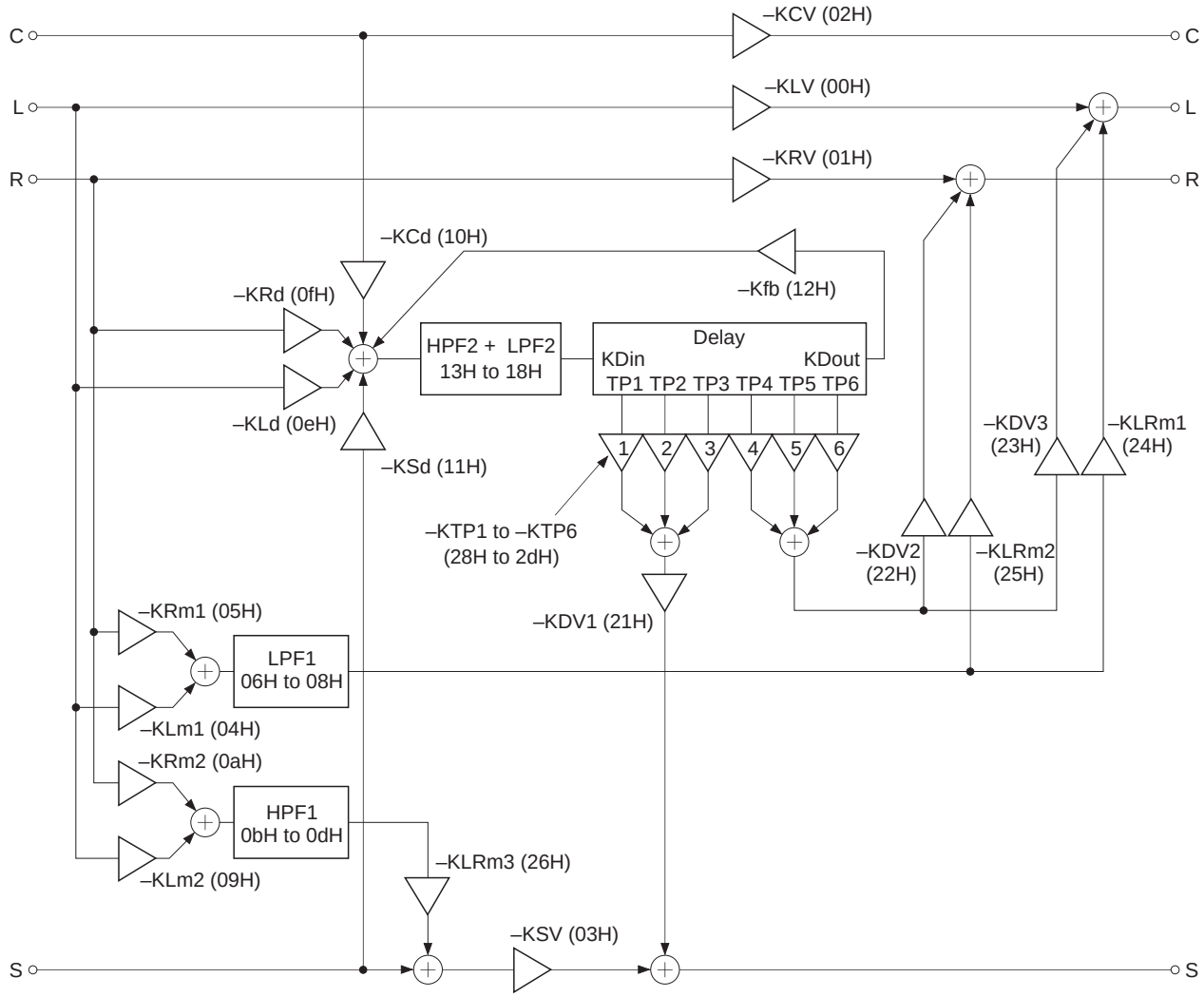


Fig. 8-1-4. Simple SFC Signal Flow

(7)-1. Volume Settings for Each Section

[Relevant data] Coefficients: KLV (00H), KRV (01H), KCV (02H), KSV (03H), KLm1 (04H), KRm1 (05H), KLm2 (09H), KRm2 (0aH), KLd (0eH), KRd (0fH), KCd (10H), KSd (11H), Kfb (12H), KDV1 (21H), KDV2 (22H), KDV3 (23H), KLRm1 (24H), KLRm2 (25H), KLRm3 (26H), KTP1 (28H), KTP2 (29H), KTP3 (2aH), KTP4 (2bH), KTP5 (2cH), KTP6 (2dH)

The format is the same as that described in "(3) Volume Coefficient Settings". The levels are as follows when 0dB = 8000H.

The I/O levels for 8000H to ffffH are obtained by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})] \times (-1)$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
8000H	0.00
a563H	–3.00
c000H	–6.02
d2b2H	–9.02
e000H	–12.04
f000H	–18.06
ffffH	–90.31
0000H	–∞

Table 8-1-13. Setting Value Examples for Each Volume (Negative Values)

The above coefficients are normally applied as negative values, but positive values should be applied when intentionally inverting the phase with TP1 to TP6, etc. In this case, the levels are as follows when 0dB = 7fffH.

The I/O levels for 7fffH to 0001H are obtained by the following formulas.

$$\text{(Coefficient value)} = [D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})]$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
7fffH	0.00
5a9dH	–3.00
4000H	–6.02
2d4eH	–9.02
2000H	–12.04
1000H	–18.06
0001H	–90.31
0000H	–∞

Table 8-1-14. Setting Value Examples for Each Volume (Positive Values)

(7)-2. Delay Line Settings

[Relevant data] Coefficients: KDin (19H), TP1 (1aH), TP2 (1bH), TP3 (1cH), TP4 (1dH), TP5 (1eH), TP6 (1fH), KDout (20H)

The Pro Logic mode delay lines are used for both the passive decoder short delay and the simple SFC reverberation, and are thus subject to the following restrictions:

- Dly + 0020H ≤ KDin (0020H ≤ Dly ≤ KDin – 0020H)
- 0020H ≤ TP* ≤ KDout
- KDin + KDout ≤ bfe0H

Dly (fbH): Pro Logic delay line read address
KDin (19H): Simple SFC delay line write address
TP1 to TP6 (1aH to 1fH): Simple SFC tap read addresses (determine the delay time for each tap)
KDout (20H): Simple SFC feedback loop read address (determines the maximum delay time)

Note) The minimum unit for all the above coefficients is "0020H". Values smaller than this are ignored.

The TP1 to TP6 and KDout addresses are specified in a different manner than Dly and KDin. These addresses are specified by the address value assuming KDin as the reference (= 0000H).
That is to say, the actual address is KDin + KDout, etc.
The coefficient values are calculated as follows.

$(Dly)_{Decimal} = (Delay\ [s]) \times fs\ [Hz] \times 32$

Example) When using 20ms for the passive decoder, and all remaining delay lines as reverberation

20ms → Dly = 6e40H
KDin = 6e40H + 0020H = 6e60H
KDout = bfe0H – 6e60H = 5180H
0020H ≤ TP1 to 6 ≤ 5180H

Setting value KDout, TP1 to TP6	Delay (fs = 44.1kHz)
0020H	0.022ms
0040H	0.045ms
.	.
.	.
1a60H	4.784ms
.	.
35f0H	9.784ms
.	.
5180H	14.784ms
.	.
6d10H	19.784ms
.	.
.	.
bf80H	34.739ms
bfa0H	34.762ms

Table 8-1-15. Simple SFC Delay Time Setting Value Examples

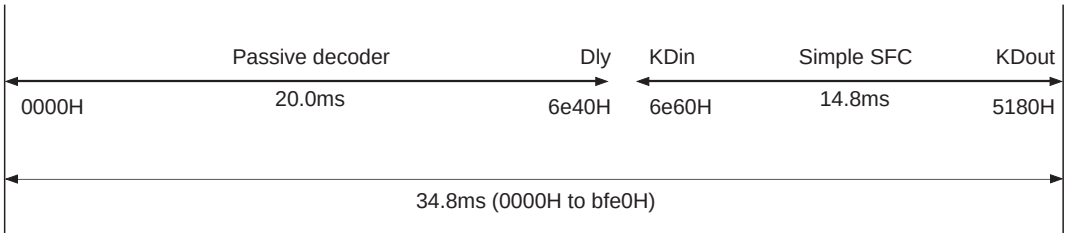


Fig. 8-1-5. Pro Logic Mode Delay Line Setting Example

(7)-3. Filters

[Relevant data] Coefficients: a0 (06H, 0bH, 13H, 16H), a1 (07H, 0cH, 14H, 17H), b (08H, 0dH, 15H, 18H)

LPF1, HPF1, LPF2 and HPF2 are comprised of primary IIR filters, and the coefficient setting and cut-off frequency relationship are as shown in Table 8-1-16.

Cut-off frequency [Hz]	LPF1, 2			HPF1, 2			Cut-off frequency [Hz]	LPF1, 2			HPF1, 2		
	a0	a1	b	a0	a1	b		a0	a1	b	a0	a1	b
100	FF19	00E7	7E30	80E8	7F18	7E30	5200	DC32	23CE	3863	A3CF	5C31	3863
200	FE34	01CC	7C67	81CD	7E33	7C67	5400	DB1D	24E3	3639	A4E4	5B1C	3639
300	FD53	02AD	7AA4	82AE	7D52	7AA4	5600	DA0C	25F4	3416	A5F5	5A0B	3416
400	FC74	038C	78E7	838D	7C73	78E7	5800	D8FD	2703	31F9	A704	58FC	31F9
500	FB99	0467	7731	8468	7B98	7731	6000	D7F2	280E	2FE2	A80F	57F1	2FE2
600	FAC1	053F	7580	8540	7AC0	7580	6200	D6E9	2917	2DD0	A918	56E8	2DD0
700	F9EB	0615	73D4	8616	79EA	73D4	6400	D5E3	2A1D	2BC4	AA1E	55E2	2BC4
800	F918	06E8	722E	86E9	7917	722E	6600	D4DF	2B21	29BD	AB22	54DE	29BD
900	F848	07B8	708E	87B9	7847	708E	6800	D3DE	2C22	27BB	AC23	53DD	27BB
1000	F77A	0886	6EF2	8887	7779	6EF2	7000	D2DF	2D21	25BD	AD22	52DE	25BD
1200	F5E6	0A1A	6BCB	8A1B	75E5	6BCB	7200	D1E3	2E1D	23C4	AE1E	51E2	23C4
1400	F45C	0BA4	68B6	8BA5	745B	68B6	7400	D0E8	2F18	21CF	AF19	50E7	21CF
1600	F2DB	0D25	65B4	8D26	72DA	65B4	7600	CFEF	3011	1FDD	B012	4FEE	1FDD
1800	F162	0E9E	62C3	8E9F	7161	62C3	7800	CEF8	3108	1DEF	B109	4EF7	1DEF
2000	EFF2	100E	5FE2	900F	6FF1	5FE2	8000	CE03	31FD	1C04	B1FE	4E02	1C04
2200	EE89	1177	5D11	9178	6E88	5D11	8200	CD0F	32F1	1A1C	B2F2	4D0E	1A1C
2400	ED28	12D8	5A4E	92D9	6D27	5A4E	8400	CC1D	33E3	1838	B3E4	4C1C	1838
2600	EBCE	1432	579A	9433	6BCD	579A	8600	CB2B	34D5	1655	B4D6	4B2A	1655
2800	EA7A	1586	54F3	9587	6A79	54F3	8800	CA3B	35C5	1475	B5C6	4A3A	1475
3000	E92D	16D3	5259	96D4	692C	5259	9000	C94D	36B3	1298	B6B4	494C	1298
3200	E7E6	181A	4FCB	981B	67E5	4FCB	9200	C85F	37A1	10BC	B7A2	485E	10BC
3400	E6A5	195B	4D48	995C	66A4	4D48	9400	C772	388E	0EE2	B88F	4771	0EE2
3600	E569	1A97	4AD0	9A98	6568	4AD0	9600	C685	397B	0D09	B97C	4684	0D09
3800	E432	1BCE	4863	9BCF	6431	4863	9800	C59A	3A66	0B32	BA67	4599	0B32
4000	E301	1CFF	4600	9D00	6300	4600	10000	C4AF	3B51	095C	BB52	44AE	095C
4200	E1D4	1E2C	43A6	9E2D	61D3	43A6	10200	C3C5	3C3B	0788	BC3C	43C4	0788
4400	E0AB	1F55	4155	9F56	60AA	4155	10400	C2DA	3D26	05B3	BD27	42D9	05B3
4600	DF87	2079	3F0D	A07A	5F86	3F0D	10600	C1F1	3E0F	03E0	BE10	41F0	03E0
4800	DE67	2199	3CCD	A19A	5E66	3CCD	10800	C107	3EF9	020D	BEFA	4106	020D
5000	DD4B	22B5	3A94	A2B6	5D4A	3A94	11000	C01E	3FE2	003A	BFE3	401D	003A
							OFF	8000	0000	0000	8000	0000	0000

Table 8-1-16. Simple SFC HPF and LPF Setting Coefficients

8-2. Dolby 3 Stereo Mode

This mode is a part of the Pro Logic adaptive matrix functions.
Specifically, surround output is muted and surround signal directionality is not harmonized.

(1) Setting Dolby 3 Stereo Mode

Dolby 3 Stereo mode must be set by the following procedures in order to achieve stable adaptive matrix operation. Setting Dolby 3 Stereo mode by procedures other than those given below may aggravate the decoder characteristics.

- Immediately after power-on reset
  i) Transfer the following setup data.
     SQA = 0030H (Field A)
     SQD = 7ee7H (Field D)
  Note) Field C is "All 0", so the DAC forced mute is applied.
  ii) Transfer the Dolby 3 Stereo mode coefficient data.
  iii) Transfer the setup data set in Dolby 3 Stereo mode.

- Changing to Dolby 3 Stereo mode from a different mode
  i) Apply the soft mute in the current mode.
  ii) Set the coefficients at the following addresses to "0000H".
     Addresses: 6eH to 7fH
  iii) Transfer the following setup data.
     SQA = 0030H (Field A)
     SQD = 7ee7H (Field D)
  Note) The DAC forced mute is not applied by Field C.
  iv) Transfer the Dolby 3 Stereo mode coefficients for the soft mute status.
  v) Transfer the setup data set in Dolby 3 Stereo mode.
  vi) Cancel the Dolby 3 Stereo mode soft mute.

(2) Setting Data

(2)-1. Setup Data

Table 8-3-1 lists the registers most closely related to Dolby 3 Stereo mode.
Setup data not listed in Table 8-3-1 may be set as desired, with due consideration given to the contents of Fields A to D noted in "6. Setup Register".

Register name	Setting value	Remarks
SQA14	"0"	1: Noise sequencer mode
SQA09, 08	"01"	01: Dolby 3 Stereo mode
SQA05, 04	"00"	01: SFC mode
SQB15 to 11	Don't care	Center channel (C-ch) trim volume

Table 8-2-1. Dolby 3 Stereo Mode Setup Register Settings

(2)-2. Coefficient Data

The coefficient data used in Dolby 3 Stereo mode is entirely the same as that for Pro Logic mode. See "8-1. Dolby Pro Logic Surround Mode".

8-3. Noise Sequencer Mode

(1) Setting Noise Sequencer Mode

Set noise sequencer mode by the following procedures.

- Immediately after power-on reset
  i) Transfer the setup data set in noise sequencer mode.
  ii) Transfer the noise sequencer mode coefficient data.
- Changing to noise sequencer mode from a different mode
  i) Apply the soft mute in the current mode.
  ii) Transfer the setup data set in noise sequencer mode.
  iii) Transfer the noise sequencer mode coefficient data.

(2) Setting Data

(2)-1. Setup Data

Table 8-3-1 lists the registers most closely related to noise sequencer mode.

Setup data not listed in Table 8-3-1 may be set as desired, with due consideration given to the contents of Fields A to D noted in "6. Setup Register".

Register name	Setting value	Remarks
SQA14	"1"	1: Noise sequencer mode
SQA09, 08	"00"	01: Dolby 3 Stereo mode
SQA05, 04	"00"	01: SFC mode
SQB15 to 11	Don't care	Center channel (C-ch) trim volume
SQB10 to 06	Don't care	Surround channel (S-ch) trim volume

Table 8-3-1. Noise Sequencer Mode Setup Register Settings

(2)-2. Coefficient Data

In noise sequencer mode, change the coefficients from addresses d0H to e2H of Pro Logic mode as shown in the table below. The other coefficients may be left as the Pro Logic mode coefficient settings.

	T1 (d0H)	T2 (d1H)	T3 (d2H)	T4 (d3H)
L-ch	2000	2000	2000	2000
C-ch	0000	3000	3000	3000
R-ch	0000	0000	4000	4000
S-ch	0000	0000	0000	5000
L → C → R → S	2000	3000	4000	5000
L → C → R	2000	3000	4000	4000

Table 8-3-2. Noise Sequencer Mode Coefficient Setting Values

Address	Fixed value
d4H	1000H
d5H	0040H
d6H	c000H
d7H	d2b1H
d8H	0000H
d9H	2d4fH
daH	0000H
dbH	d2b1H
dcH	c000H
ddH	d2b1H
deH	8000H
dfH	7789H
e0H	6f12H
e1H	0876H
e2H	6f14H

Table 8-3-3. Noise Sequencer Mode Coefficient Fixed Values

(3) Output Level Adjustment

[Relevant data] Coefficients: KL (f2H), KR (f3H), KH (f4H), KP (f5H), KCH (f6H), KCP (f7H), KS (f8H)

The noise output level in noise sequencer mode is adjusted by the center mode control coefficients (f2H to f7H) and the passive decoder volume coefficient (f8H)

See (5) and (6)-4 of "8-1. Pro Logic Mode".

8-4. SFC Mode

SFC mode is used for 2-channel stereo input, and realizes reverberation effects using the delay lines, and dynamics processing using 1/2 and 1/3 decimation and the compressor.

* This is a separate application from the simple SFC of Pro Logic mode.

(1) Setting SFC Mode

Set SFC mode by the following procedures.

- Immediately after power-on reset
  - i) Transfer the setup data set in SFC mode.
  - ii) Transfer the SFC mode coefficient data.
- Changing to SFC mode from a different mode
  - i) Apply the soft mute in the current mode.
  - ii) Transfer the setup data set in SFC mode.
  - iii) Transfer the SFC mode coefficient data.

(2) Setting Data

(2)-1. Setup Data

Table 8-4-1 lists the registers most closely related to SFC mode.

Setup data not listed in Table 8-4-1 may be set as desired, with due consideration given to the contents of Fields A to D noted in "6. Setup Register".

Register name	Setting value	Remarks
SQA11, 10	Don't care	00: No decimation, 01: 1/2, 10: 1/3
SQA05, 04	"01"	01: SFC mode
SQB15 to 11	Don't care	Center channel (C-ch) trim volume
SQB10 to 06	Don't care	Surround channel (S-ch) trim volume
SQC07, 06	Don't care	00: No decimation, 01: 1/2, 1*: 1/3

Table 8-4-1. SFC Mode Setup Register Settings

(2)-2. Coefficient Data

The SFC mode coefficient data uses the RAM for the entire area. Also, like other modes, the coefficient data consists of fixed values and setting values.

- **Fixed values during SFC mode initialization**

  The following fixed values must be set in the coefficient RAM to ensure proper DSP internal operation.

Address	Fixed value	Address	Fixed value	Address	Fixed value	Address	Fixed value
00H	7fe8H	46H	34eeH	56H	fb5cH	76H	f5b8H
01H	7fd1H	47H	0000H	57H	f8e3H	77H	075cH
38H	0000H	48H	6000H	58H	fbf6H	78H	fa97H
39H	0092H	49H	ff80H	59H	0575H	79H	0402H
3aH	0209H	4aH	00a1H	5aH	129cH	7aH	fd0bH
3bH	02cdH	4bH	016eH	5bH	1e0dH	7bH	0225H
3cH	0109H	4cH	01f8H	5cH	2294H	7cH	fe7cH
3dH	fda9H	4dH	0193H	6dH	051eH	7dH	01d3H
3eH	fd19H	4eH	0024H	6eH	ff86H	7eH	f312H
3fH	0189H	4fH	fe70H	6fH	02a0H	7fH	4b85H
40H	058aH	50H	fdbaH	70H	f6c0H	80H	0000H
41H	016dH	51H	fed8H	71H	2715H	94H	7fffH
42H	f7beH	52H	015aH	72H	4000H	d7H	68a9H
43H	f72aH	53H	037fH	73H	5149H	d8H	5121H
44H	0a4eH	54H	0344H	74H	e571H	daH	7ff4H
45H	2706H	55H	ffffH	75H	0f4eH	dbH	7fe8H

Table 8-4-2. SFC Mode Fixed Value Coefficients

• **SFC mode user setting coefficients**

The relationships between the coefficient RAM and each function during SFC mode operation are as follows.

Address	Symbol	Function	Setting value
02H	k	Compressor gain coefficient	See Table 8-5-7.
03H	XthP	Compressor threshold value (+)	See Table 8-5-7.
04H	XthM	Compressor threshold value (–)	See Table 8-5-7.
05H	Ksd	Compressor ON/OFF	0000 = OFF, 8000 = ON
06H	Ap	Compressor parameter	See Table 8-5-7.
07H	Am	Compressor parameter	See Table 8-5-7.
08H	Bp	Compressor parameter	See Table 8-5-7.
09H	Bm	Compressor parameter	See Table 8-5-7.
0aH	Cp	Compressor parameter	See Table 8-5-7.
0bH	Cm	Compressor parameter	See Table 8-5-7.
0cH	KLsri	Delay line L-ch input volume	See Table 8-5-5.
0dH	KRsri	Delay line R-ch input volume	See Table 8-5-5.
0eH	Kfb	Delay line feedback coefficient	See Tables 8-5-5, 6.
0fH	ahd	Feedback loop internal Hi-dump filter coefficient	See Table 8-2-8.
10H	a00	Feedback loop internal LPF0 parameter	See Tables 8-5-9, 10, 11.
11H	a01	Feedback loop internal LPF0 parameter	See Tables 8-5-9, 10, 11.
12H	a02	Feedback loop internal LPF0 parameter	See Tables 8-5-9, 10, 11.
13H	b01	Feedback loop internal LPF0 parameter	See Tables 8-5-9, 10, 11.
14H	b02	Feedback loop internal LPF0 parameter	See Tables 8-5-9, 10, 11.
15H	KLtp0	Delay line L-ch Tap0 volume	See Tables 8-5-5, 6.
16H	KLtp1	Delay line L-ch Tap1 volume	See Tables 8-5-5, 6.
17H	KLtp2	Delay line L-ch Tap2 volume	See Tables 8-5-5, 6.
18H	KLtp3	Delay line L-ch Tap3 volume	See Tables 8-5-5, 6.
19H	KLtp4	Delay line L-ch Tap4 volume	See Tables 8-5-5, 6.
1aH	KRtp0	Delay line R-ch Tap0 volume	See Tables 8-5-5, 6.
1bH	KRtp1	Delay line R-ch Tap1 volume	See Tables 8-5-5, 6.
1cH	KRtp2	Delay line R-ch Tap2 volume	See Tables 8-5-5, 6.
1dH	KRtp3	Delay line R-ch Tap3 volume	See Tables 8-5-5, 6.
1eH	KRtp4	Delay line R-ch Tap4 volume	See Tables 8-5-5, 6.
1fH	KStp0	Delay line S-ch Tap0 volume	See Tables 8-5-5, 6.
20H	KStp1	Delay line S-ch Tap1 volume	See Tables 8-5-5, 6.
21H	KStp2	Delay line S-ch Tap2 volume	See Tables 8-5-5, 6.
22H	KStp3	Delay line S-ch Tap3 volume	See Tables 8-5-5, 6.
23H	b0	All pass filter 0 coefficient	See Tables 8-5-5, 6.
24H	b1	All pass filter 1 coefficient	See Tables 8-5-5, 6.
25H	KLdry	L-ch direct sound mix volume	See Table 8-5-5.
26H	KRdry	R-ch direct sound mix volume	See Table 8-5-5.

Table 8-4-3 (1). SFC Mode Setting Value Coefficients

Address	Symbol	Function	Setting value
27H	KLeff	L-ch reflected sound mix volume	See Table 8-5-5.
28H	KReff	R-ch reflected sound mix volume	See Table 8-5-5.
29H	KLlpi	LPF1 L-ch input volume	See Table 8-5-5.
2aH	KRlpi	LPF1 R-ch input volume	See Table 8-5-5.
2bH	a10	LPF1 parameter	See Table 8-5-9.
2cH	a11	LPF1 parameter	See Table 8-5-9.
2dH	a12	LPF1 parameter	See Table 8-5-9.
2eH	b11	LPF1 parameter	See Table 8-5-9.
2fH	b12	LPF1 parameter	See Table 8-5-9.
30H	KLlpo	LPF1 L-ch mix volume	See Table 8-5-5.
31H	KRlpo	LPF1 R-ch mix volume	See Table 8-5-5.
32H	KLod	L-ch output total volume	See Table 8-5-5.
33H	KRod	R-ch output total volume	See Table 8-5-5.
34H	KSod	S-ch output total volume	See Table 8-5-5.
35H	KLd	L-ch → C-ch mix volume	See Table 8-5-5.
36H	KRd	R-ch → C-ch mix volume	See Table 8-5-5.
37H	KCod	C-ch output total volume	See Table 8-5-5.
5dH	Kd	Compressor input volume (both L and R)	See Table 8-5-5.
81H	Ltp0	Delay line L-ch Tap0 read address	See Table 8-5-12.
82H	Ltp1	Delay line L-ch Tap1 read address	See Table 8-5-12.
83H	Ltp2	Delay line L-ch Tap2 read address	See Table 8-5-12.
84H	Ltp3	Delay line L-ch Tap3 read address	See Table 8-5-12.
85H	Ltp4	Delay line L-ch Tap4 read address	See Table 8-5-12.
86H	Rtp0	Delay line R-ch Tap0 read address	See Table 8-5-12.
87H	Rtp1	Delay line R-ch Tap1 read address	See Table 8-5-12.
88H	Rtp2	Delay line R-ch Tap2 read address	See Table 8-5-12.
89H	Rtp3	Delay line R-ch Tap3 read address	See Table 8-5-12.
8aH	Rtp4	Delay line R-ch Tap4 read address	See Table 8-5-12.
8bH	Stp0	Delay line S-ch Tap0 read address	See Table 8-5-12.
8cH	Stp1	Delay line S-ch Tap1 read address	See Table 8-5-12.
8dH	Stp2	Delay line S-ch Tap2 read address	See Table 8-5-12.
8eH	Stp3	Delay line S-ch Tap3 read address	See Table 8-5-12.
8fH	tp_fb	Delay line feedback read address	See Table 8-5-12.
90H	ap0_in	All pass filter 0 delay RAM write address	See Table 8-5-12.
91H	ap0_out	All pass filter 0 delay RAM read address	See Table 8-5-12.
92H	ap1_in	All pass filter 1 delay RAM write address	See Table 8-5-12.
93H	ap1_out	All pass filter 1 delay RAM read address	See Table 8-5-12.
d6H	KiA	Serial audio interface input volume	See Table 8-5-5.
d9H	Ke	De-emphasis ON/OFF	0000 = OFF, ac19 = ON
dcH	Kia	Analog input mix switch	See Table 8-5-4.
ddH	Kis	Digital input mix switch	See Table 8-5-5.

Table 8-4-3 (2). Coefficient RAM Setting Data in SFC Mode

(2)-3. Signal Flow

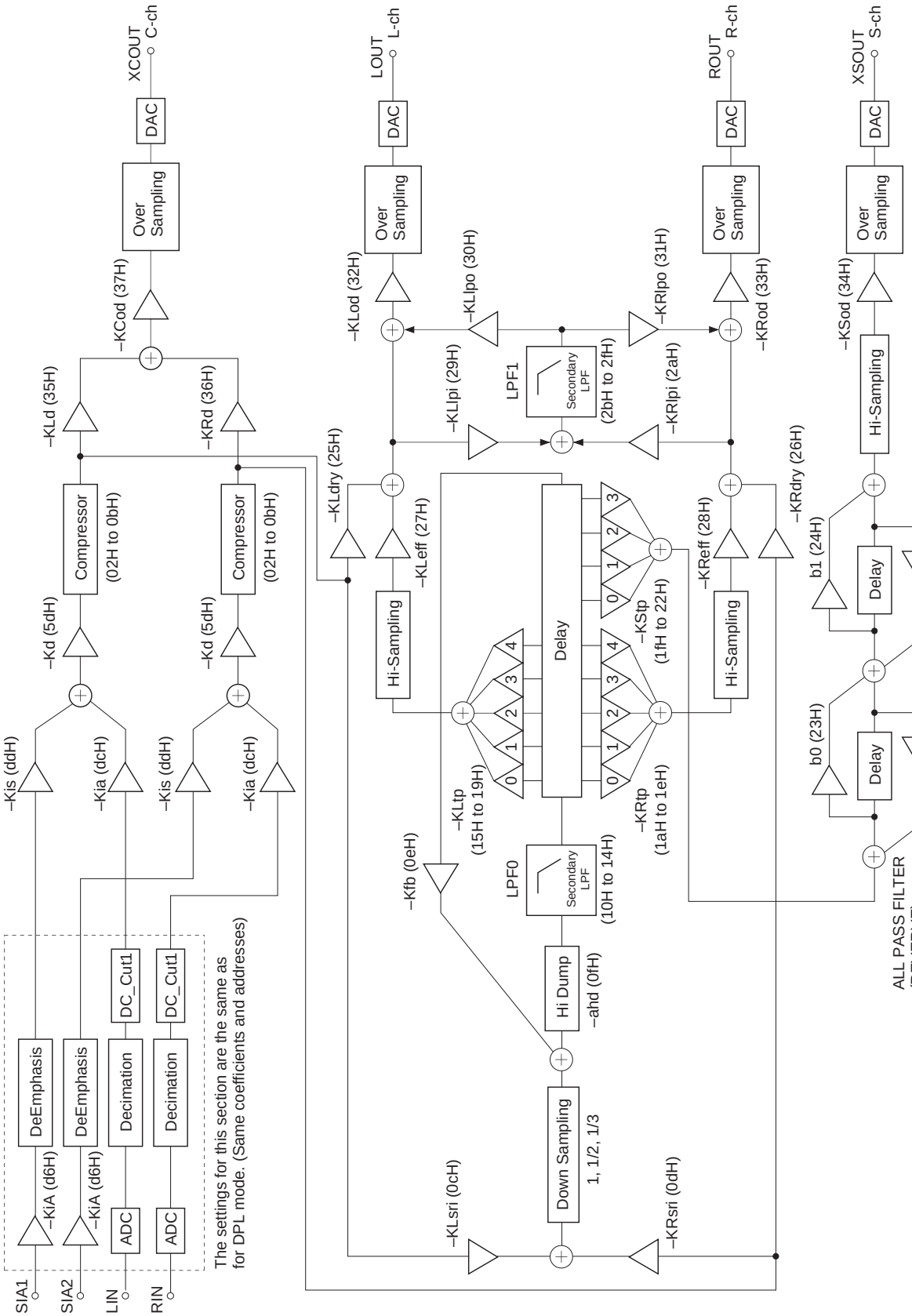


Fig. 8-4-1. Signal Flow for SFC Mode

(3) Volume Settings

[Relevant data] Coefficients: KLsri (0cH), KRsri (0dH), Kfb (0eH), KLtp0 (15H), KLtp1 (16H), KLtp2 (17H), KLtp3 (18H), KLtp4 (19H), KRtp0 (1aH), KRtp1 (1bH), KRtp2 (1cH), KRtp3 (1dH), KRtp4 (1eH), KStp0 (1fH), KStp1 (20H), KStp2 (21H), KStp3 (22H), b0 (23H), b1 (24H), KLdry (25H), KRdry (26H), KLeff (27H), KReff (28H), KLlpi (29H), KRlpi (2aH), KLlpo (30H), KRlpo (31H), KLod (32H), KRod (33H), KSod (34H), KLd (35H), KRd (36H), KCod (37H), Kd (5dH), KiA (d6H), Kia (dcH), Kis (ddH)

The I/O levels and volumes are 2's complement format with a decimal point between D15 and D14, and hexadecimal notation with D15 as MSB and D0 as LSB.
The coefficient and level relationships are as follows.

(3)-1. Kia (dcH): 0dB = c000H
The I/O levels for 8000H to ffffH are obtained by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})] \times (-2)$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
8000H	+6.02
c000H	0.00
e000H	–6.02
eff6H	–12.00
ffffH	–84.29
0000H	–∞

Table 8-4-4. Kia (dcH) Setting Value Examples

(3)-2. Other Coefficients
Except for Kia, the coefficients listed in the [Relevant data] above are basically specified by negative values (D15 to D0) with "0dB = 8000H". When intentionally inverting the phase, however, specify positive values with "0dB = 7fffH".
* The DSP calculation for coefficient values other than Kfb is (–1) × (D15 to D0).

The I/O levels for 8000H to ffffH are obtained by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})] \times (-1)$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
8000H	0.00
a563H	–3.00
c000H	–6.02
d2b2H	–9.02
e000H	–12.04
f000H	–18.06
ffffH	–90.31
0000H	–∞

Table 8-4-5. Setting Value Examples for Each Volume (Other than Kia, Negative Values)

The I/O levels for 7fffH to 0001H are obtained by the following formulas.

$$\text{(Coefficient value)} = [D15 + \sum_{n=0}^{14} (Dn \times 2^{n-15})]$$

I/O level = 20 log [coefficient value] dB

D15 to D0	Level [dB]
7fffH	0.00
5a9dH	–3.00
4000H	–6.02
2d4eH	–9.02
2000H	–12.04
1000H	–18.06
0001H	–90.31
0000H	–∞

Table 8-4-6. Setting Value Examples for Each Volume (Other than Kia, Positive Values)

(4) Compressor

[Relevant data] Coefficients: k (02H), XthP (03H), XthM (04H), Ksd (05H), Ap (06H), Am (07H), Bp (08H), Bm (09H), Cp (0aH), Cm (0bH)

The parameter table is shown in Table 8-4-7, and the I/O characteristics in Fig. 8-4-2.

Compressor ON: Ksd (05H) = 8000H
Compressor OFF: Ksd (05H) = 0000H

	Threshold		Gain	Coefficient					
	XthM	XthP	k	Ap	Am	Bp	Bm	Cp	Cm
Comp_5	–∞ [dB]		6.0 [dB]	–1.0 E000	1.0 2000	2.0 4000	2.0 4000	0 0000	0 0000
	0 0000	0 0000	2.0 4000						
Comp_4	–20 [dB]		5.2 [dB]	–100/99 DFAE	100/99 2052	200/99 40A5	200/99 40A5	–1/99 FEB6	1/99 014A
	–1/10 F334	1/10 0CCC	20/11 3A2E						
Comp_3	–17 [dB]		4.4 [dB]	–49/54 E2F7	49/54 1D09	52/27 3DA1	52/27 3DA1	–1/54 FDA2	1/54 025E
	–1/7 EDB7	1/7 1249	5/3 3555						
Comp_2	–14 [dB]		2.9 [dB]	–5/8 EC00	5/8 1400	33/20 34CC	33/20 34CC	–1/40 FCCD	1/40 0333
	–1/5 E667	1/5 1999	7/5 2CCC						
Comp_1	–9.5 [dB]		1.6 [dB]	–9/20 F19A	9/20 0E66	3/2 3000	3/2 3000	–1/20 F99A	1/99 0666
	–1/3 D556	1/3 2AAA	6/5 2666						

Table 8-4-7. Compressor Parameter Table

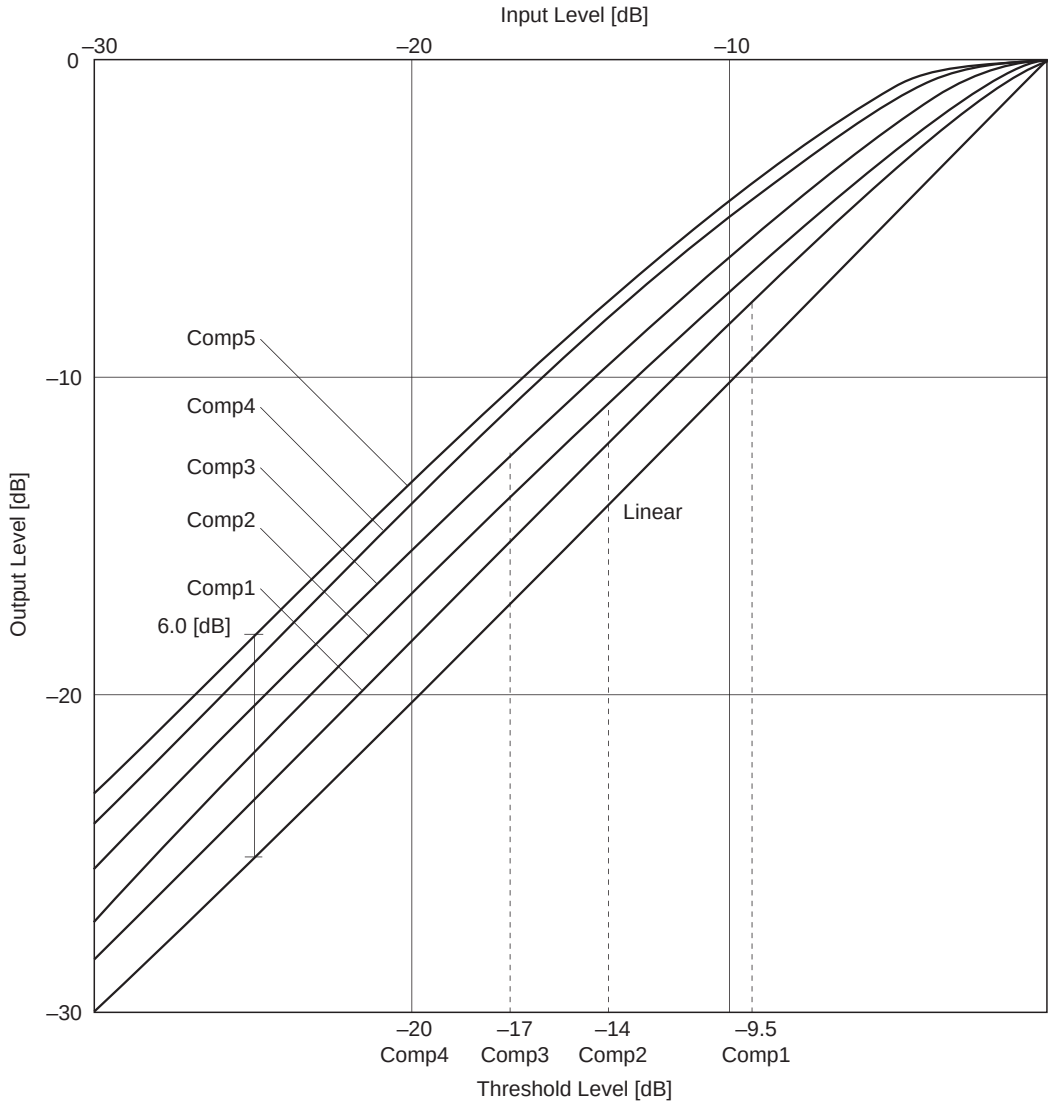


Fig. 8-4-2. Compressor I/O Characteristics

(5) Hi-Dump Filter Setting

[Relevant data] Coefficient: ahd (0fH)

This filter is used to attenuate the high frequencies. It is mainly used in the delay line feedback loop to prevent or alleviate noise generated when high frequency components are multiplied. Table 8-4-8 shows the parameter table.

To turn off this filter, set "ahd = 8000H".

fc [Hz]	–ahd			fc [Hz]	–ahd		
	1/1	1/2	1/3		1/1	1/2	1/3
40	EF46	FE8D	FDD5	1k	EF08	E073	D404
60	FEEA	FDD5	FCC3	2k	E073	C97A	B91E
80	FE8D	FD1E	FBB3	4k	C97A	AD94	9FC6
100	FE31	FC68	FAA6	6k	B91E	9FC6	974D
200	FC68	F8EA	F585	8k	AD94	9912	
400	F8EA	F23A	EBEE	10k	A578		
600	F585	EBEE	E32F	12k	9FC6		
800	F23A	E603	DB3B	14k	9BCC		

Table 8-4-8. Hi-Dump Filter Parameter Table

(6) Secondary LPF Settings

[Relevant data] Coefficients: a00 (10H), a01 (11H), a02 (12H), b01 (13H), b02 (14H), a10 (2bH), a11 (2cH), a12 (2dH), b11 (2eH), b12 (2fH)

These two LPF are comprised from the same secondary IIR filters. The parameter tables are shown in Tables 8-4-9 to 8-4-11. These tables show the parameters for no decimation, 1/2 decimation and 1/3 decimation, respectively.

Use Table 8-5-9 (No decimation) for LPF1.

The coefficients used for the LPF0 and LPF1 parameters are as follows.

LPF0: a00 (10H), a01 (11H), a02 (12H), b01 (13H), b02 (14H)
LPF1: a10 (2bH), a11 (2cH), a12 (2dH), b11 (2eH), b12 (2fH)

To turn off the filters, set only a00 and a10 to "8000H" and the other four coefficient values to "0000H".

Cut-off frequency [Hz]	a00 a10	a01 a11	a02 a12	b01 b11	b02 b12	Cut-off frequency [Hz]	a00 a10	a01 a11	a02 a12	b01 b11	b02 b12
5200	F4A5	16B6	0B5B	7FDF	D2B4	8200	E86A	2F2C	1796	3CC1	E4E8
5300	F448	176F	0BB8	7D90	D391	8300	E7F6	3014	180A	3A93	E545
5400	F3EB	182A	0C15	7B43	D469	8400	E781	30FD	187F	3867	E59E
5500	F38D	18E7	0C73	78F7	D53B	8500	E70C	31E8	18F4	363B	E5F4
5600	F32D	19A5	0CD3	76AD	D609	8600	E696	32D5	196A	3410	E647
5700	F2CD	1A65	0D33	7464	D6D2	8700	E61F	33C3	19E1	31E5	E695
5800	F26D	1B27	0D93	721C	D796	8800	E5A7	34B2	1A59	2FBB	E6E1
5900	F20B	1BEA	0DF5	6FD6	D855	8900	E52F	35A3	1AD1	2D92	E729
6000	F1A8	1CB0	0E58	6D91	D910	9000	E4B6	3695	1B4A	2B69	E76D
6100	F145	1D77	0EBB	6B4D	D9C6	9100	E43C	3788	1BC4	2941	E7AE
6200	F0E0	1E3F	0F20	690B	DA77	9200	E3C1	387D	1C3F	2719	E7EC
6300	F07B	1F09	0F85	66CA	DB24	9300	E346	3974	1CBA	24F2	E826
6400	F016	1FD5	0FEA	648A	DBCD	9400	E2CA	3A6C	1D36	22CB	E85D
6500	EFAF	20A2	1051	624B	DC71	9500	E24D	3B65	1DB3	20A5	E890
6600	EF47	2171	10B9	600D	DD10	9600	E1D0	3C60	1E30	1E7F	E8C0
6700	EEDF	2241	1121	5DD1	DDAC	9700	E152	3D5C	1EAE	1C5A	E8ED
6800	EE76	2313	118A	5B96	DE43	9800	E0D3	3E5A	1F2D	1A35	E917
6900	EE0D	23E7	11F3	595C	DED6	9900	E053	3F5A	1FAD	1810	E93D
7000	EDA2	24BC	125E	5723	DF66	10000	DFD3	405A	202D	15EB	E960
7100	ED37	2593	12C9	54EA	DFF0	10100	DF52	415D	20AE	13C7	E980
7200	ECCB	266B	1335	52B3	E077	10200	DED0	4261	2130	11A3	E99C
7300	EC5E	2744	13A2	507D	E0FA	10300	DE4D	4366	21B3	0F7F	E9B5
7400	EBF0	281F	1410	4E48	E179	10400	DDCA	446D	2236	0D5C	E9CB
7500	EB82	28FC	147E	4C14	E1F4	10500	DD45	4575	22BB	0B38	E9DD
7600	EB13	29DA	14ED	49E1	E26C	10600	DCC0	467F	2340	0915	E9ED
7700	EAA4	2AB9	155C	47AF	E2DF	10700	DC3B	478B	23C5	06F2	E9F9
7800	EA33	2B9A	15CD	457E	E34F	10800	DBB4	4898	244C	04CF	EA02
7900	E9C2	2C7C	163E	434D	E3BA	10900	DB2D	49A6	24D3	02AC	EA07
8000	E950	2D60	16B0	411E	E422	11000	DAA5	4AB7	255B	0089	EA0A
8100	E8DD	2E45	1723	3EEF	E487	OFF	8000	0000	0000	0000	0000

Table 8-4-9. Secondary LPF Parameter Table (No Decimation, Q = 0.707107)

Cut-off frequency [Hz]	a00	a01	a02	b01	b02	Cut-off frequency [Hz]	a00	a01	a02	b01	b02
2600	F4A5	16B6	0B5B	7FDF	D2B4	4100	E86A	2F2C	1796	3CC1	E4E8
2700	F3EB	182A	0C15	7B43	D469	4200	E781	30FD	187F	3867	E59E
2800	F32D	19A5	0CD3	76AD	D609	4300	E696	32D5	196A	3410	E647
2900	F26D	1B27	0D93	721C	D796	4400	E5A7	34B2	1A59	2FBB	E6E1
3000	F1A8	1CB0	0E58	6D91	D910	4500	E4B6	3695	1B4A	2B69	E76D
3100	F0E0	1E3F	0F20	690B	DA77	4600	E3C1	387D	1C3F	2719	E7EC
3200	F016	1FD5	0FEA	648A	DBCD	4700	E2CA	3A6C	1D36	22CB	E85D
3300	EF47	2171	10B9	600D	DD10	4800	E1D0	3C60	1E30	1E7F	E8C0
3400	EE76	2313	118A	5B96	DE43	4900	E0D3	3E5A	1F2D	1A35	E917
3500	EDA2	24BC	125E	5723	DF66	5000	DFD3	405A	202D	15EB	E960
3600	ECCB	266B	1335	52B3	E077	5100	DED0	4261	2130	11A3	E99C
3700	EBF0	281F	1410	4E48	E179	5200	DDCA	446D	2236	0D5C	E9CB
3800	EB13	29DA	14ED	49E1	E26C	5300	DCC0	467F	2340	0915	E9ED
3900	EA33	2B9A	15CD	457E	E34F	5400	DBB4	4898	244C	04CF	EA02
4000	E950	2D60	16B0	411E	E422	5500	DAA5	4AB7	255B	0089	EA0A
						OFF	8000	0000	0000	0000	0000

Table 8-4-10. Secondary LPF Parameter Table (1/2 Decimation, Q = 0.707107)

Cut-off frequency [Hz]	a00	a01	a02	b01	b02
1800	F3EB	182A	0C15	7B43	D469
1900	F2CD	1A65	0D33	7464	D6D2
2000	F1A8	1CB0	0E58	6D91	D910
2100	F07B	1F09	0F85	66CA	DB24
2200	EF47	2171	10B9	600D	DD10
2300	EE0D	23E7	11F3	595C	DED6
2400	ECCB	266B	1335	52B3	E077
2500	EB82	28FC	147E	4C14	E1F4
2600	EA33	2B9A	15CD	457E	E34F
2700	E8DD	2E45	1723	3EEF	E487
2800	E781	30FD	187F	3867	E59E
2900	E61F	33C3	19E1	31E5	E695
3000	E4B6	3695	1B4A	2B69	E76D
3100	E346	3974	1CBA	24F2	E826
3200	E1D0	3C60	1E30	1E7F	E8C0
3300	E053	3F5A	1FAD	1810	E93D
3400	DED0	4261	2130	11A3	E99C
3500	DD45	4575	22BB	0B38	E9DD
3600	DBB4	4898	244C	04CF	EA02
OFF	8000	0000	0000	0000	0000

Table 8-4-11. Secondary LPF Parameter Table (1/3 Decimation, Q = 0.707107)

(7) Delay Time Settings

[Relevant data] Coefficients: Ltp0 (81H), Ltp1 (82H), Ltp2 (83H), Ltp3 (84H), Ltp4 (85H), Rtp0 (86H), Rtp1 (87H), Rtp2 (88H), Rtp3 (89H), Rtp4 (8aH), Stp0 (8bH), Stp1 (8cH), Stp2 (8dH), Stp3 (8eH), tp_fb (8fH), ap0_in (90H), ap0_out (91H), ap1_in (92H), ap1_out (93H)

Setup: SQA05, SQA04, SQC07, SQC06

First, select No decimation, 1/2 decimation or 1/3 decimation.

1/1 (No decimation): SQA11, 10 = "00", SQC07, 06 = "00"
1/2 decimation: SQA11, 10 = "01", SQC07, 06 = "01"
1/3 decimation: SQA11, 10 = "10", SQC07, 06 = "1*" (* = Don't care)

Next, set tp_fb (8fH) which determines the comb filter delay time, and ap0_in (90H), ap0_out (91H), ap1_in (92H) and ap1_out (93H) which determine the all pass filter delay times.
The following conditions apply.

- 0 ≤ tp_fb, tp_fb + 0020H ≤ ap0_in ≤ ap0_out, ap0_out + 0020H ≤ ap1_in ≤ ap1_out ≤ bfe0H
- 0 ≤ Comb filter tap (Ltp0 to Stp3) ≤ tp_fb

Note) The minimum unit for all the above coefficients is "0020H". Values larger than this are ignored.

(7)-1. Comb Filter

First, set the comb filter maximum delay time tp_fb (8fH). The coefficient value is calculated as follows.

$(Dly)_{Decimal}$ = (Delay [s]) × fs [Hz] × 32
(The delay value is multiplied by 1/2 and 1/3 during 1/2 and 1/3 decimation, respectively.)

Next set the delay times for the comb filter taps, and calculate the coefficient values in the same manner as for tp_fb. (0 ≤ Tap ≤ tp_fb)

Example) For a maximum delay time of 36ms (1/2 decimation, fs = 44100Hz)
0.036 × (1/2) × 44100 × 32 = 25401.6
Rounding up to 25402 and converting to hexadecimal notation:
633aH
However, the address is specified in 0020H increments, so this becomes:
6340H
Therefore, set all (14) of the L, R and S channel taps to 6340H (36 ms) or less. For example, the L channel settings could be:
Ltp0 = 1ba0H (10ms)
Ltp1 = 2960H (15ms)
Ltp2 = 3720H (20ms)
Ltp3 = 44e0H (25ms)
Ltp4 = 52c0H (30ms)
Set the R and S channels in the same manner.

Setting value	Delay (fs = 44.1kHz)		
	1/1 (No decimation)	1/2 decimation	1/3 decimation
0020H	0.022ms	0.045ms	0.068ms
0040H	0.045ms	0.090ms	0.136ms
.	.	.	.
.	.	.	.
3720H	10.000ms	20.000ms	30.000ms
.	.	.	.
6e40H	20.000ms	40.000ms	60.000ms
.	.	.	.
a560H	30.000ms	60.000ms	90.000ms
.	.	.	.
bf80H	34.739ms	69.478ms	104.217ms
bfa0H	34.761ms	69.523ms	104.285ms

Table 8-4-12. SFC Mode Delay Time Setting Value Examples

(7)-2. All Pass Filters (APF0, APF1)

The all pass filter delay times are determined by (read address) – (write address - 0020H). Set ap*_in and ap*_out so that this subtraction results in the target delay time setting value. The calculation method is the same as that for tp_fb.

Example) When setting a maximum comb filter delay time of 36ms and splitting the remainder evenly between APF0 and APF1.

(1/2 decimation)

(bfe0H – 6340H)/2 = 2e50H

The address is specified in 0020H increments, so 2e40H is used for APF0, and 2e60H for APF1.

tp_fb = 6340H, so:

ap0_in = 6360H, ap0_out = 6340H + 2e40H = 9180H

ap1_in = 91a0H, ap1_out = 9180H + 2e60H = bfe0H

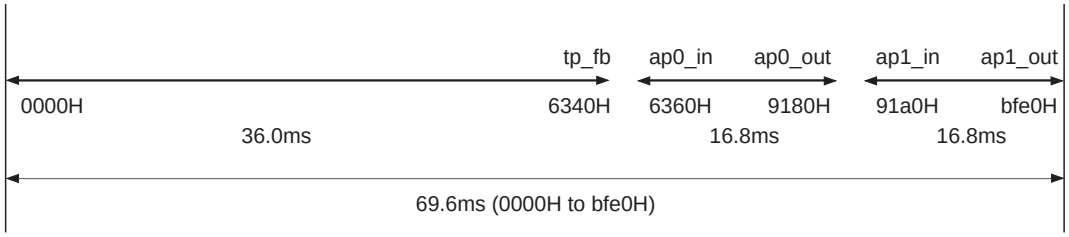


Fig. 8-4-3. Delay Time Setting Example (1/2 Decimation)

Note) Assuming the tap read address to be 0000H, the comb filter has a delay time of "0". However, the all pass filters are delayed by one sample after reading from the delay RAM.

Therefore, perfect through operation is not possible even if (write address) = (read address).

8-5. Bypass Mode

In this mode, the DSP is bypassed. The ADC and DAC are not used and both the L and R channels are in analog-to-analog through status.

(1) Setting Bypass Mode

Set the uppermost bit (SQA15) of setup register Field A to "1".
The other setup data and coefficient data is "Don't care".

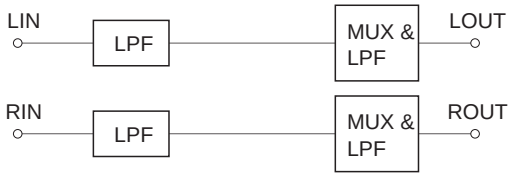


Fig. 8-5-1. Bypass Mode

In bypass mode, the output after ADC prefilter and the output after DAC postfilter are swtiched by the analog switch. The popping noise occurs at switching due to the difference of these filter's reference voltages (500mV). Therefore, the countermeasure against the noise, such as the system muting, is required when using this mode.

Appendix 1. Soft Mute

The condition where the final volume coefficient data connected to the CXD2719Q output of each mode is off (= 0000H) is called "soft mute".
(Soft mute cannot be applied in bypass mode.)

Table 9 shows the coefficients that should be set to 0000H in each mode during soft mute. Table 9 also includes the loop input volume coefficients and feedback volume coefficients for modes which contain a feedback loop.

Mode name	Coefficient name (Address [H])
Pro Logic mode	KLV (00), KRV (01), KCV (02), KSV (03), KLd (0e), KRd (0f), KCd (10), KSd (11), Kfb (12), KDV1 (21), KDV2 (22), KDV3 (23), KLRm1 (24), KLRm2 (25), KLRm3 (26), KL (f2), KR (f3), KH (f4), KP (f5), KCH (f6), KCP (f7), KS (f8)
Dolby 3 Stereo mode	Same as Pro Logic mode
Noise sequencer mode	Same as Pro Logic or Virtual mode
SFC mode	KLsri (0c), KRsri (0d), Kfb (0e), KLod (32), KRod (33), KSod (34), KCod (37)

Table 9. Recommended Mute Coefficients

RAM Initialization

Although this LSI contains a number of RAM, there is no clear function and the like. Therefore, it is impossible to predict the type of data existing in the RAM after power-on. Also, the previous mode's data remains even after the mode is changed, possibly causing momentary noise. If these problems cannot be handled by the system mute, apply soft mute for a time equal to the maximum delay time of the delay RAM (varies according to the mode and coefficient settings) during power-on and when changing the mode. This clears all the RAM.

Example 1) When using 20.0ms for the passive decoder and 14.8ms for the simple SFC delay line
The maximum delay time is 20.0ms, so soft mute must be applied continuously for 20.0ms.

Example 2) When using the delay RAM in SFC mode with 1/2 decimation
Comb filter delay time = 36.0ms
All pass filter delay time = 16.8ms
The maximum delay time is 36.0ms, so soft mute must be applied for 36.0ms.

Appendix 2. Compensation Filter

This filter compensates the shoulder characteristics of the digital filters. Fig. 9 shows the frequency response measured under the following conditions.

- Vin = 300mVrms (sine wave)
- Output level at 1kHz = 0dB
- DC cut filter cut-off = 5kHz

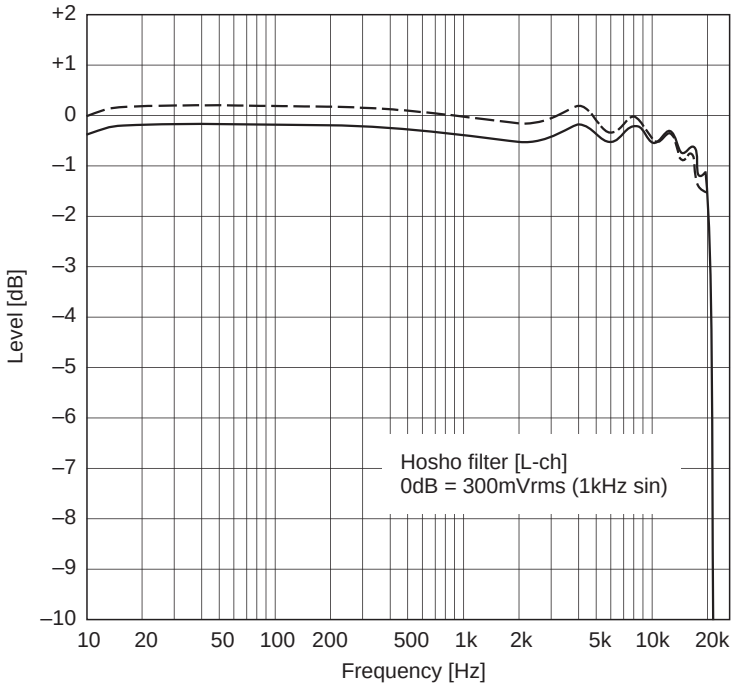
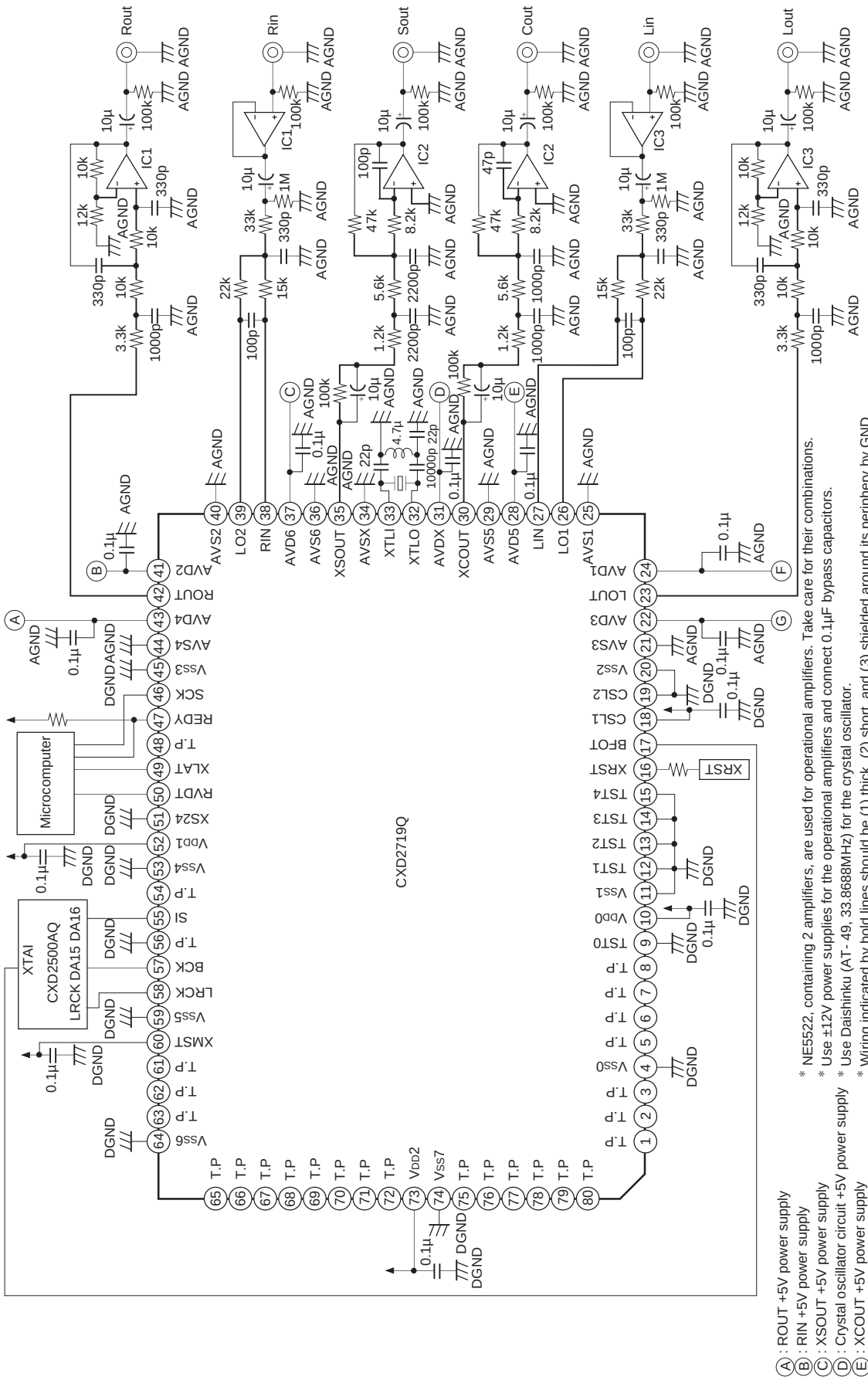


Fig. 9. Compensation Filter Frequency Response (Dotted line: Without the compensation filter)

Operation

Turn the filter on and off in each mode except bypass mode using SQA12 of setup register Field A. See "6. Setup Register".

Application Circuit



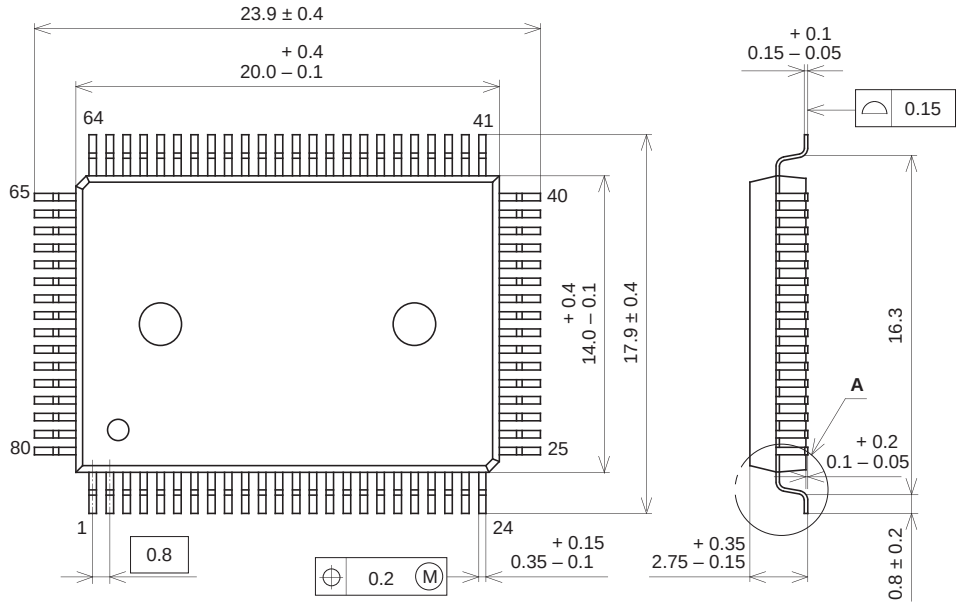
Ⓐ : ROUT +5V power supply
Ⓑ : RIN +5V power supply
Ⓒ : XSOUT +5V power supply
Ⓓ : Crystal oscillator circuit +5V power supply
Ⓔ : XCOUT +5V power supply
Ⓕ : LIN +5V power supply
Ⓖ : LOUT +5V power supply
: Digital +5V power supply

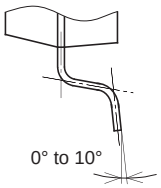
* NE5522, containing 2 amplifiers, are used for operational amplifiers. Take care for their combinations.
* Use ±12V power supplies for the operational amplifiers and connect 0.1µF bypass capacitors.
* Use Daishinku (AT- 49, 33.8688MHz) for the crystal oscillator.
* Wiring indicated by bold lines should be (1) thick, (2) short, and (3) shielded around its periphery by GND.
* Resistor deviation: ±1%, capacitor deviation: ±5%
(Especially , the deviation of the A/D converter front-stage resistor has a bad influence on the separation when using Pro Logic)
* The phases of the center and surround channels are invertedand output. Therefore, be sure to invert them by the external amplifier.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g