Low-Noise Matched Dual Monolithic Transistor

MAT02

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure ahttp://www.analog.com/marketSolutions/militaryAerospace/pdf/Die_Broc.pdf is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/MAT02

2.0 Part Number. The complete part number(s) of this specification follow:

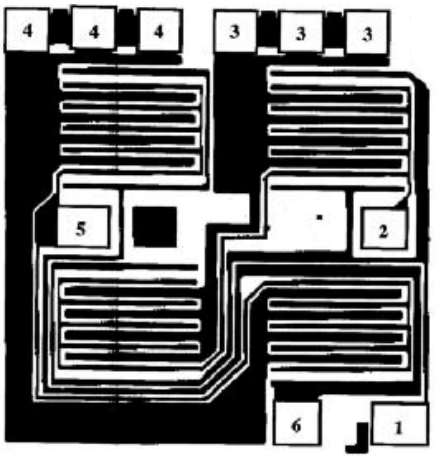
Part Number	Description
MAT02-000C	Low-Noise Matched Dual Monolithic Transistor

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
56 mil x 60 mil	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



1. C1
2. B1
3. E1
4. E2
5. B2
6. C2

Substrate can be connected to V- or floated.

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3.3 Absolute Maximum Ratings

Collector to Base Voltage (BV_{CBO})..... 40V
Collector to Emitter Voltage (BV_{CEO})..... 40V
Emitter to Emitter Voltage (BV_{EE})..... 40V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature (T_J).....+150°C
Operating Ambient Temperature Range..... -55°C to +125°C

Absolute Maximum Ratings Notes:
1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.
(a) Qual Sample Size and Qual Acceptance Criteria – 25/2
(b) Qual Sample Package – 6 Lead TO Package
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/		Limit Min	Limit Max	Units
Current Gain	h_{FE}	V_{CB} = 0V, 40V	I_C =1mA	500		
			I_C =100µA	500		
			I_C =10µA	400		
Current Gain Match 2/	Δh_{FE}	I_C=10µA, 100µA, 1mA; V_{CB} = 0V			2	%
Offset Voltage	V_{OS}	V_{CB} = 0V			50	µV
Offset Voltage vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	V_{CB} = 0V, 40V			25	µV
Offset Voltage vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} =0V; I_C =10µA, 1mA			25	µV
Input Offset Current	I_{OS}	V_{CB} = 0V, 40V			0.6	nA
Offset Current vs. V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	V_{CB} = 0V, 40V			70	pA/V
Bulk Emitter Resistance	r_{BE}				0.5	Ω

Table I - Dice Electrical Characteristics (Continued)					
Parameter	**Symbol**	**Conditions 1/**	**Limit Min**	**Limit Max**	**Units**
Bias Current	I_B	V_{CB} = 0V, 40V		25	nA
Collector Saturation Voltage	$V_{CE}SAT$	I_C = 1mA, I_B = 100µA		0.1	V
Breakdown Voltage	BV_{CEO}	I_C =100µA		40	V

Table I Notes:

1/ V_{CB} = 15V, I_C = ±10µA, and T_A = 25°C, unless otherwise specified.

2/ Current gain match (Δh_{FE}) is defined as $\Delta h_{FE} = \frac{100(\Delta I_B)h_{FE}min}{I_C}$.

Table II - Electrical Characteristics for Qual Samples						
Parameter	**Symbol**	**Conditions 1/**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
Current Gain	h_{FE}	I_C = 1mA; V_{CB} = 0V, 40V	1	450		
			2, 3	225		
		I_C =100µA, V_{CB} = 0V, 40V	1	450		
		I_C = 100µA, V_{CB} = 15V	2, 3	175		
		I_C = 10µA; V_{CB} = 0V, 40V	1	350		
		I_C = 10µA; V_{CB} = 15V	2, 3	125		
Current Gain Match 2/	Δh_{FE}	I_C = 10µA, 100µA, 1mA; V_{CB} = 0V	1		3	%
Offset Voltage	V_{OS}	V_{CB} = 0V	1		60	µV
			2, 3		90	
Offset Voltage vs. Temperature 4/	TCV_{OS}	V_{CB} = 0V			0.4	µV/°C
Offset Voltage vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	V_{CB} = 0V, 40V	1		40	µV
Offset Voltage vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} =0V; I_C =10µA, 1mA	1		40	µV
Input Offset Current	I_{OS}	V_{CB} = 0V, 40V	1		1	nA
			2, 3		10	
Offset Current vs. V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	V_{CB} = 0V, 40V	1		100	pA/V
Bulk Emitter Resistance	r_{BE}		1		0.75	Ω
Collector Base Leakage Current	I_{CBO}	V_{CB} = 40V	1		200	pA
Collector Emitter Leakage Current 3/	I_{CES}	V_{CE} = 40V, V_{BE} = 0V	1		200	pA
Collector-Collector Leakage Current 3/	I_{CC}	V_{CC} = 40V	1		200	pA
Bias Current	I_B	V_{CB} = 0V, 40V	1		30	nA
			2, 3		70	
Collector Saturation Voltage	$V_{CE}SAT$	I_C = 1mA, I_B = 100µA	1		0.1	V
Breakdown Voltage	BV_{CEO}	I_C = 100µA	1	40		

Table II Notes:

1/ V_{CB} = 15V, I_C = ±10µA, and T_A = 25°C, unless otherwise specified.

2/ Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)h_{FE}\min}{I_C}$.

3/ I_{CC} and I_{CES} are verified by measurement of I_{CBO}.

4/ Guaranteed by V_{OS} test ($TCV_{OS} \cong \underline{V_{OS}}$ for $V_{OS} << V_{BE}$) T=298°K for TA=+25°C.

Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table II with the following exceptions)								
Parameter	**Symbol**	**Sub-groups**	**Post Burn In Limit**		**Post Life Test Limit**		**Life Test Delta**	**Units**
			Min	**Max**	**Min**	**Max**		
Current Gain @ 1mA	h_{FE}	1	370		290		±80	
		2, 3			145			
Current Gain @ 100µA	h_{FE}	1	360		270		±90	
		2, 3			135			
Current Gain @ 10µA	h_{FE}	1	250		150		±100	
		2, 3			75			
Input Offset Current	I_{OS}	1		1.5		2	±0.5	nA
		2, 3				11.5		

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition A, B, or C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Feb. 28, 2002
B	Update web address	Aug. 5, 2003
C	Change Pin 4 from C2 to E2 and Pin 6 from E2 to C2	Oct. 15, 2004
D	Update 1.0 Scope description.	Aug. 2, 2007
E	Update header/footer & add to 1.0 Scope description	Feb. 19, 2008
F	Add Junction Temperature(T_J)….150°C to 3.3 Absolute Max Ratings	March 31, 2008
G	Updated Section 4.0c note to indicate pre-screen temp testing being performed.	6-JUN-2009
H	Updated fonts and sizes to ADI standards	7-Oct-2011