

NP30N06QDK

60 V – 30 A – Dual N-channel Power MOS FET Application: Automotive

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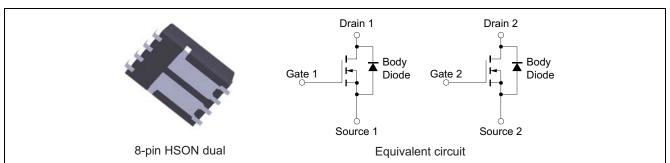
Description

NP29N06QDK is a dual N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
 - $R_{DS(on)1} = 14 \text{ m}\Omega$ MAX. ($V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$)
 - --- $R_{DS(on)2} = 21$ mΩ MAX. ($V_{GS} = 4.5$ V, $I_D = 7.5$ A)
- Low C_{iss} : $C_{iss} = 1500 \text{ pF TYP.}$ $(V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON dual

Outline



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP30N06QDK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON dual
NP30N06QDK-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T _C = 25°C) *4	I _{D(DC)}	±30	А
Drain Current (pulse) *1,4	I _{D(pulse)}	±120	Α
Total Power Dissipation (T _C = 25°C) *4	P _{T1}	59	W
Total Power Dissipation (T _A = 25°C) *2,4	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Repetitive Avalanche Current *3	I _{AR}	19	Α
Repetitive Avalanche Energy *3	E _{AR}	35	mJ

Thermal Resistance

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

*2. Mounted on glass epoxy substrate of 40 mm \times 40 mm \times 1.6 mmt with 4% copper area (35 $\mu\text{m})$

*3. R_G = 25 $\Omega,\,V_{GS}$ = 20 V \rightarrow 0 V

*4. One channel operation

Electrical Characteristics (T_A = 25°C)

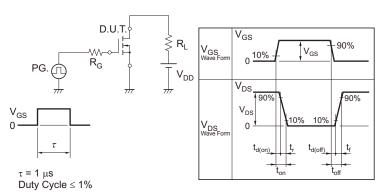
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	13	25		S	$V_{DS} = 5 \text{ V}, I_{D} = 15 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		11.5	14	mΩ	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$
Resistance *1	R _{DS(on)2}		16.5	21	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 7.5 \text{ A}$
Input Capacitance	C _{iss}		1500	2250	pF	V _{DS} = 25 V,
Output Capacitance	Coss		160	240	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		50	90	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		15	30	ns	$V_{DD} = 30 \text{ V}, I_D = 15 \text{ A},$
Rise Time	t _r		5	13	ns	V _{GS} = 10 V,
Turn-off Delay Time	t _{d(off)}		50	100	ns	$R_G = 0 \Omega$
Fall Time	t _f		3	8	ns	
Total Gate Charge	Q _G		25	38	nC	V _{DD} = 48 V,
Gate to Source Charge	Q _{GS}		5		nC	V _{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		4		nC	I _D = 30 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I _F = 30 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		25		ns	$I_F = 30 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		26		nC	di/dt = 100 A/μs

Note: *1. Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD} V_{DD} V_{DS} V_{DS} V_{DS} V_{DS} V_{DS} V_{DS} V_{DS}

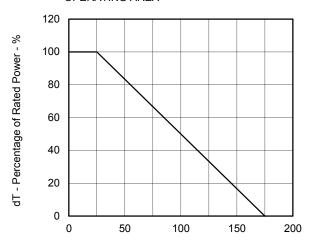
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

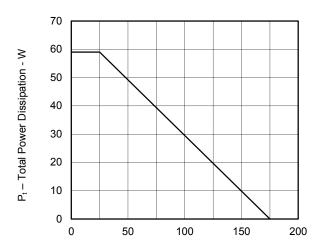
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



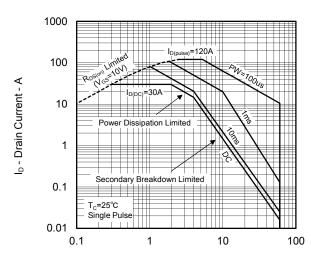
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



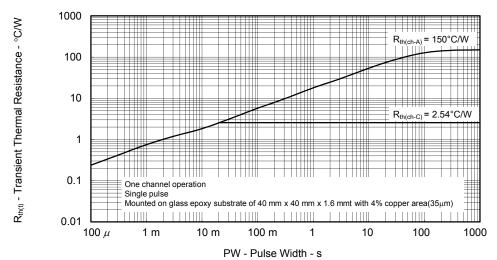
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



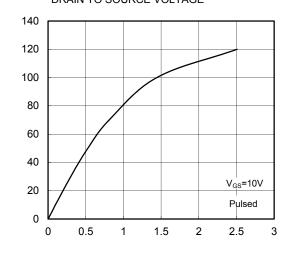
 V_{DS} - Drain to Source Voltage – V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



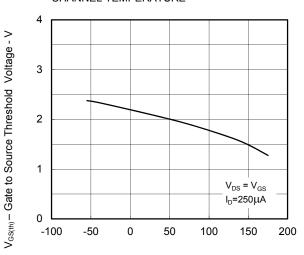
Ip - Drain Current - A

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



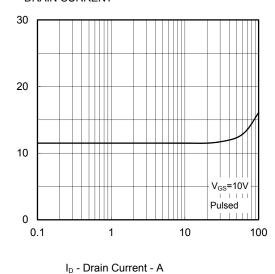
 V_{DS} - Drain to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

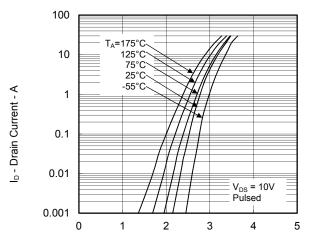


 T_{ch} - Channel Temperature - $^{\circ}C$

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

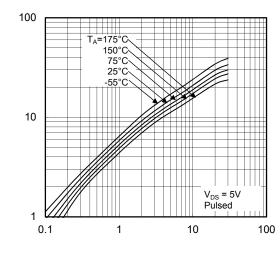


FORWARD TRANSFER CHARACTERISTICS



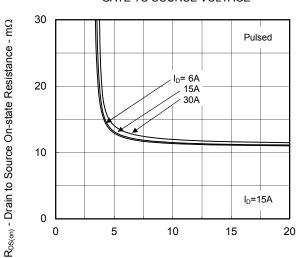
V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I_D - Drain Current - A

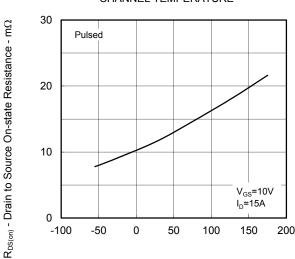
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



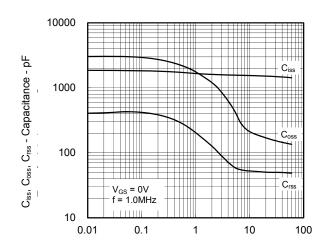
V_{GS} - Gate to Source Voltage - V

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

 $\mid y_{fs} \mid$ - Forward Transfer Admittance - S

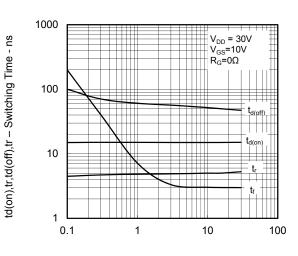


T_{ch} - Channel Temperature - °C



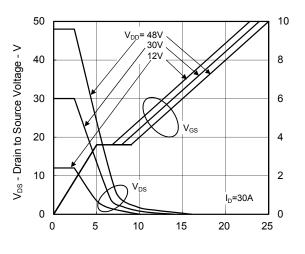
V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS



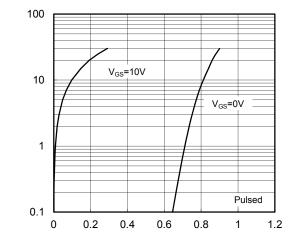
I_D - Drain Current - A

DYNAMIC INPUT CHARACTERISTICS



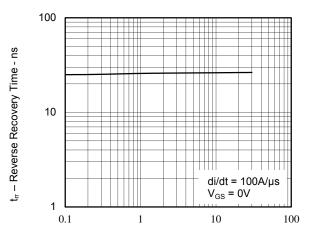
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{F(S-D)}$ - Source to Drain Voltage - V

REVERSE RECOVERY TIME vs. DRAIN CURRENT

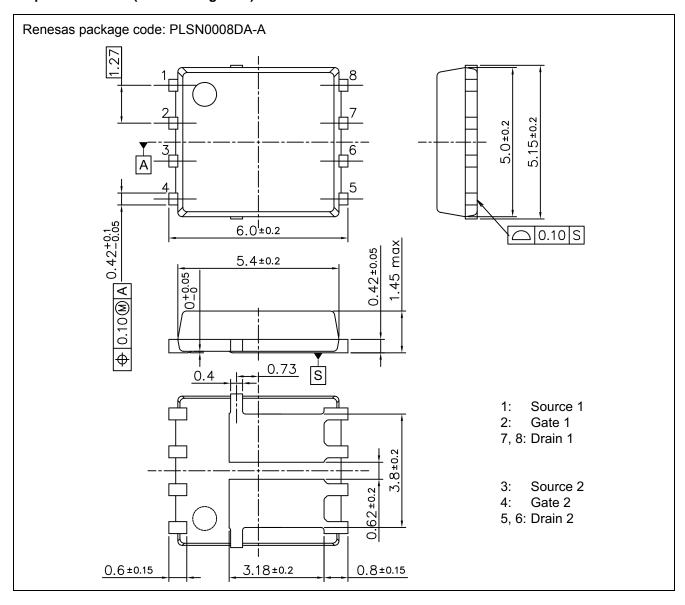


I_F - Drain Current - A

IF - Diode Forward Current - A

Package Drawings (Unit: mm)

8-pin HSON Dual (Mass: 0.12 g TYP.)



Revision History

NP30N06QDK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Mar 28, 2016	_	First Edition Issued	

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