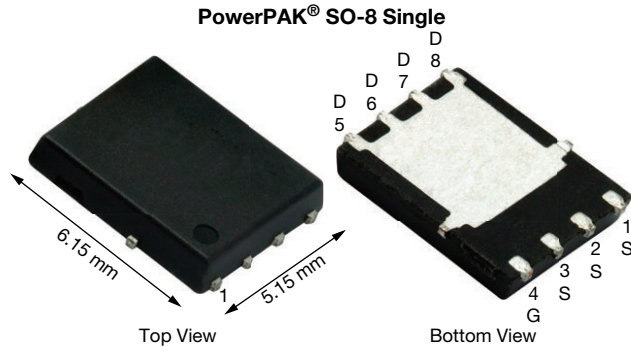


## N-Channel 25 V (D-S) MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	25
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00058
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.00082
$Q_g$ typ. (nC)	61
$I_D$ (A)	100 <sup>a, g</sup>
Configuration	Single

### FEATURES

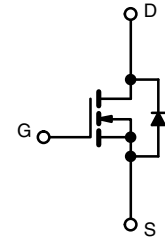
- TrenchFET<sup>®</sup> Gen IV power MOSFET
- Optimized  $Q_g$ ,  $Q_{gd}$ , and  $Q_{gd}/Q_{gs}$  ratio reduces switching related power loss
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Synchronous buck converter
- OR-ing
- Load switching
- Battery management



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8 Single
Lead (Pb)-free and halogen-free	SiRA20DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	25	V	
Gate-source voltage	$V_{GS}$	+16 / -12	V	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	100 <sup>a</sup>	A
		$T_C = 70$ °C	100 <sup>a</sup>	
		$T_A = 25$ °C	81.7 <sup>b, c</sup>	
		$T_A = 70$ °C	65.3 <sup>b, c</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	500	A	
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	94.5	A
		$T_A = 25$ °C	5.6 <sup>b, c</sup>	
Single pulse avalanche current	$I_{AS}$	60	A	
Single pulse avalanche energy	$E_{AS}$	180	mJ	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	104	W
		$T_C = 70$ °C	66.6	
		$T_A = 25$ °C	6.25 <sup>b, c</sup>	
		$T_A = 70$ °C	4 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	15	20	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	0.9	1.2	

### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 54 °C/W.
- $T_C = 25$  °C.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	25	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	21	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-4.8	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	-	2.1	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +16 / -12 V	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00048	0.00058	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	-	0.00065	0.00082	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	-	110	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	10 850	-	pF
Output capacitance	C <sub>OSS</sub>		-	3360	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	720	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	134	200	nC
		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	-	61	92	
Gate-source charge	Q <sub>gs</sub>		-	24	-	
Gate-drain charge	Q <sub>gd</sub>		-	9.2	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.1	0.38	0.75	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 0.5 Ω, I <sub>D</sub> ≅ 20 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	19	38	ns
Rise time	t <sub>r</sub>		-	24	48	
Turn-off delay time	t <sub>d(off)</sub>		-	53	105	
Fall time	t <sub>f</sub>		-	9	18	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 0.5 Ω, I <sub>D</sub> ≅ 20 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	51	100	
Rise time	t <sub>r</sub>		-	95	190	
Turn-off delay time	t <sub>d(off)</sub>		-	47	94	
Fall time	t <sub>f</sub>		-	16	32	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	94.5	A
Pulse diode forward current	I <sub>SM</sub>		-	-	300	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.71	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	63	126	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	87	174	nC
Reverse recovery fall time	t <sub>a</sub>		-	27	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	36	-	

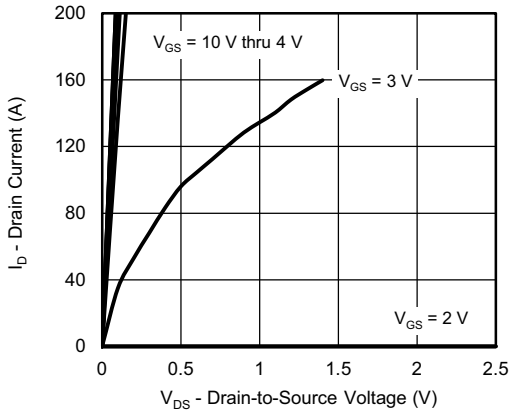
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

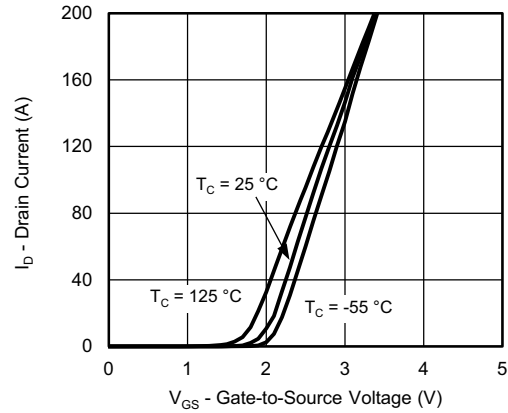
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



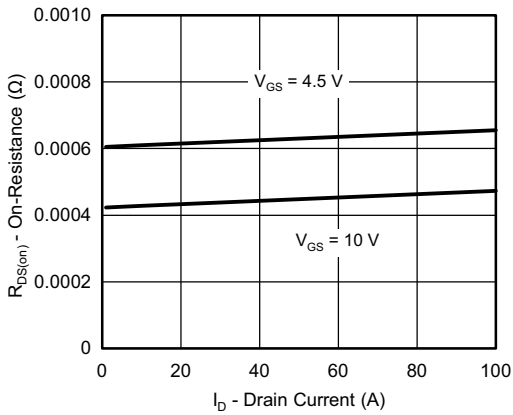
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



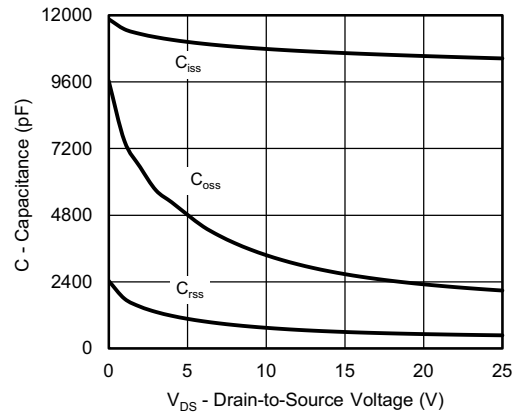
**Output Characteristics**



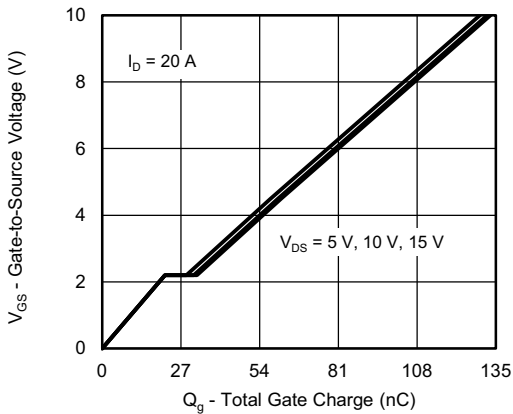
**Transfer Characteristics**



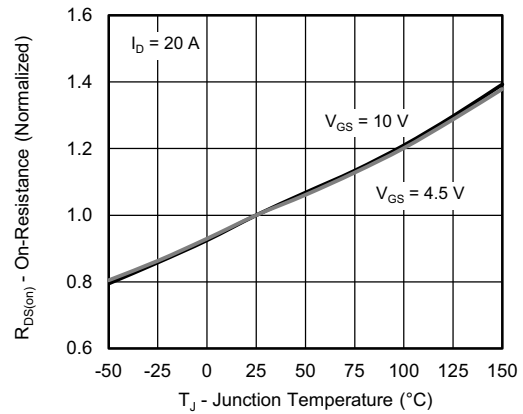
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



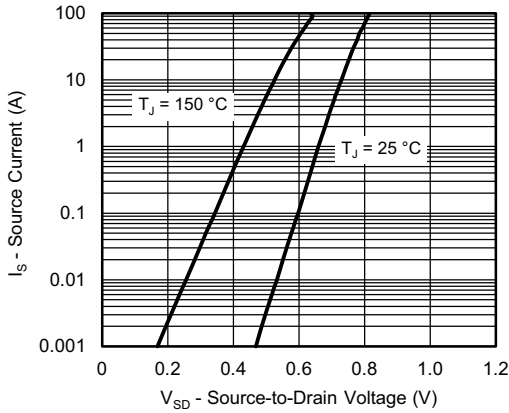
**Gate Charge**



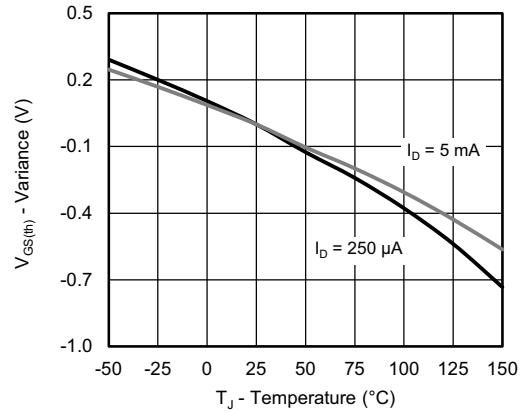
**On-Resistance vs. Junction Temperature**



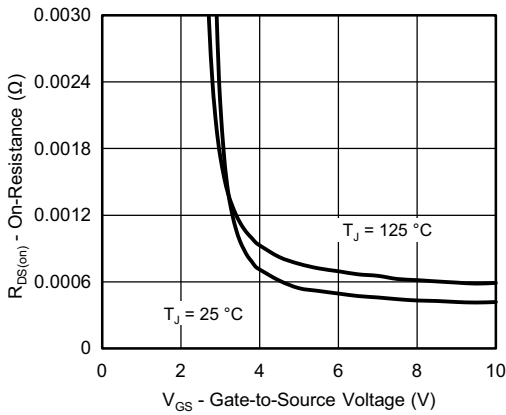
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



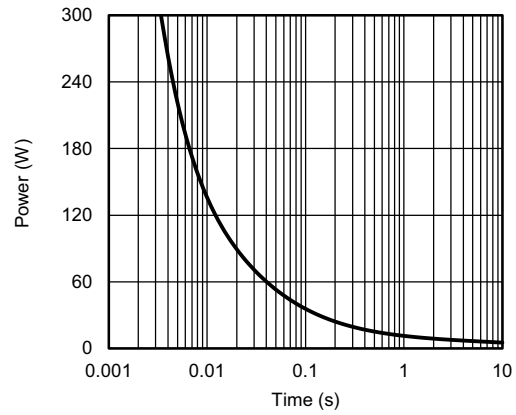
**Source-Drain Diode Forward Voltage**



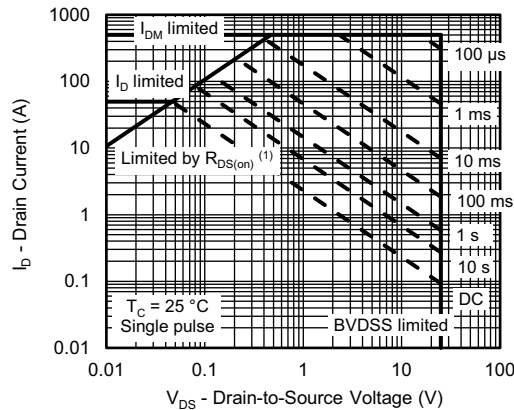
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



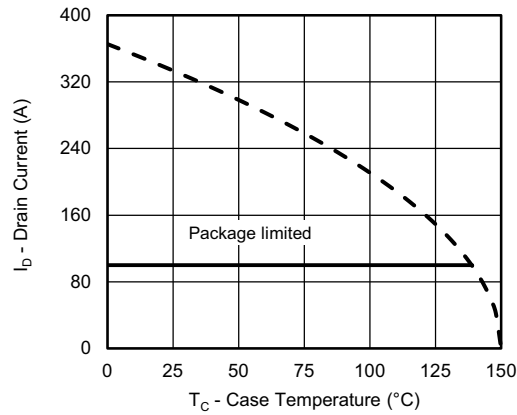
**Single Pulse Power, Junction-to-Ambient**



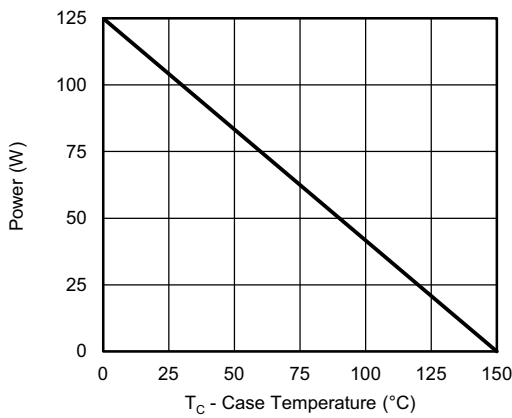
**Safe Operating Area, Junction-to-Ambient**



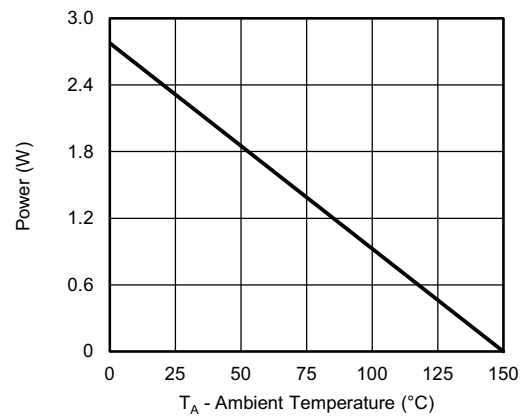
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



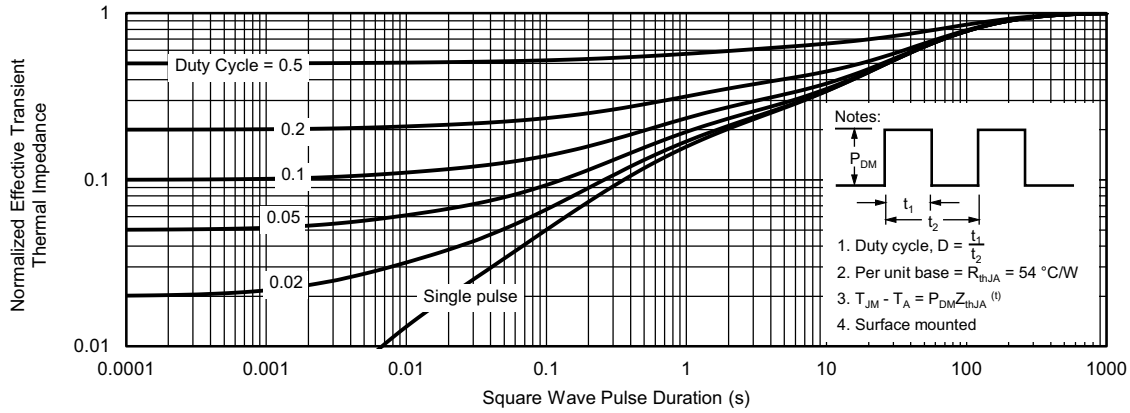
**Power, Junction-to-Ambient**

**Note**

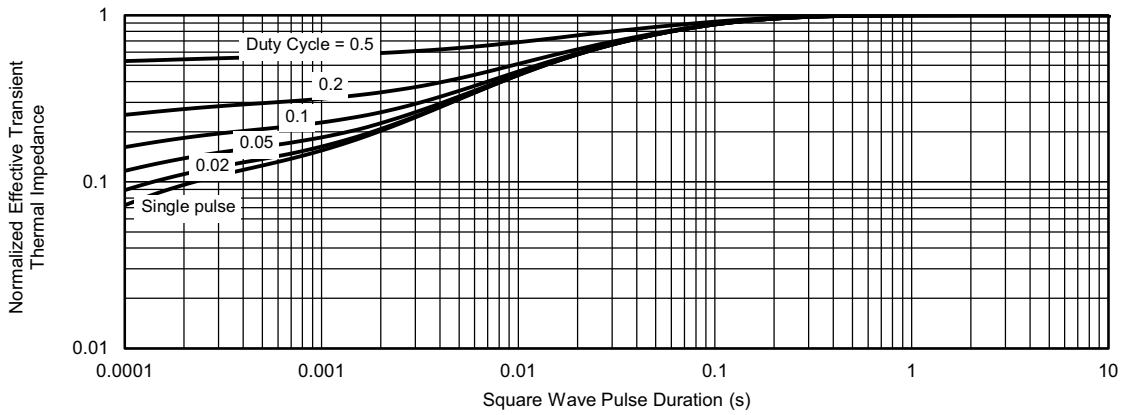
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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