

N-Channel 30 V (D-S) MOSFET

DESCRIPTION

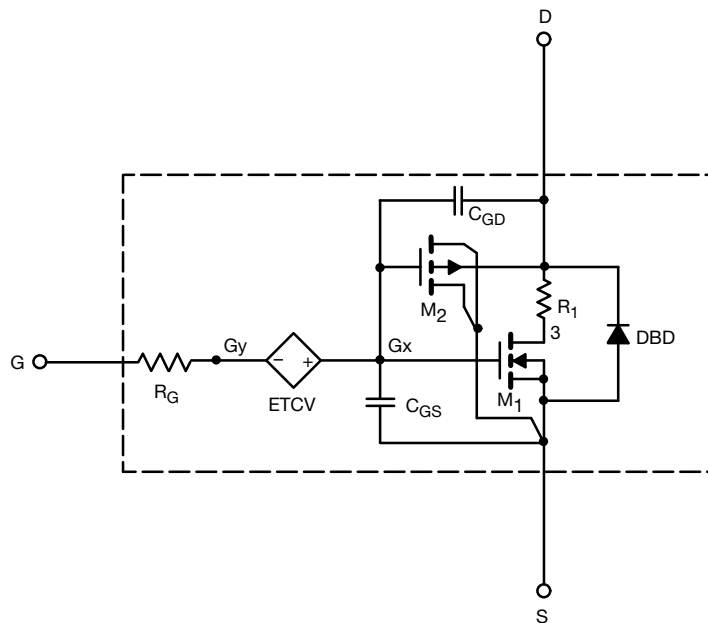
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



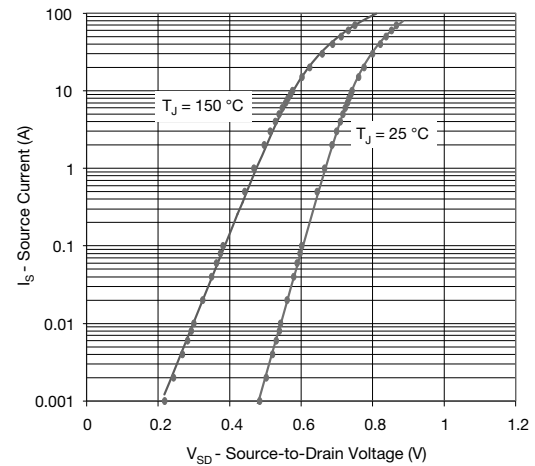
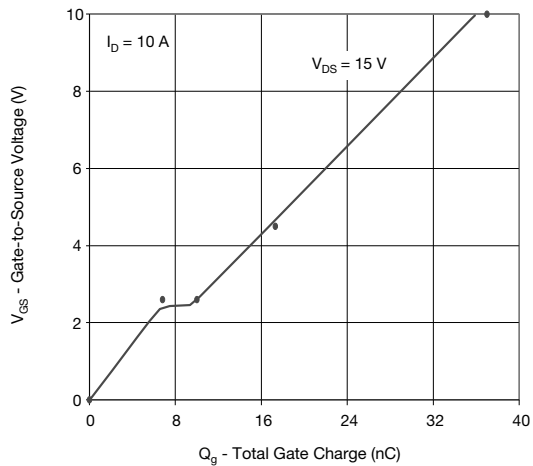
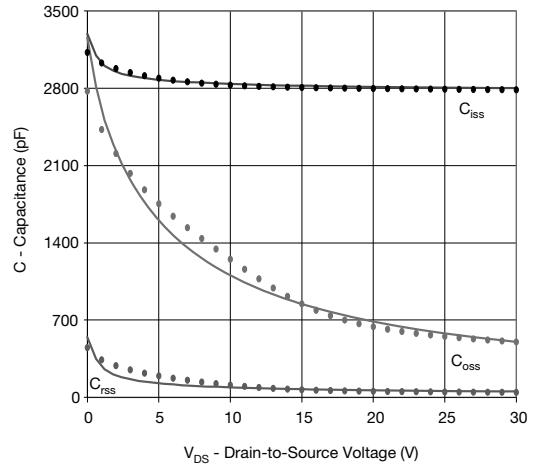
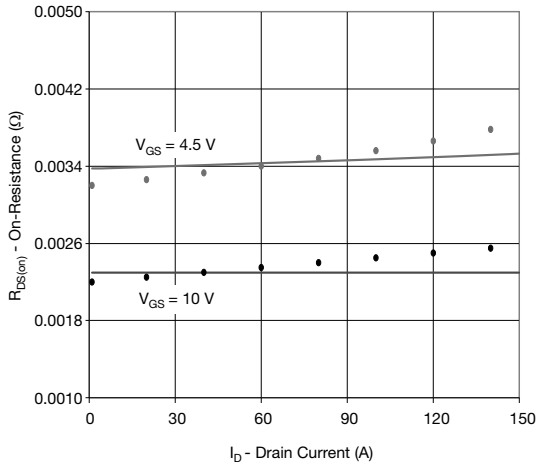
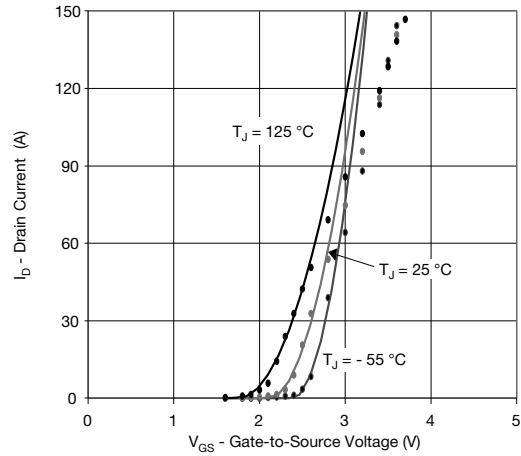
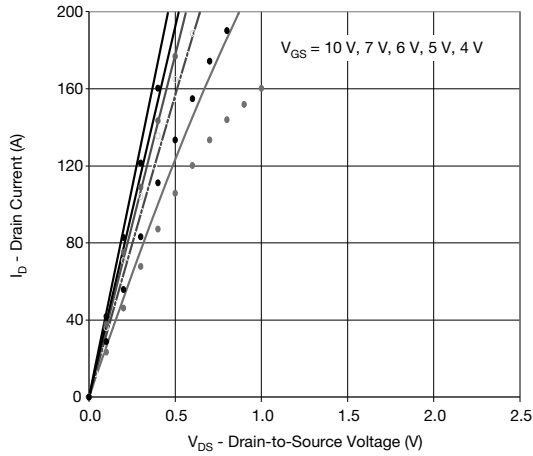
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.7	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	0.0023	0.0023	Ω
		V _{GS} = 4.5 V, I _D = 10 A	0.0034	0.0033	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A	99	115	S
Diode Forward Voltage	V _{SD}	I _S = 5 A	0.72	0.73	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	2820	2815	pF
Output Capacitance	C _{oss}		847	842	
Reverse Transfer Capacitance	C _{rss}		72	70	
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	37	37	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	17	17.3	
Gate-Source Charge	Q _{gs}		6.8	6.8	
Gate-Drain Charge	Q _{gd}		3.2	3.2	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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