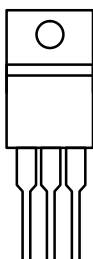


N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
100	0.021 at V _{GS} = 10 V	50 ^d	30.2 nC
	0.023 at V _{GS} = 8 V	49.7	
	0.028 at V _{GS} = 6 V	45	

TO-220AB



G D S

Top View

Ordering Information:

SUP50N10-21P-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

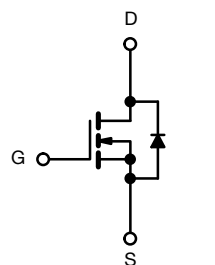
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/AC Inverters
- Primary Side Switching
- Synchronous Rectification



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
Pulsed Drain Current (t = 300 μs)	I _{DM}	60	
Avalanche Current	I _{AS}	40	
Single Avalanche Energy ^a	E _{AS}	80	mJ
Maximum Power Dissipation ^a	P _D	T _C = 25 °C	W
		T _A = 25 °C ^c	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W
Junction-to-Case (Drain)	R _{thJC}	1	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

c. When mounted on 1" square PCB (FR-4 material).

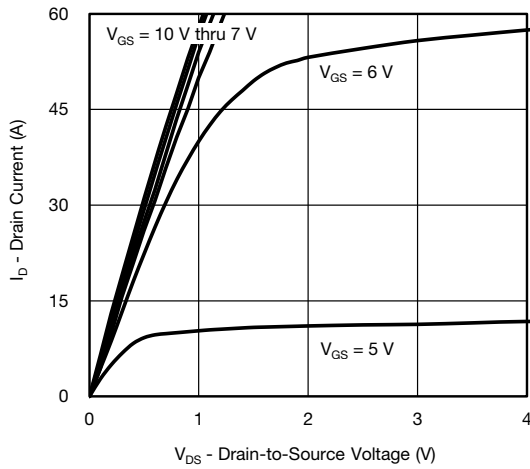
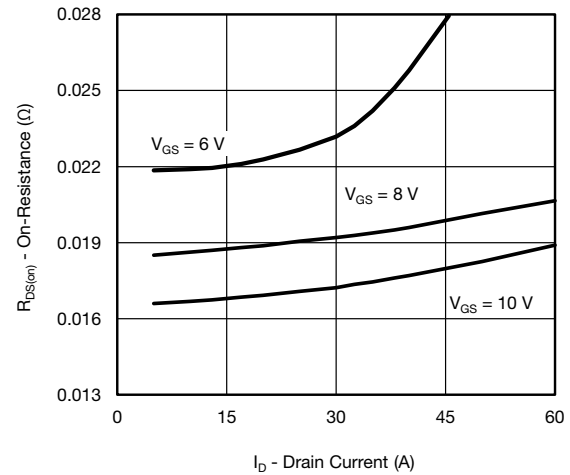
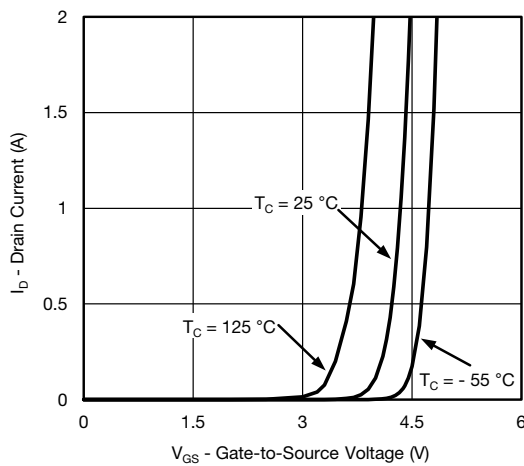
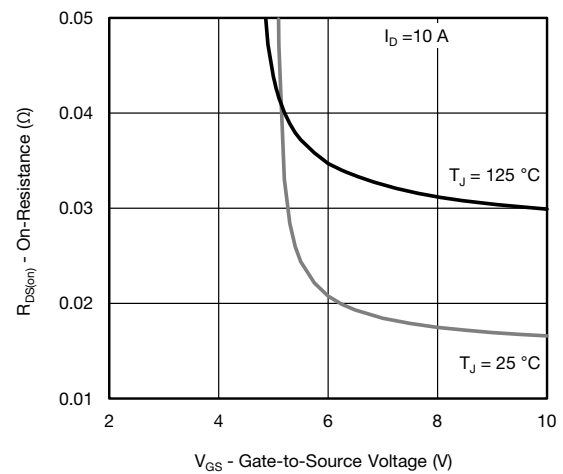
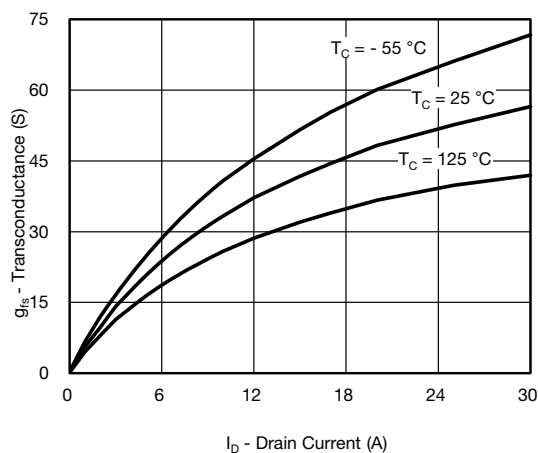
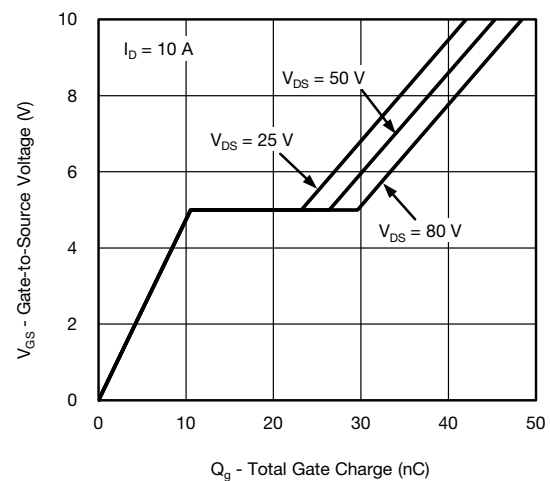
d. Package limited.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		0.017	0.021	Ω
		V _{GS} = 8 V, I _D = 9.6 A		0.019	0.023	
		V _{GS} = 6 V, I _D = 8.7 A		0.022	0.028	
Forward Transconductance ^a	g _{fs}	V _{DS} = 20 V, I _D = 10 A		40		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz		2055		pF
Output Capacitance	C _{oss}			227		
Reverse Transfer Capacitance	C _{rss}			120		
Total Gate Charge ^c	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A		45	68	nC
Gate-Source Charge ^c	Q _{gs}			10.5		
Gate-Drain Charge ^c	Q _{gd}			15.9		
Gate Resistance	R _g	f = 1 MHz	0.3	1.5	3	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 8 A, V _{GEN} = 10 V, R _g = 1 Ω		10	20	ns
Rise Time ^c	t _r			10	20	
Turn-Off Delay Time ^c	t _{d(off)}			22	33	
Fall Time ^c	t _f			7	14	
Drain-Source Body Diode Ratings and Characteristics (T _C = 25 °C) ^b						
Continuous Current	I _S				50	A
Pulsed Current	I _{SM}				60	
Forward Voltage ^a	V _{SD}	I _F = 8 A, V _{GS} = 0 V		0.75	1.2	V
Reverse Recovery Time	t _{rr}	I _F = 8 A, dI/dt = 100 A/μs		55	83	ns
Peak Reverse Recovery Current	I _{RM(REC)}			4.1	6.2	A
Reverse Recovery Charge	Q _{rr}				107	161

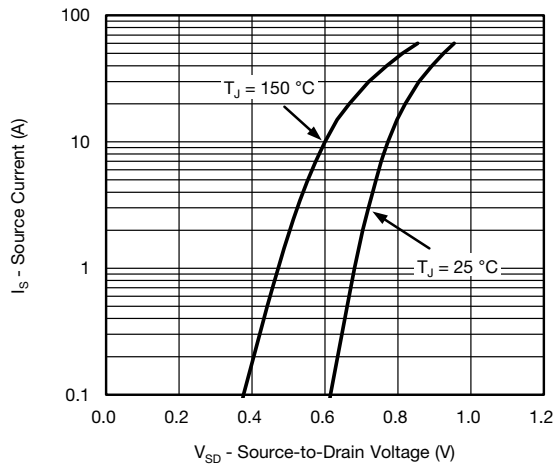
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

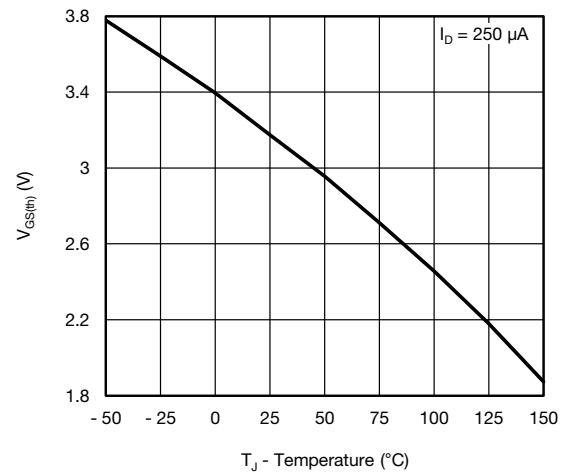
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

On-Resistance vs. Drain Current

Transfer Characteristics

On-Resistance vs. Gate-to-Source Voltage

Transconductance

Gate Charge

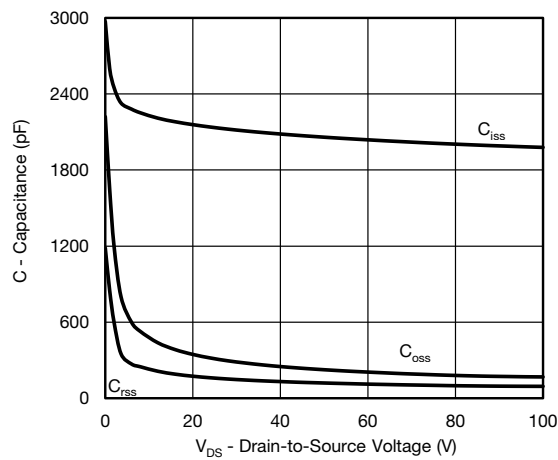
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



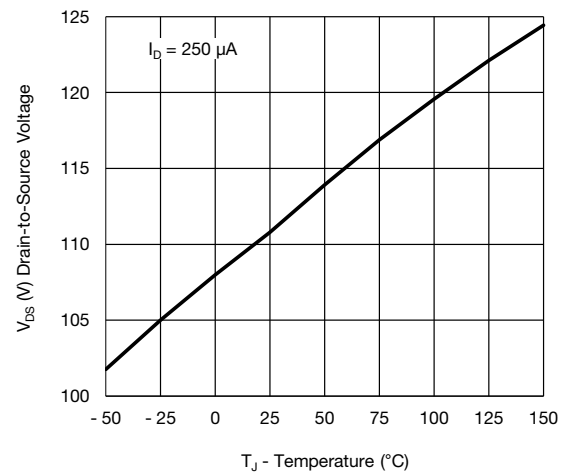
Source-Drain Diode Forward Voltage



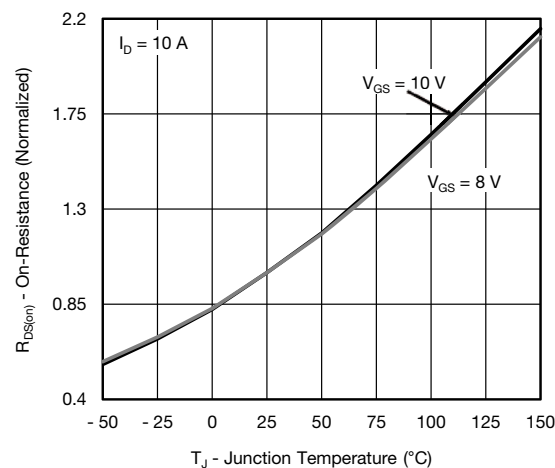
Threshold Voltage



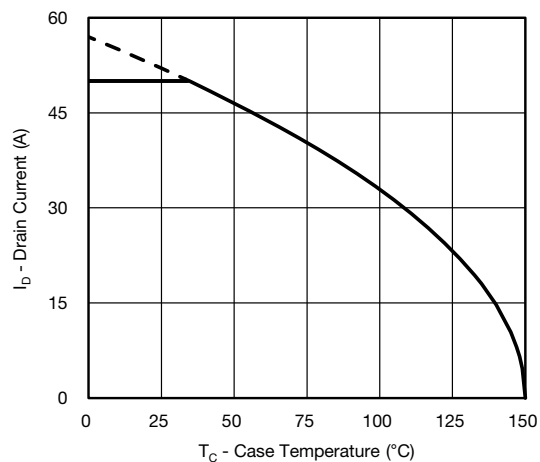
Capacitance



Drain Source Breakdown vs. Junction Temperature

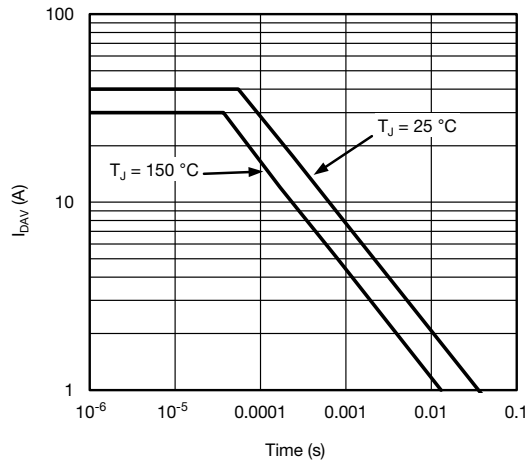


On-Resistance vs. Junction Temperature

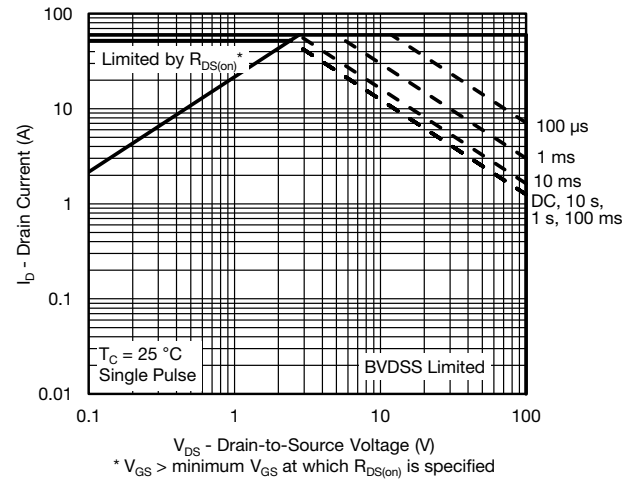


Current Derating

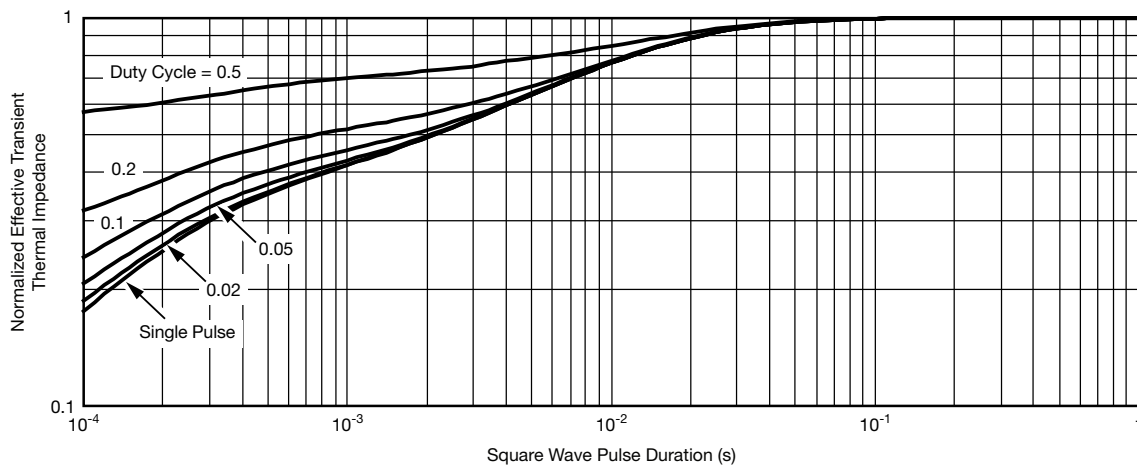
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area

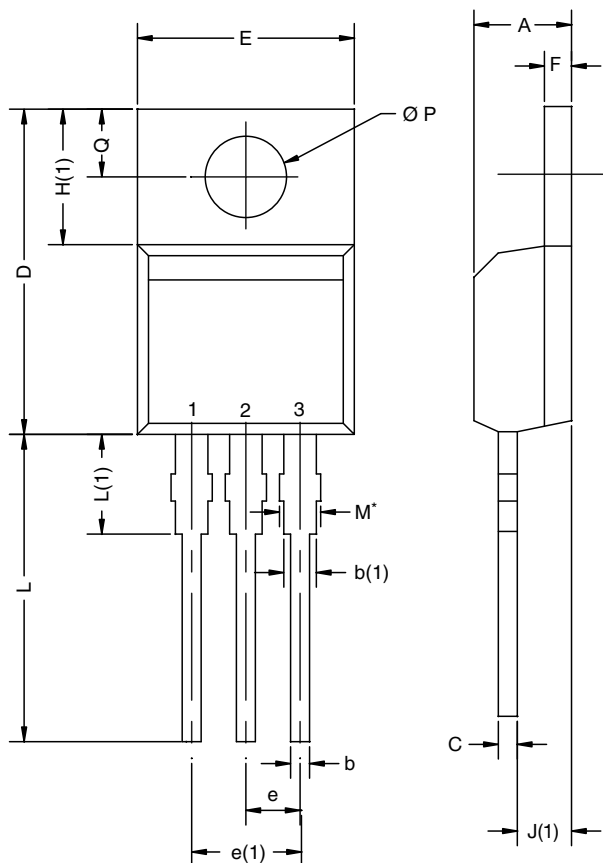


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62781.



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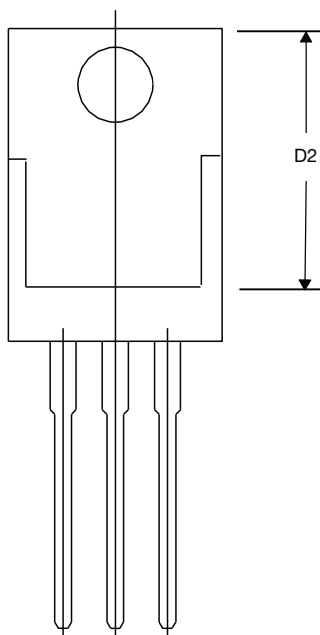


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T14-0413-Rev. P, 16-Jun-14
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM





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