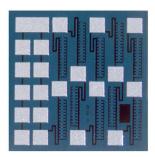




Wire Bondable Thin Film Multi-Tap Resistor Arrays



Product may not be to scale

The MTT multi-tap resistors offer nineteen taps allowing the user to select specified increments and a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTT's are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

FEATURES

- · Wire bondable
- · Selectable values by wire bonding
- Resistance range: 1.1 kΩ to 275 kΩ
- Chip size: 0.038" x 0.038"
- Case: 0404



(5-2008)

- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- · Ideally suited for hybrid prototyping
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

The MTT series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES			
PARAMETER	VALUE	UNIT	
Total Resistance Range	1.1K, 2.75K, 5.5K, 11K, 27.5K, 55K, 110K, 275K	Ω	
10 Resistors Between Pads 1 and 11 10 Resistors Between Pads 11 and 21	Each 9.1 % of total resistance Each 0.91 % of total resistance		
Standard Tolerances	± 1, ± 5, ± 10, ± 20 of total resistance of all 20 resistors	%	
TCR	± 250	ppm/°C	

Example:

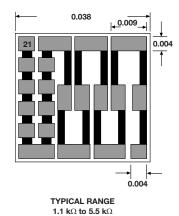
When the total resistance value is 55 k Ω , the resistors between pads 11 and 21 are 500 Ω each, and the resistors between pads 1 and 11 are 5 k Ω each.

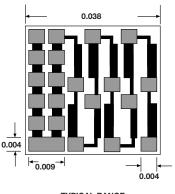
STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	VALUE	UNIT
TCR Tracking Between Elements	± 5	ppm/°C
Noise, MIL-STD-202, Method 308	-30 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	\pm 0.5 max. $\Delta R/R$	%
Stability, 1000 h, +125 °C, 125 mW	\pm 0.5 max. $\Delta R/R$	%
Operating Temperature Range	-55 to +125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	\pm 0.25 max. $\Delta R/R$	%
High Temperature Exposure ± 150 °C, 100 h	\pm 0.5 max. $\Delta R/R$	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10 ¹² min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at +70 °C (Derated to Zero at +175 °C)	0.250, total <i>R</i>	W
5x Rated Power Short-Time Overload, +25 °C, 5 s	± 0.25 max. Δ <i>R/R</i>	%





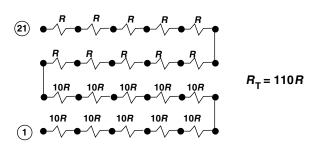
DIMENSIONS in inches



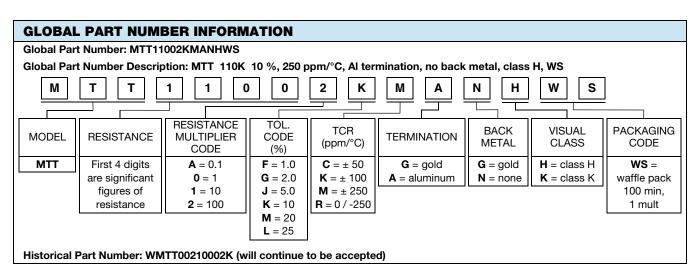


TYPICAL RANGE

SCHEMATIC



MECHANICAL SPECIFICATIONS		
PARAMETER		
Chip Size	0.038" x 0.038" ± 0.002" (0.965 mm x 0.965 mm ± 0.05 mm)	
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)	
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO2	
Resistor Material	Tantalum nitride, self-passivating	
Bonding Pads	0.004" x 0.004" (0.10 mm x 0.10 mm)	
Number of Pads	21	
Pad Material	10 kÅ minimum aluminum	
Backing	None, lapped semiconductor silicon	





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