STW40N95K5



N-channel 950 V, 0.110 Ω typ., 38 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

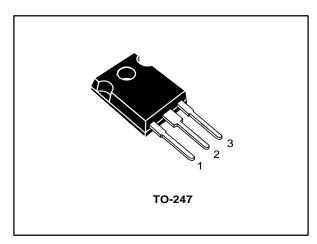
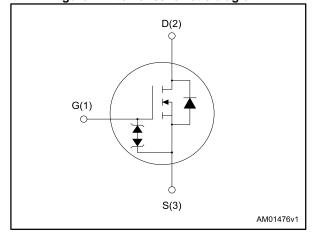


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	ΙD	Ртот
STW40N95K5	950 V	0.130 Ω	38 A	450 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

• Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STW40N95K5	40N95K5	TO-247	Tube

Contents STW40N95K5

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STW40N95K5 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25 °C	38	Α
I _D	Drain current (continuous) at T _C = 100 °C	24	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	152	Α
Ртот	Total dissipation at T _C = 25 °C		W
I _{AR}	Max current during repetitive or single pulse avalanche	13	Α
Eas	Single pulse avalanche energy (starting T _J = 25 °C, I _D = 13 A, V _{DD} = 50 V)		mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness 50		V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	0.28	°C/W
R _{thj-amb}	R _{thj-amb} Thermal resistance junction-amb max		°C/W

⁽¹⁾Pulse width limited by safe operating area.

 $^{^{(2)}}I_{SD} \leq$ 19 A, di/dt \leq 100 A/ μ s, VDS(peak) \leq V(BR)DSS.

 $^{^{(3)}}V_{DS} \le 760 \text{ V}$

Electrical characteristics STW40N95K5

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 1 mA	950			٧
	Zara gata valtaga drain	V _{GS} = 0, V _{DS} = 950 V			1	μΑ
IDSS	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 950 V, T _C =125 °C			50	μΑ
Igss	Gate-body leakage current	$V_{DS}=0, V_{GS}=\pm 20 \text{ V}$			±10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 19 A		0.110	0.130	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	3300	•	pF
Coss	Output capacitance	V _{GS} =0, V _{DS} =100 V, f=1 MHz	-	250	ı	pF
Crss	Reverse transfer capacitance	V33-0, V53-100 V, 1-1 WHZ	-	2	ı	pF
C _{o(tr)} (1)	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0$ to 760 V	-	398	ı	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related	V _{GS} = 0, V _{DS} = 0 to 760 V	-	142	1	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D =0	-	5	ı	Ω
Q_g	Total gate charge	$V_{DD} = 760 \text{ V}, I_D = 38 \text{ A}$	-	93	•	nC
Q _{gs}	Gate-source charge	V _{GS} =10 V	-	18.7	-	nC
Q _{gd}	Gate-drain charge	(see Figure 16: "Gate charge test circuit")	-	63.4	ı	nC

Notes

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Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 475 V, I _D = 19 A,	-	33.5	-	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	ı	51	1	ns
t _{d(off)}	Turn-off-delay time	(see Figure 15: "Switching times test circuit for resistive load")	- 1	91.5	ı	ns
t _f	Fall time		-	10	-	ns

 $^{^{(1)}}$ Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

 $^{^{(2)}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current		-		38	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		1		152	Α
V _{SD} (2)	Forward on voltage	I _{SD} = 38 A, V _{GS} = 0	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 38 A, di/dt = 100 A/µs	-	706		ns
Qrr	Reverse recovery charge	V _{DD} = 60 V (see Figure 18: " Unclamped inductive load test circuit")	-	22		μC
I _{RRM}	Reverse recovery current		-	62		Α
t _{rr}	Reverse recovery time	I _{SD} = 38 A, di/dt = 100 A/µs V _{DD} = 60 V T _J = 150 °C (see <i>Figure 18: " Unclamped</i>	-	886		ns
Qrr	Reverse recovery charge		-	28.2		μC
I _{RRM}	Reverse recovery current	inductive load test circuit")		64		А

Notes:

Table 8: Gate-source Zener diode

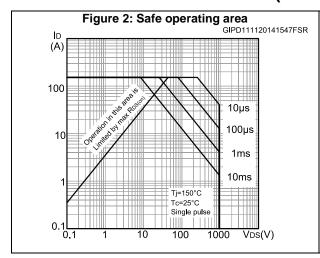
Symbol	Parameter	Test conditions	Min	Тур.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{mA}, I_{D}=0$	30	-	1	V

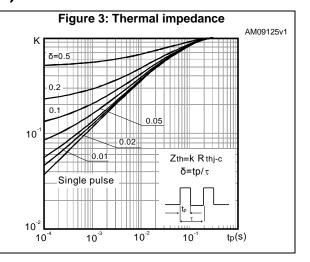
The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

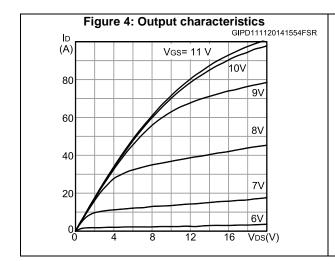
⁽¹⁾Pulse width limited by safe operating area.

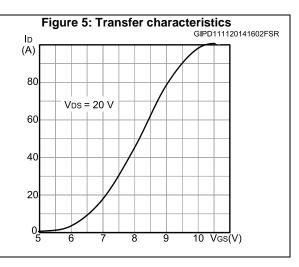
 $^{^{(2)}}$ Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

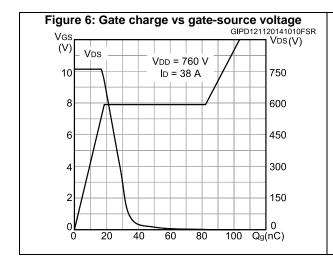
2.1 Electrical characteristics (curves)

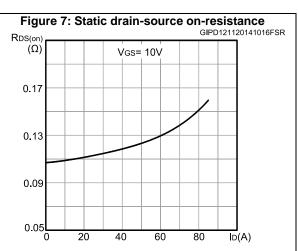












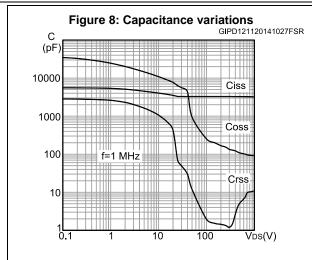
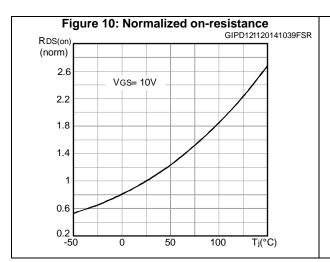
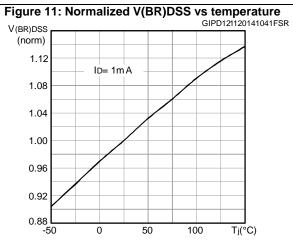
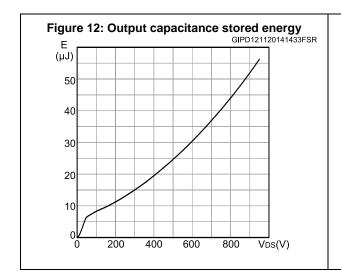
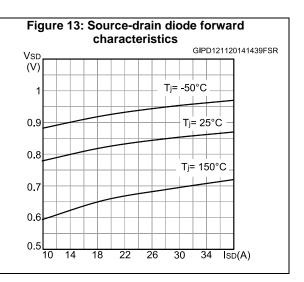


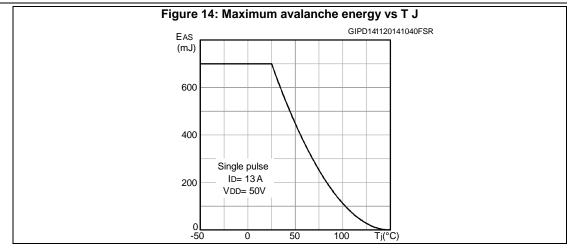
Figure 9: Normalized gate threshold voltage vs temperature GIPD121120141035FSR VGS(th) (norm) ID = 100 μA 1.2 1.0 0.8 0.6 0.4 0.2 -50 0 50 100 Tj(°C)





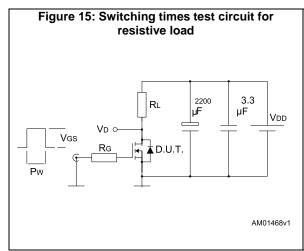






STW40N95K5 Test circuits

3 Test circuits



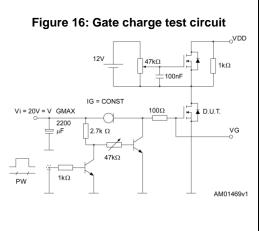
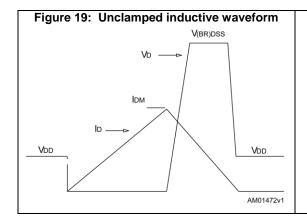


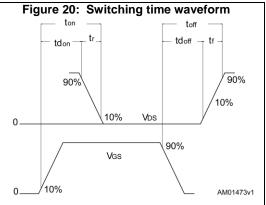
Figure 18: Unclamped inductive load test circuit

VD 0 2200 3.3 JF VDD

ND D.U.T.

AM01471v1





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-247 package information

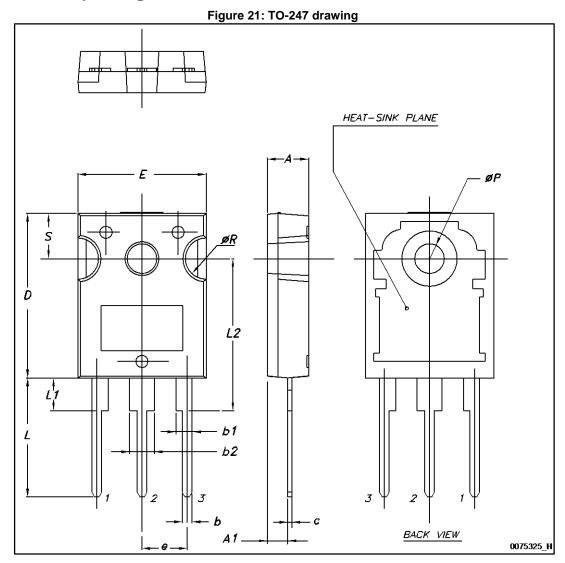


Table 9: TO-247 mechanical data

Dim	mm.				
Dim.	Min.	Тур.	Max.		
А	4.85		5.15		
A1	2.20		2.60		
b	1.0		1.40		
b1	2.0		2.40		
b2	3.0		3.40		
С	0.40		0.80		
D	19.85		20.15		
E	15.45		15.75		
е	5.30	5.45	5.60		
L	14.20		14.80		
L1	3.70		4.30		
L2		18.50			
ØP	3.55		3.65		
ØR	4.50		5.50		
S	5.30	5.50	5.70		



Revision history STW40N95K5

5 Revision history

Table 10: Document revision history

Date	Revision	Changes	
03-Jun-2014	1	First release.	
14-Nov-2014	2	Document status promoted from preliminary to production data. Added Section 2.1: "Electrical characteristics (curves)".	

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