## Multilayer Ceramic Chip Capacitors

# 1 of 3 Creation Date : April 05, 2017 (GMT)

# C1005JB1C104K050BA



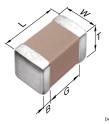






#### **TDK item description** C1005JB1C104KT\*\*\*\*

Applications	Commercial Grade	
Feature	General General (Up to 50V)	
Series	C1005 [EIA 0402]	
Status	Production (Not Recommended for New Design)	



	Size	
Length(L)	1.00mm ±0.05mm	
Width(W)	0.50mm ±0.05mm	
Thickness(T)	0.50mm ±0.05mm	
Terminal Width(B)	0.10mm Min.	
Terminal Spacing(G)	0.30mm Min.	
Recommended Land Pattern (PA)	0.30mm to 0.50mm	
Recommended Land Pattern (PB)	0.35mm to 0.45mm	
Recommended Land Pattern (PC)	0.40mm to 0.60mm	

Electrical Characteristics		
Capacitance	100nF ±10%	
Rated Voltage	16VDC	
Temperature Characteristic	JB(±10%)	
Dissipation Factor (Max.)	5%	
Insulation Resistance (Min.)	1000ΜΩ	

Other		
Soldering Method	Reflow	
AEC-Q200	No	
Packing	Punched (Paper)Taping [180mm Reel]	
Package Quantity	10000pcs	

<sup>!</sup> Images are for reference only and show exemplary products. ! This PDF document was created based on the data listed on the TDK Corporation website.

<sup>!</sup> All specifications are subject to change without notice.

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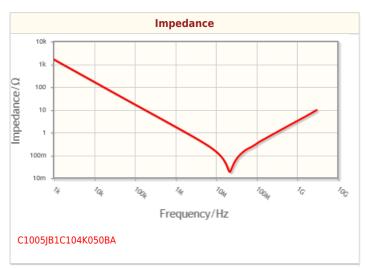


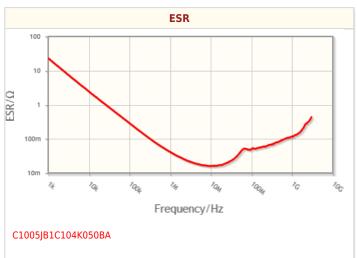


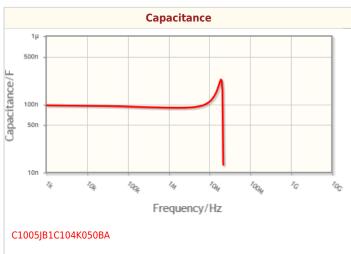


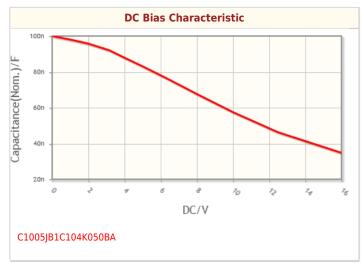


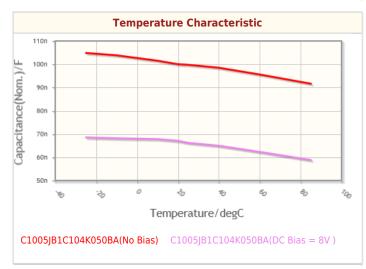
## Characteristic Graphs(This is reference data, and does not guarantee the products characteristics.)

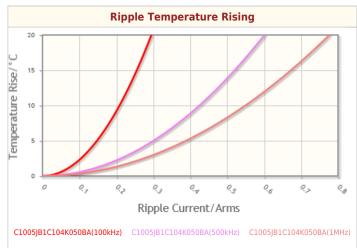












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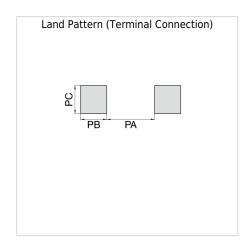








# **Associated Images**



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