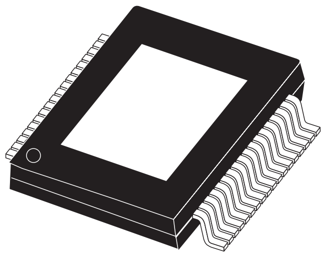
TDA7498MV

100 W mono BTL class-D audio amplifier

Datasheet - production data



PowerSSO-36
with exposed pad up

Features

- 100 W output power at THD = 10% with R_L = 6 Ω and V_{CC} = 36 V
- 80-W output power at THD = 10% with R_L = 8 Ω and V_{CC} = 34 V
- Wide-range single-supply operation (14 - 39 V)
- High efficiency (η = 90%)
- Four selectable, fixed gain settings of nominally 25.6 dB, 31.6 dB, 35.1 dB and 37.6 dB
- Differential inputs minimize common-mode noise
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable

Description

The TDA7498MV is a mono BTL class-D audio amplifier with single power supply designed for home systems and active speaker applications.

It comes in a 36-pin PowerSSO package with exposed pad up (EPU) to facilitate mounting a separate heatsink.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
Root part number 1TR	-40 to 85 °C	PowerSSO-36 (EPU)	Tape and reel

This is information on a product in full production. www.st.com

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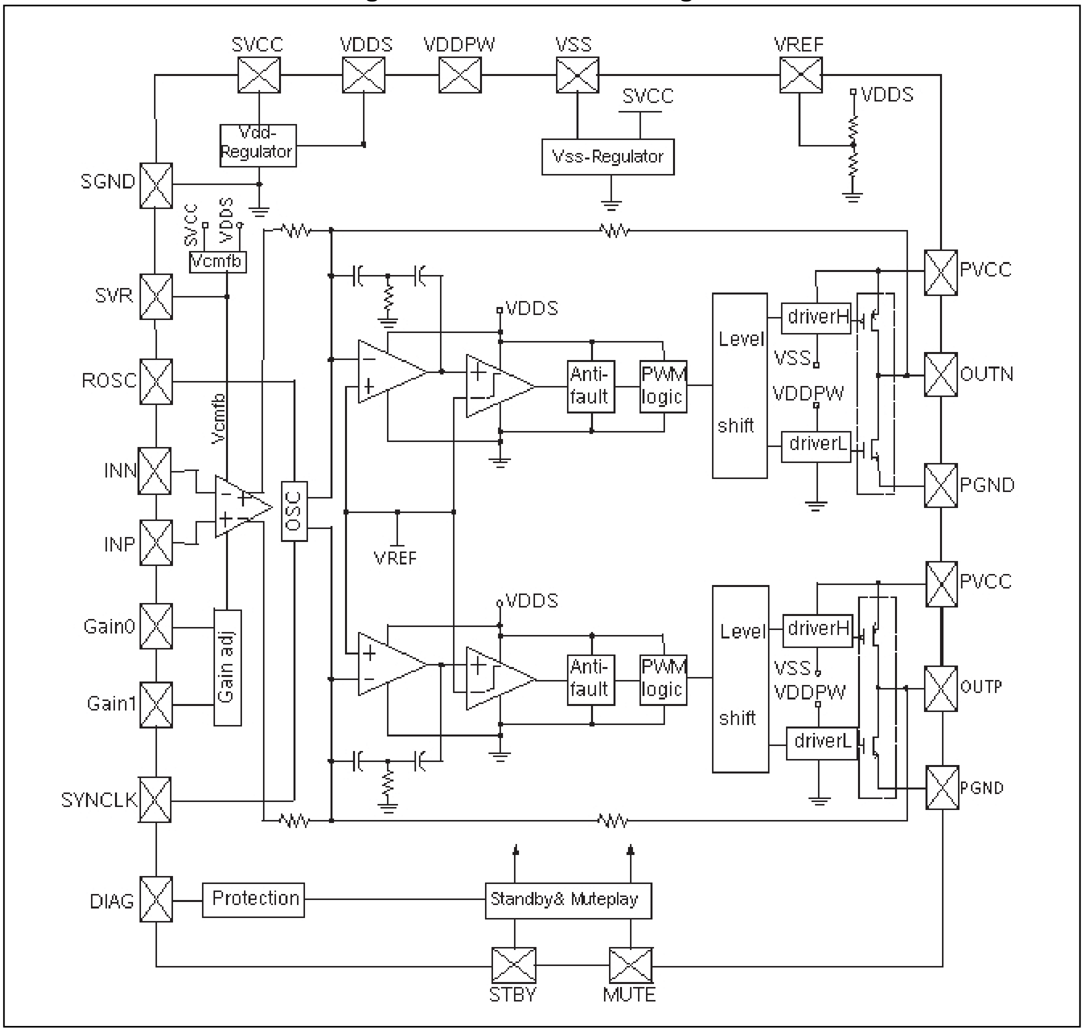
1 Device block diagram

Figure 1 shows the block diagram of the TDA7498MV.

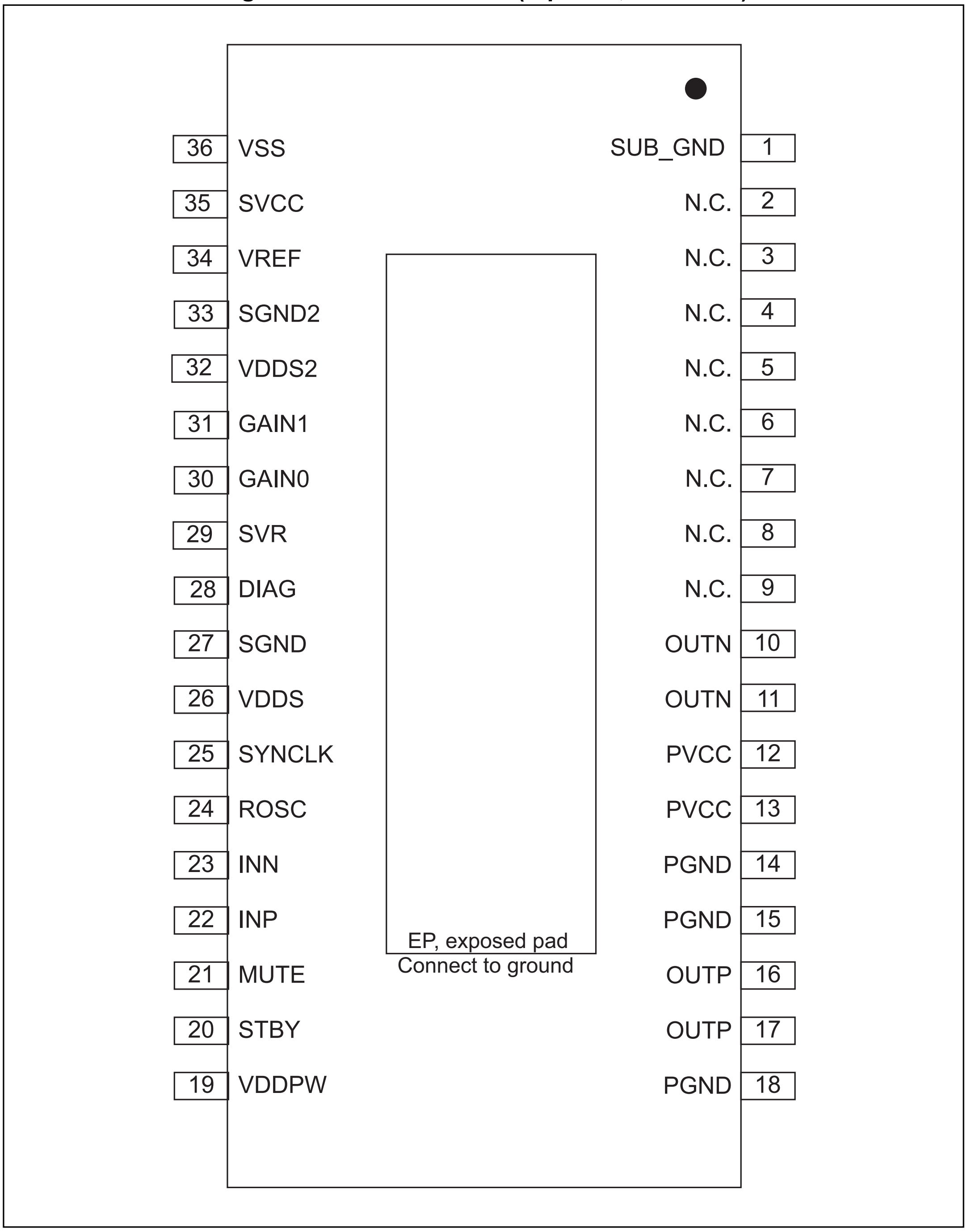
Figure 1. Internal block diagram



2 Pin description

2.1 Pinout

Figure 2. Pin connections (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

Pin n°	Name	Type	Description
1	SUB_GND	PWR	Connect to the frame
2,3	N.C.	-	No internal connection
4,5	N.C.	-	No internal connection
6,7	N.C.	-	No internal connection
8,9	N.C.	-	No internal connection
10,11	OUTN	O	Negative PWM output for audio channel
12,13	PVCC	PWR	Power supply for audio channel
14,15	PGND	PWR	Power stage ground
16,17	OUTP	O	Positive PWM output for audio channel
18	PGND	PWR	Power stage ground
19	VDDPW	O	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	I	Standby mode control
21	MUTE	I	Mute mode control
22	INP	I	Positive differential input
23	INN	I	Negative differential input
24	ROSC	O	Master oscillator frequency-setting pin
25	SYNCLK	I/O	Clock in/out for external oscillator
26	VDDS	O	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	PWR	Signal ground
28	DIAG	O	Open-drain diagnostic output
29	SVR	O	Supply voltage rejection
30	GAIN0	I	Gain setting input 1
31	GAIN1	I	Gain setting input 2
32	VDDS2	O	Connect to VDDS (pin 26)
33	SGND2	PWR	Connect to SGND (pin 27)
34	VREF	O	Half VDDS (nominal) referred to ground
35	SVCC	PWR	Signal power supply decoupling
36	VSS	O	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for heatsink, to be connected to ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC_MAX}	DC supply voltage for pins PVCCA, PVCCB	44	V
V_{L_MAX}	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN0, GAIN1	-0.3 to 3.6	V
T_{j_MAX}	Operating junction temperature	0 to 150	°C
T_{op_MAX}	Operating temperature	-40 to 85	°C
T_{stg}	Storage temperature	-40 to 150	°C

Warning: Stresses beyond those listed under "Absolute maximum ratings" make cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating condition" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supply with nominal value rated inside recommended operating conditions may experience some rising beyond the maximum operating condition for short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum rating is not exceeded.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case	-	2	3	°C/W

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB	14	-	39	V
T_{amb}	Ambient operating temperature	-20	-	85	°C

3.4 Electrical specifications

Unless otherwise stated, the results in *Table 6* below are given for the conditions: V_{CC} = 36 V, R_L (load) = 6 Ω, R_{OSC} = R3 = 39 kΩ, C8 = 100 nF, f = 1 kHz, G_V = 25.6 dB and T_{amb} = 25 °C.

Table 6. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_q	Total quiescent current	No LC filter, no load	-	40	60	mA
I_{qSTBY}	Quiescent current in standby	-	-	1	10	µA
V_{OS}	Output offset voltage	Play mode	-100	-	100	mV
		Mute mode	-60	-	60	
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	5.5	7	-	A
T_{jS}	Junction temperature at thermal shutdown	-	-	150	-	°C
R_i	Input resistance	Differential input	48	60	-	kΩ
V_{OVP}	Overvoltage protection threshold	-	42	43	-	V
V_{UVP}	Undervoltage protection threshold	-	-	-	8	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	100	-	W
		THD = 1%	-	78	-	
P_o	Output power	R_L = 8 Ω, THD = 10%, V_{CC} = 36V	-	80	-	W
P_D	Dissipated power	P_o = 100 W, THD = 10%	-	10	-	W
η	Efficiency	P_o = 100 W	-	90	-	%
THD	Total harmonic distortion	P_o = 1 W	-	0.1	-	%
G_V	Closed-loop gain	GAIN0 = L, GAIN1 = L	24.6	25.6	26.6	dB
		GAIN0 = L, GAIN1 = H	30.6	31.6	32.6	
		GAIN0 = H, GAIN1 = L	34.1	35.1	36.1	
		GAIN0 = H, GAIN1 = H	36.6	37.6	38.6	
ΔG_V	Gain matching	-	-1	-	1	dB
eN	Total input noise	A Curve, G_V = 20 dB	-	15	-	µV
		f = 22 Hz to 22 kHz	-	25	50	
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 0.5 Vpp, C_{SVR} = 10 µF	-	70	-	dB
T_r, T_f	Rise and fall times	-	-	50	-	ns
f_{SW}	Switching frequency	Internal oscillator	290	310	330	kHz

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SWR}	Output switching frequency range	With internal oscillator (1)	250	-	400	kHz
		With external oscillator (2)	250	-	400	
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
V_{STBY}	Pin STBY voltage high (H)	-	2.9	-	-	V
	Pin STBY voltage low (L)		-	-	0.5	
V_{MUTE}	Pin MUTE voltage high (H)	-	2.5	-	-	V
	Pin MUTE voltage low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	V_{MUTE} < 0.8 V	-	70	-	dB

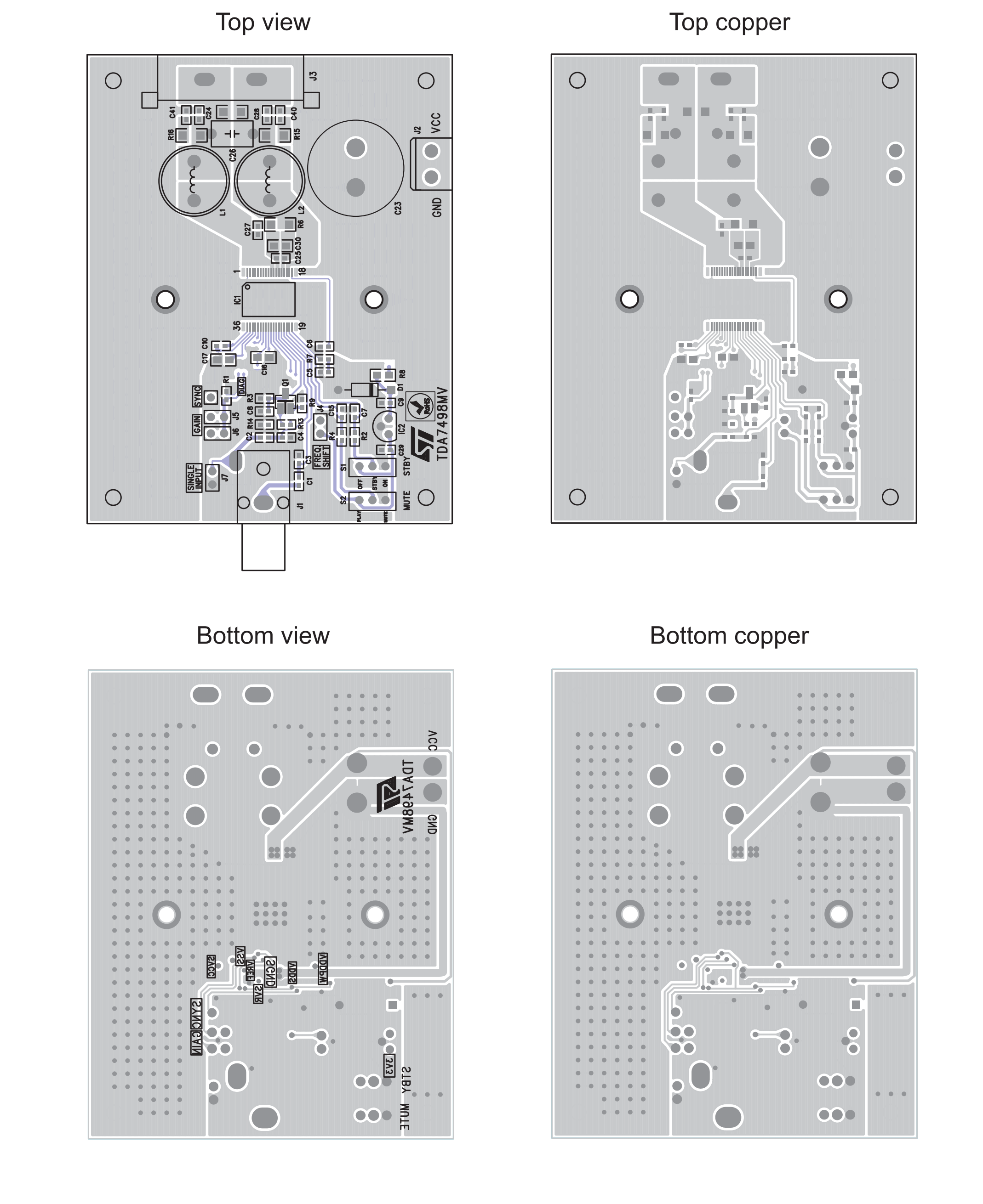
1. $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with R3 = 39 kΩ (see *Figure 18.*).
2. $f_{SW} = f_{SYNCLK} / 2$ with the external oscillator.

4 Characterization curves

Figure 18 on page 18 shows the test circuit with which the characterization curves, shown in the next sections, were measured. *Figure 3* shows the PCB layout.

4.1 Test board

Figure 3. Test board



4.2 Characterization curves

Unless otherwise stated, the measurements were made under the following conditions: V_{CC} = 36 V, f = 1 kHz, G_V = 25.6 dB, R_{OSC} = 39 kΩ, C_{OSC} = 100 nF, T_{amb} = 25 °C.

4.2.1 For R_L = 6 Ω

Figure 4. Output power (THD = 10%) vs. supply voltage

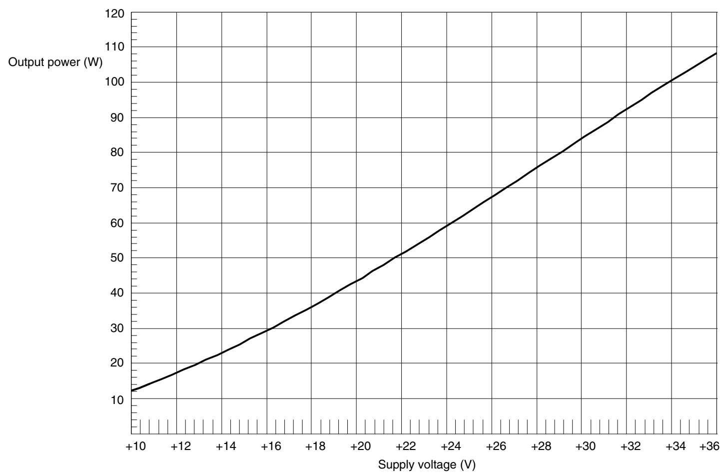


Figure 5. THD vs. output power

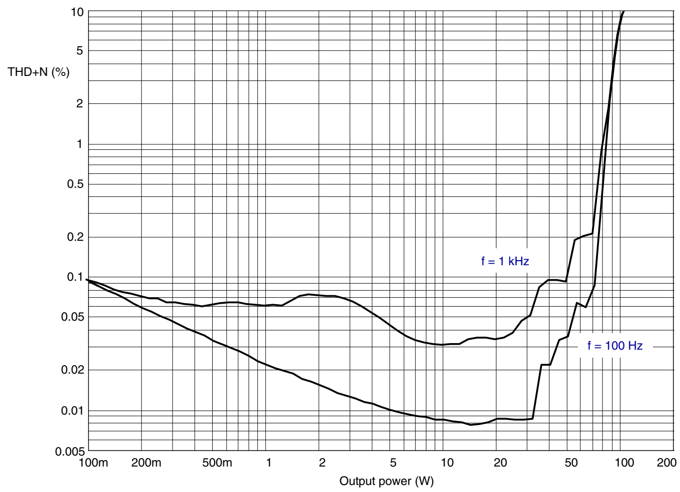


Figure 6. THD vs. frequency (1 W)

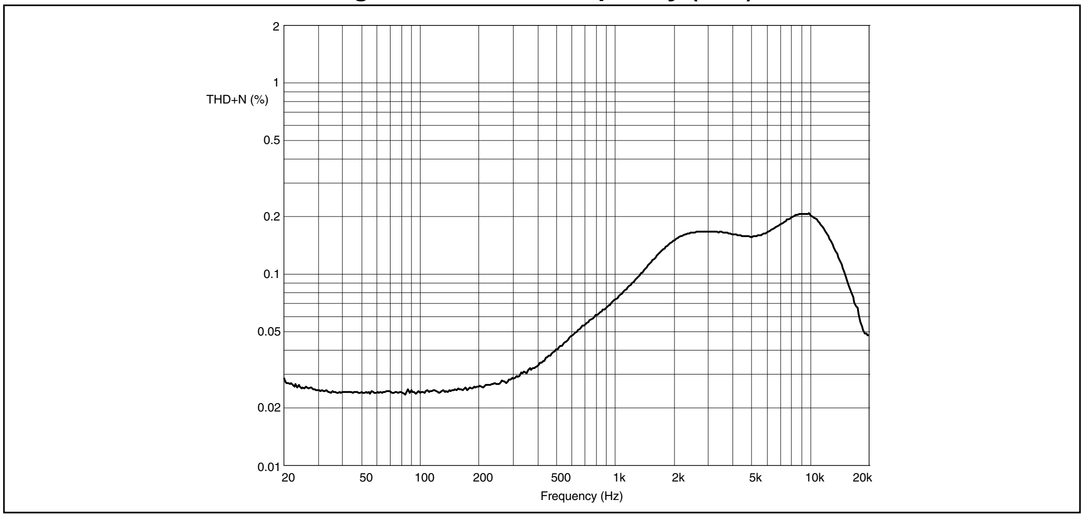


Figure 7. THD vs. frequency (100 mW)

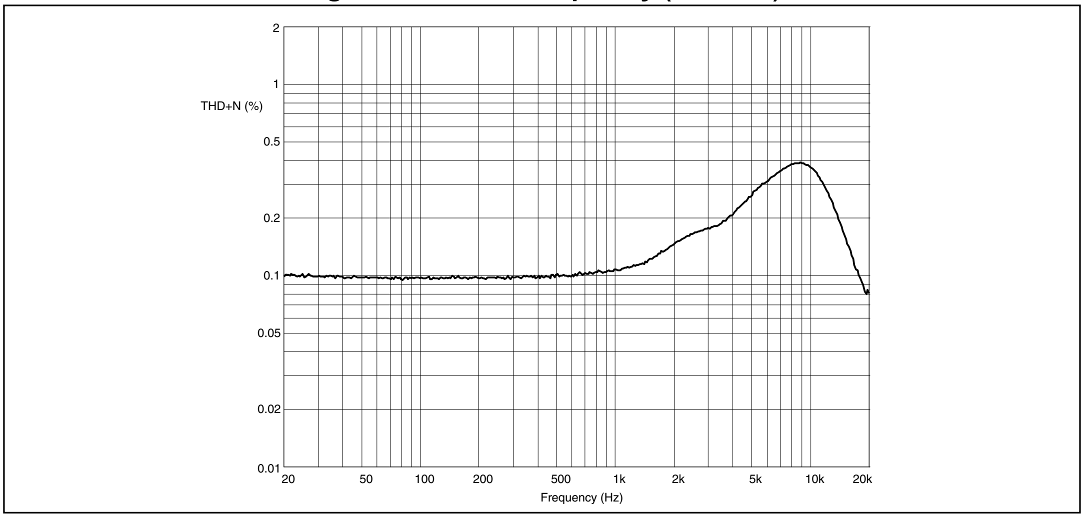


Figure 8. Frequency response

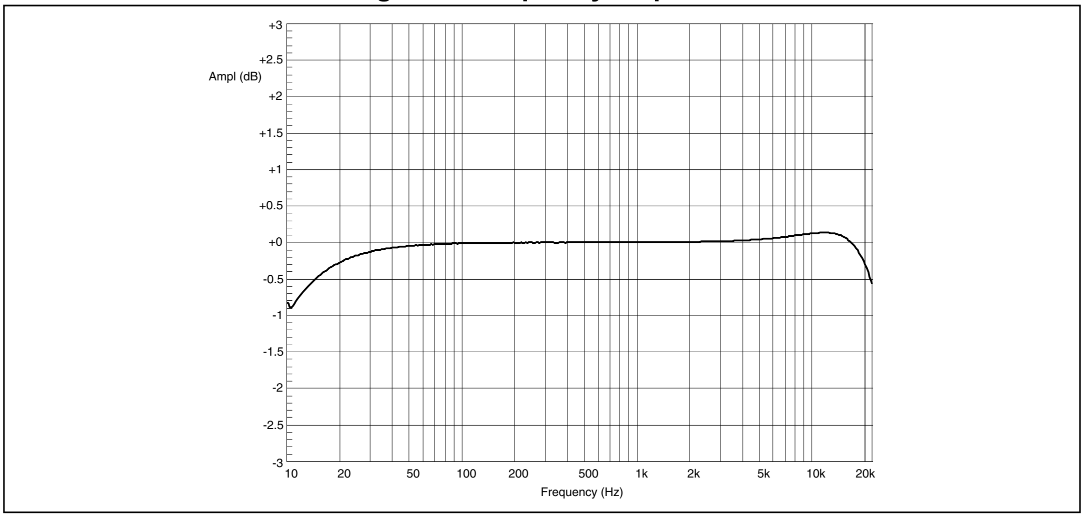


Figure 9. FFT performance (0 dBFS)

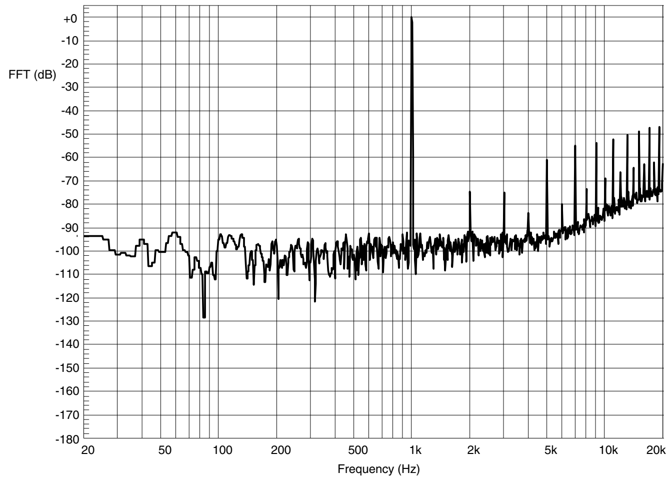
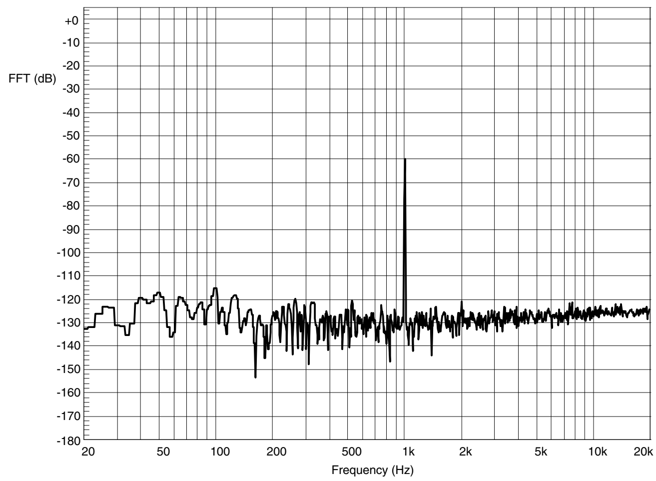


Figure 10. FFT performance (-60 dBFS)



4.2.2 For $R_L = 8\ \Omega$

Figure 11. Output power (THD = 10%) vs. supply voltage

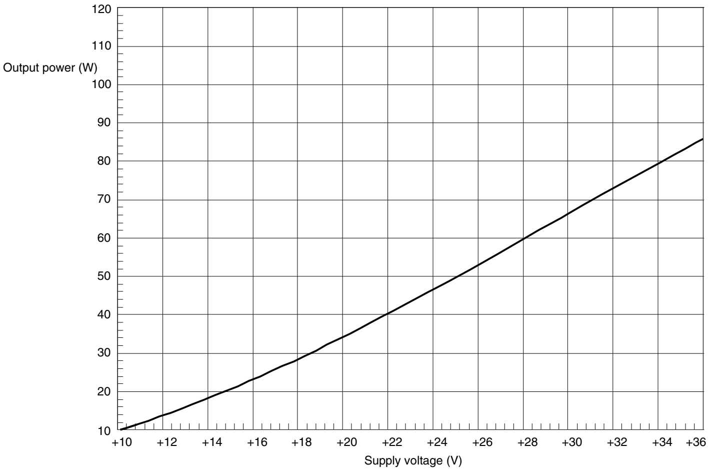


Figure 12. THD vs. output power

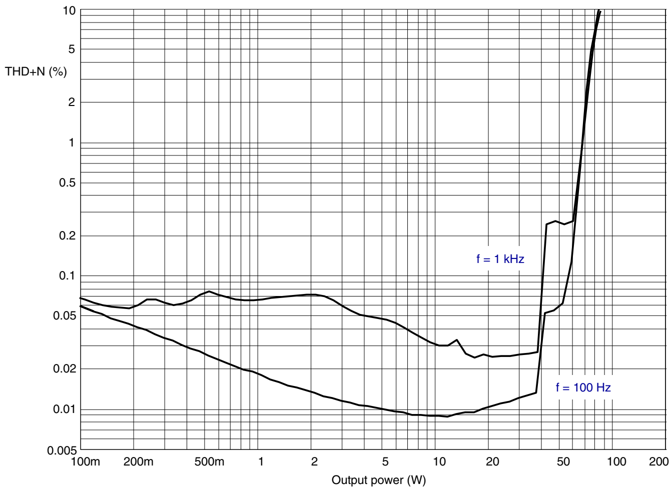


Figure 13. THD vs. frequency (1 W)

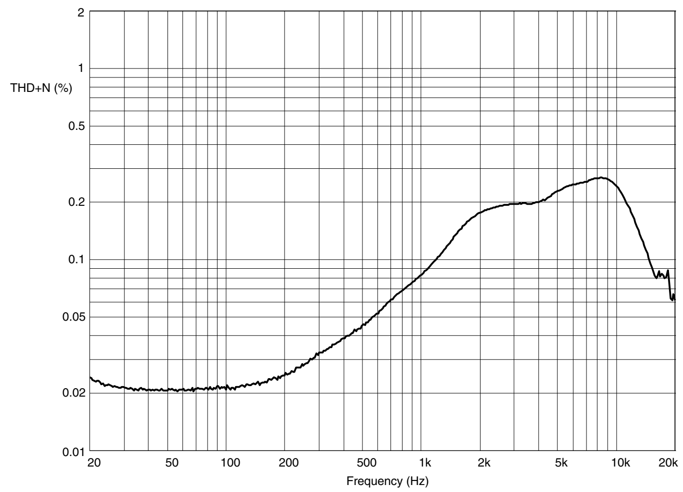


Figure 14. THD vs. frequency (100 mW)

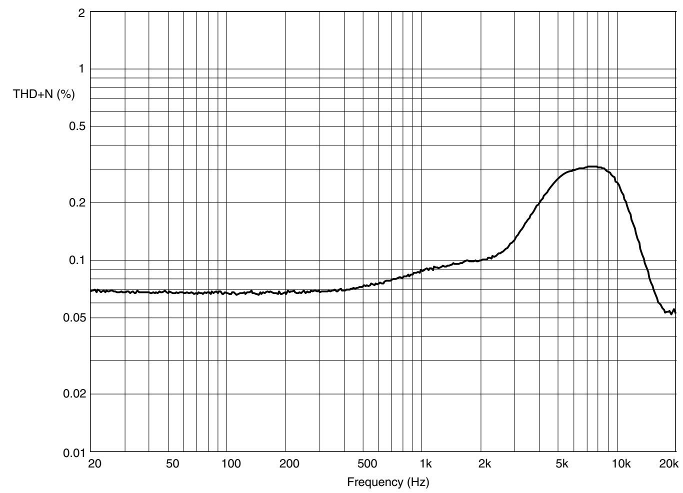


Figure 15. Frequency response

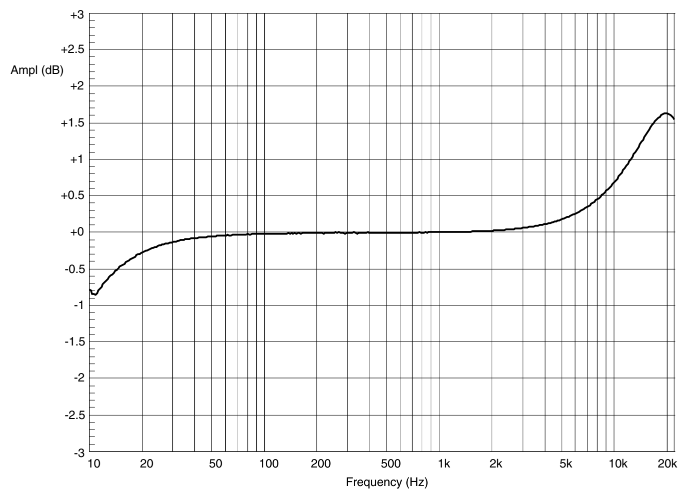


Figure 16. FFT performance (0 dB)

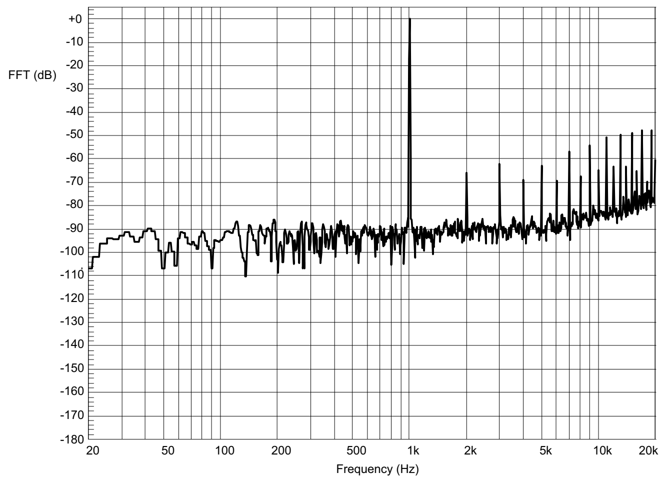
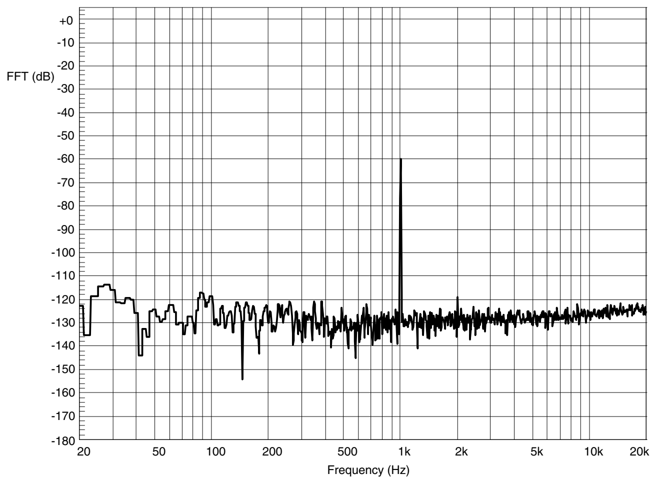


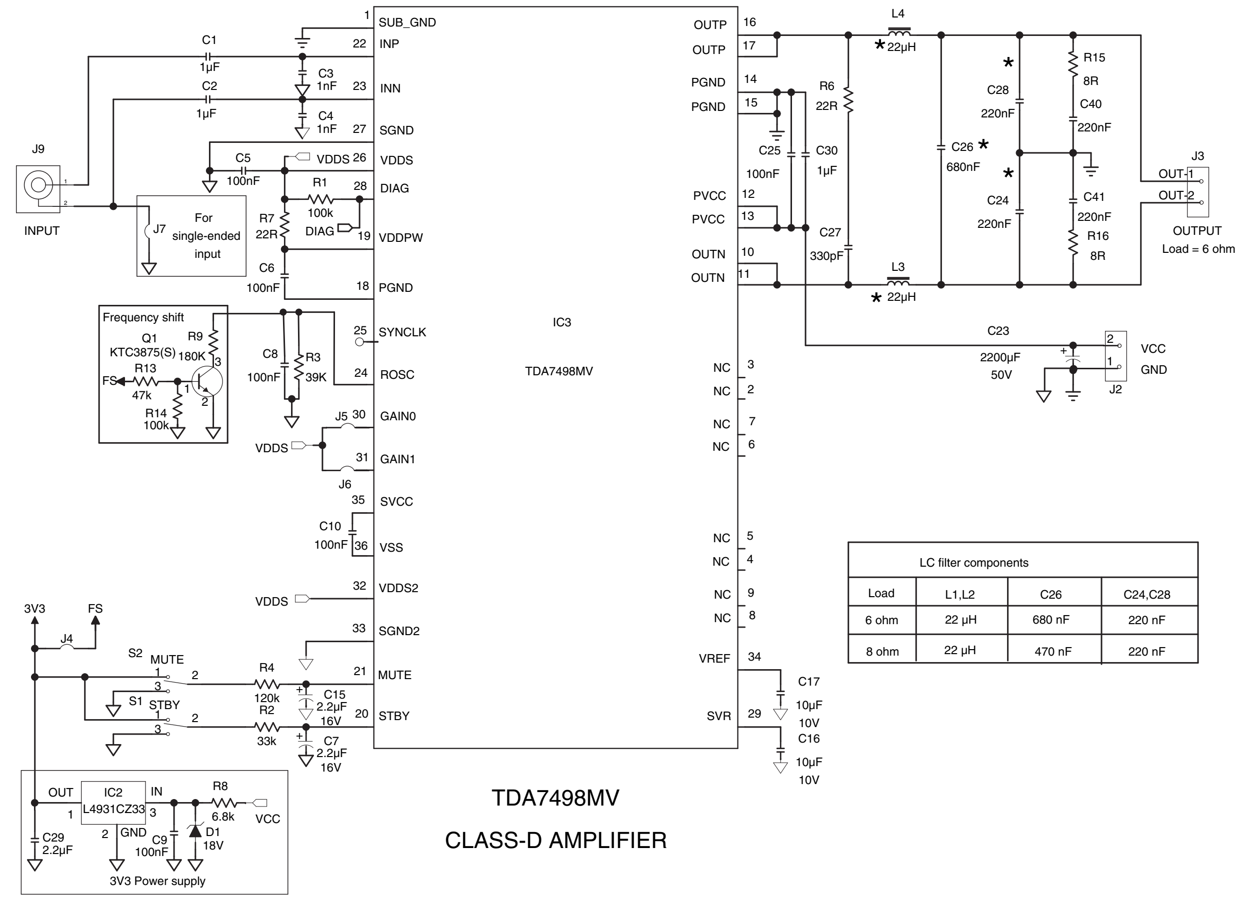
Figure 17. FFT performance (-60 dB)



5 Application information

5.1 Application circuit

Figure 18. Application circuit



LC filter components			
Load	L1,L2	C26	C24,C28
6 ohm	22 µH	680 nF	220 nF
8 ohm	22 µH	470 nF	220 nF

5.2 Mode selection

The three operating modes of the TDA7498MV are set by the two inputs, STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7498MV are realized by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 19*. The input current of the corresponding pins must be limited to 200 µA.

Table 7. Mode settings

Mode	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in *Table 6: Electrical specifications on page 9*

Figure 19. Standby and mute circuits

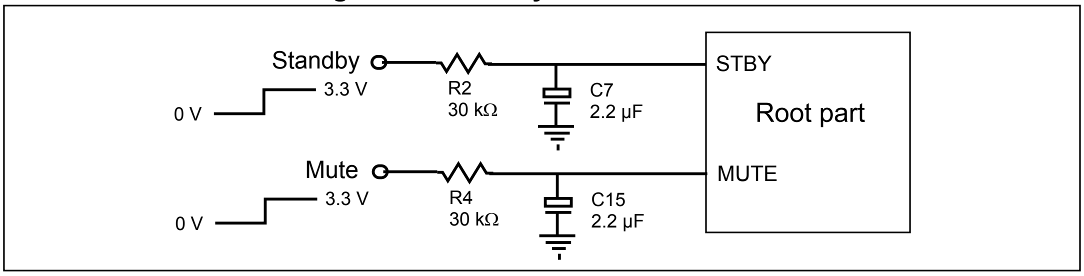
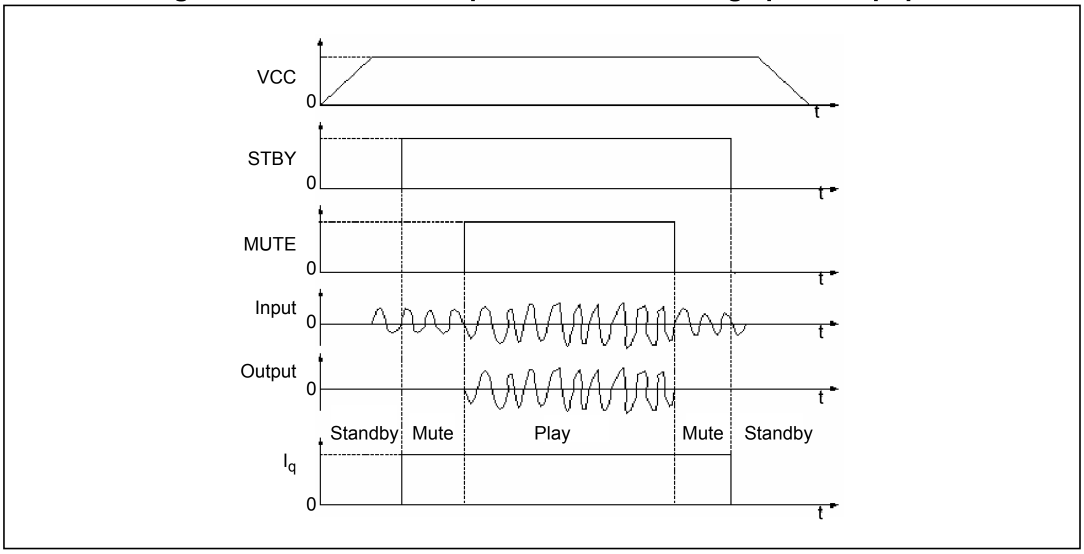


Figure 20. Turn-on/off sequence for minimizing speaker "pop"



5.3 Gain setting

The gain of the TDA7498MV is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 8. Gain settings

GAIN0	GAIN1	Nominal gain, G_V (dB)
L	L	25.6
L	H	31.6
H	L	35.6
H	H	37.6

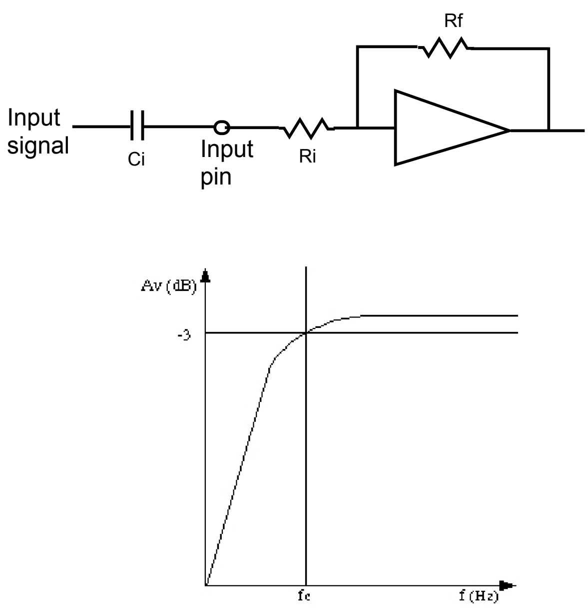
5.4 Input resistance and capacitance

The input impedance is set by an internal resistor Ri = 60 kΩ (typical). An input capacitor (Ci) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in *Figure 21*. For Ci = 470 nF the high-pass filter cut-off frequency is below 20 Hz:

$$f_C = 1 / (2 * \pi * Ri * Ci)$$

Figure 21. Input circuit and frequency response



5.5 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7498MV as master clock, while the other devices are in slave mode, that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

5.5.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW}, is controlled by the resistor, R_{OSC}, connected to pin ROSC:

$$f_{SW} = 10^6 / ((R_{OSC} * 16 + 182) * 4) \text{ kHz}$$

where R_{OSC} is in kΩ.

In master mode, pin SYNCLK is used as a clock output pin whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 kΩ as given below in *Table 9*.

5.5.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in *Table 9*.

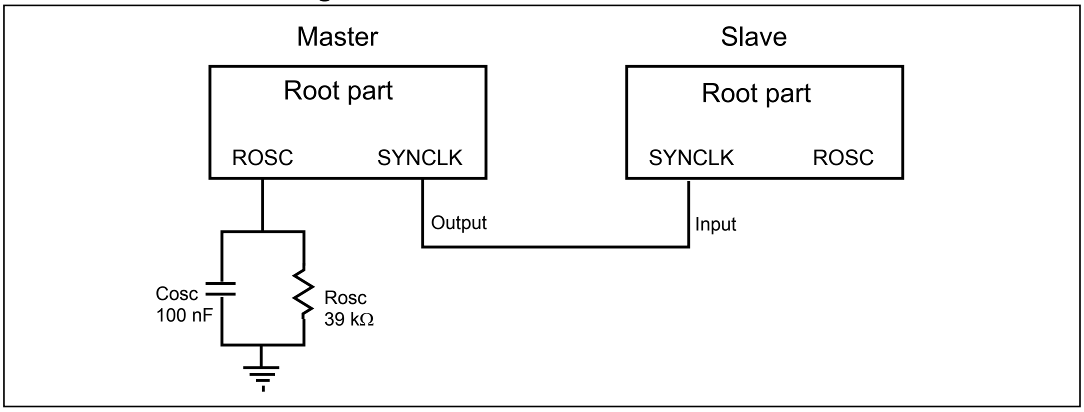
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 9. How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	R_{OSC} < 60 kΩ	Output
Slave	Floating (not connected)	Input

Figure 22. Master and slave connection



5.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cut-off frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L and C component values depending on the loudspeaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in *Figure 23* and *Figure 24* below.

Figure 23. Typical LC filter for an 8 Ω speaker

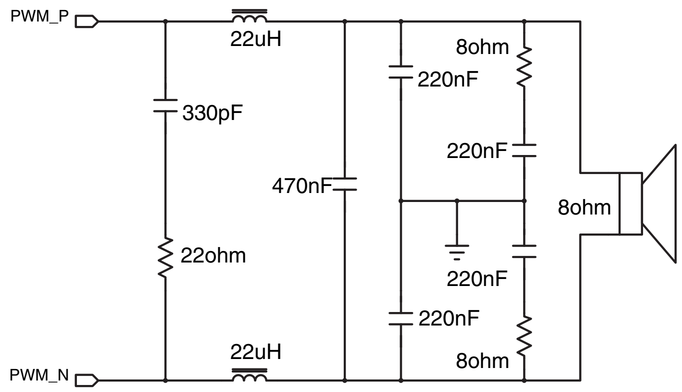
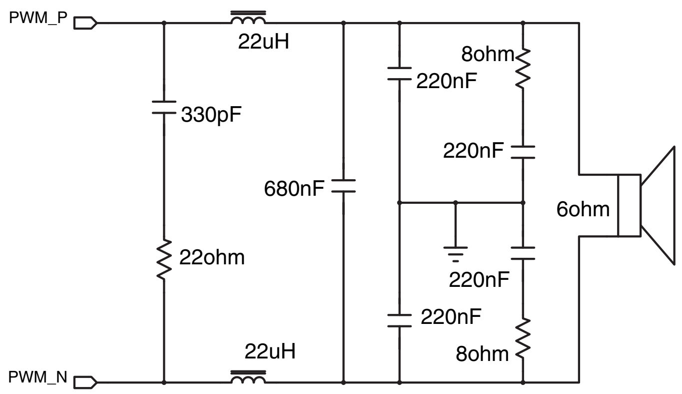


Figure 24. Typical LC filter for a 6 Ω speaker



5.7 Protection function

The TDA7498MV is fully protected against overvoltage, undervoltage, overcurrent and thermal overloads as explained here.

Overvoltage protection (OVP)

If the supply voltage exceeds the value for V_{OVP} given in *Table 6: Electrical specifications on page 9* the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage falls back to within the operating range the device restarts.

Undervoltage protection (UVP)

If the supply voltage drops below the value for V_{UVP} given in *Table 6: Electrical specifications on page 9* the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers to within the operating range the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value for I_{OCP} given in *Table 6: Electrical specifications on page 9* the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, T_{OC}, is determined by the R-C components connected to pin STBY.

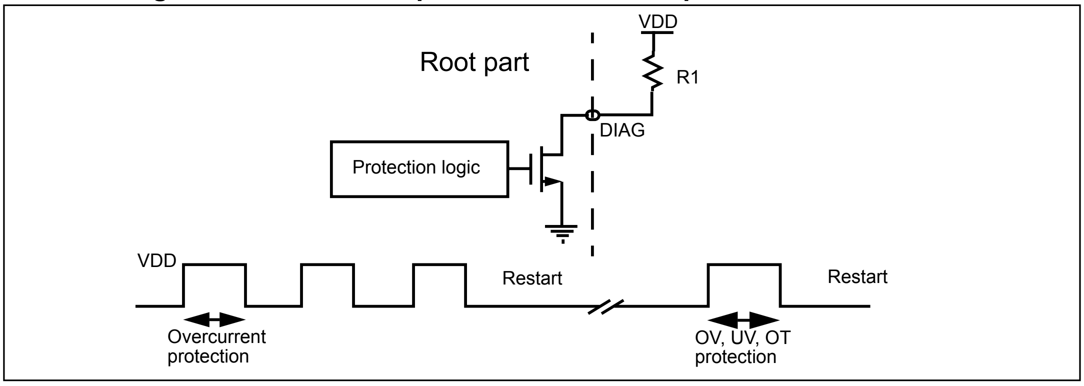
Thermal protection (OTP)

If the junction temperature, T_j, reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for T_j given in *Table 6: Electrical specifications on page 9* the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently the device restarts.

5.8 Diagnostic output

The output pin DIAG is an open drain transistor. When any protection is activated it switches to the high-impedance state. The pin can be connected to a power supply (< 39 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 µA) of the pin.

Figure 25. Behavior of pin DIAG for various protection conditions



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

The TDA7498MV comes in a 36-pin PowerSSO package with exposed pad up (EPU).

Figure 26 shows the package outline and *Table 10* gives the dimensions.

Figure 26. PowerSSO-36 EPU outline drawing

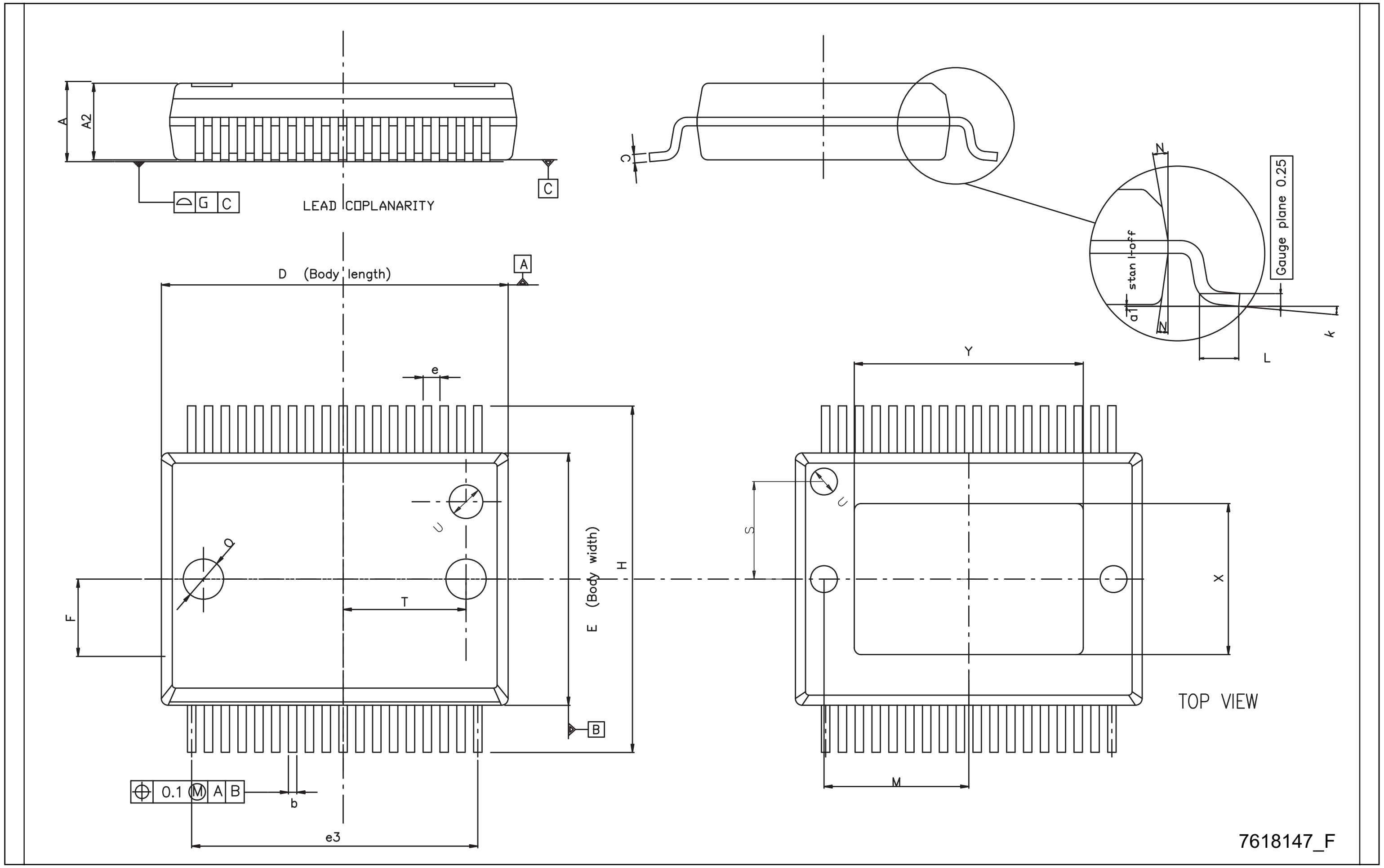


Table 10. PowerSSO-36 exposed pad up dimensions

Symbol	Dimensions in mm.			Dimensions in inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.15	-	2.45	0.085	-	0.096
A2	2.15	-	2.35	0.085	-	0.092
a1	0	-	0.1	0.00	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.4	-	7.6	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.1	-	-	0.004
H	10.1	-	10.5	-	-	0.413
h	-	-	0.4	-	-	0.016
k	0 deg	-	8 deg	0 deg	-	8 deg
L	0.55	-	0.85	0.022		0.033
M	-	4.3	-	-	0.169	-
N	-	-	10 deg	-	-	10 deg
O	-	1.2	-	-	0.047	-
Q	-	0.8	-	-	0.031	-
S	-	2.9	-	-	0.114	-
T	-	3.65	-	-	0.114	-
U	-	1.0	-	-	0.039	-

7 Revision history

Table 11. Document revision history

Date	Revision	Changes
30-Nov-2009	1	Initial release.
28-Jul-2010	2	Removed datasheet preliminary status, updated features list and updated device summary table *on page 1* Added operating temperature range to *Table 3 on page 8* Updated minimum supply voltage and temperature range in *Table 5: Recommended operating conditions on page 8* Updated voltage for logical 1 on pin STBY in *Table 6 on page 9*
27-Jan-2011	3	Updated applications circuit in *Figure 18 on page 18*.
24-Feb-2014	4	Updated order code *Table 1 on page 1*
19-Sep-2014	5	Updated *Figure 2: Pin connections (top view, PCB view)* Updated package information (representation on page 1, *Figure 26*, *Table 10*)