MP5455

Peak Power Assist for Smart/AI-Enabled Speakers and Low-Power Applications

The Future of Analog IC Technology

DESCRIPTION

The MP5455 is intelligently designed as a power storage system, releasing energy as needed during peak loading events, providing an efficient solution for smart speakers. It is also capable of providing back-up power in the event of a power failure targeting solid state drive supplications.

The internal input current limit block with dV/dt control prevents inrush current during system start-up. The storage capacitors charge while sufficient power load is applied. At peak loading, energy is released to maintain adequate power levels and prevent fluctuating performance. MPS's patented power back-up control circuit minimizes the storage capacitor requirement. This control circuit pumps the input voltage to a higher storage voltage and releases the energy over a hold-up time to the system in the case of an input outage. Storage and release voltages are both programmable for different system requirements.

The MP5455 requires a minimal number of readily available, standard, external components and is available in a QFN-20 (3mmx4mm) package.

FEATURES

- Power Back-Up Management Circuit
- Input Current Limiter with Integrated 60mΩ MOSFET
- Wide 2.7V to 7V Operating Input Range
- Up to 4.5A Input Current Limit
- Reverse-Current Protection
- Adjustable dV/dt Slew Rate for Bus Voltage Start-Up
- Over-Temperature Protection (OTP)
- Available in a QFN-20 (3mmx4mm) Package

APPLICATIONS

- Peak Power Smoother for Smart Speakers
- Artificial Intelligence (AI)-Enabled Speakers
- Power Back-Up
- Battery Hold-Up Supplies

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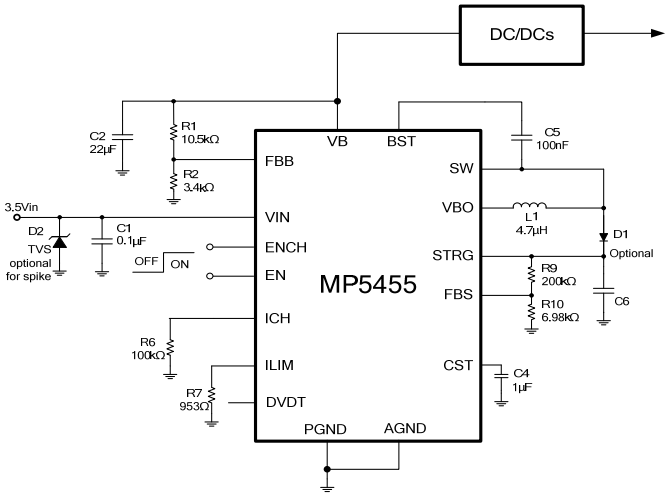
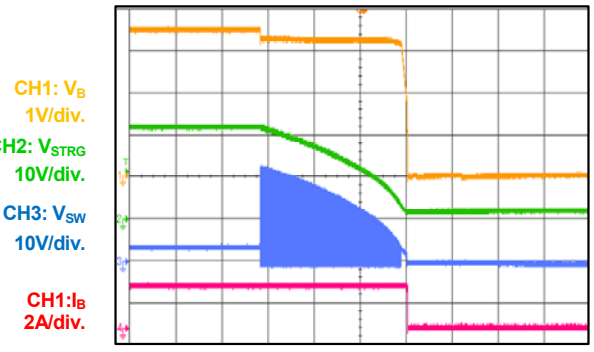
TYPICAL APPLICATION



Storage Release

VB Load = 2A, C_{STRG} = 220µFx2



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5455GL	QFN-20 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5455GL–Z)

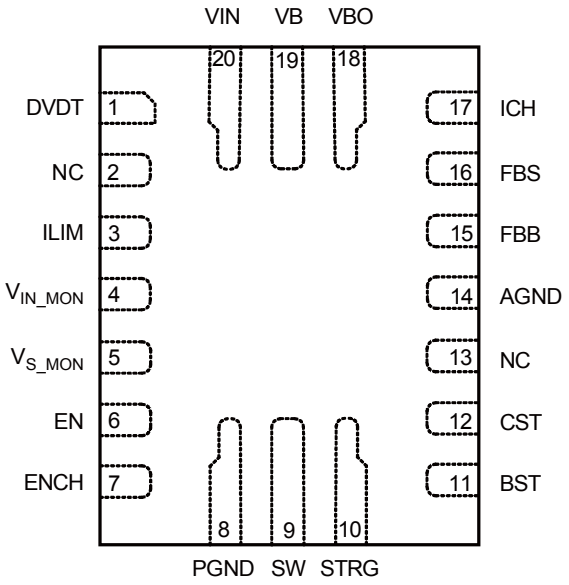
TOP MARKING

MPYW
5455
LLL

MP: MPS prefix
Y: Year code
W: Week code
5455: Digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-20 (3mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 8.0V
V_{STRG} .....-0.3V to 35V
V_{SW} .....-0.3V to V_{STRG} + 0.3V
V_{BST} .....-0.3V to V_{STRG} + 6.5V
V_{CST} .....-0.3V to 40V
All other pins .....-0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) **(2)** 2.6W
Junction temperature .....150°C
Lead temperature .....260°C
Operating temperature..... -40°C to +85°C

Recommended Operating Conditions (3)

Supply voltage (VIN) .....2.7V to 7V
Bus voltage (V_B) .....2.7V to 6V
Storage voltage (V_{STRG})..... VIN to 30V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
QFN-20 (3mmx4mm)	48	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, which is 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN = 5.0V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input supply voltage range	V_{IN}		2.7		7	V
Supply current (shutdown)	I_S	V_{EN} = 0V			2	μA
Supply current (quiescent)	I_Q	$V_{EN/ENCH}$ = 2V, $V_{FBB/FBS}$ = 1V			2	mA
Thermal shutdown (5)	T_{SD}			150		°C
Thermal shutdown hysteresis (5)	T_{HYS}			30		°C
VIN under-voltage lockout threshold rising	$INUV_R$			2.5	2.7	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$		0.3	0.4	0.5	V
EN/ENCH UVLO threshold rising	EN_R				1.2	V
EN/ENCH UVLO threshold falling	EN_F		0.4			V
Current limit MOSFET on resistance	R_{DSON}			60	65	mΩ
Continuous current limit	I_{LIM}	R_{ILIM} = 1.07kΩ		4.6		A
		R_{ILIM} = 1.2kΩ		4.1		
		R_{ILIM} = 1.4kΩ	-10%	3.7	10%	
Off-state leakage current	I_{LEAK}	VIN = 6V, VB = 0V or VB = 6V, VIN = 0V			2	μA
Rise time (dV/dt)	τ_R	DVDT pin floating	0.5	0.9	1.5	ms
		$C_{dv/dt}$ = 10nF		10		
		$C_{dv/dt}$ = 100nF		100		
Pre-charge current	$I_{CH\ PRE}$			130		mA
Charge peak current in boost mode	I_{CH}	ICH pin floating		500		mA
		R_{ICH} = 100kΩ		400		
		R_{ICH} = 200kΩ		200		
Feedback voltage	V_{FBB}, V_{FBS}		0.77	0.79	0.81	V
Buck mode dumping current limit	I_{DUMP}			5		A
VB under-voltage lockout threshold rising (6)	$INUVB_R$		1.8	2.2	2.5	V
VB under-voltage lockout threshold hysteresis (6)	$INUVB_{HYS}$		0.15	0.25	0.35	V

NOTES:

5) Guaranteed by characterization, not tested in production.

6) VB UVLO is applied to energy storage and release circuitry.

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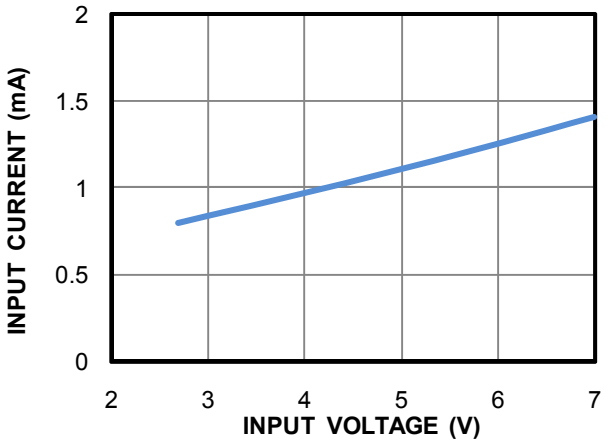
TYPICAL ELECTRICAL CHARACTERISTICS

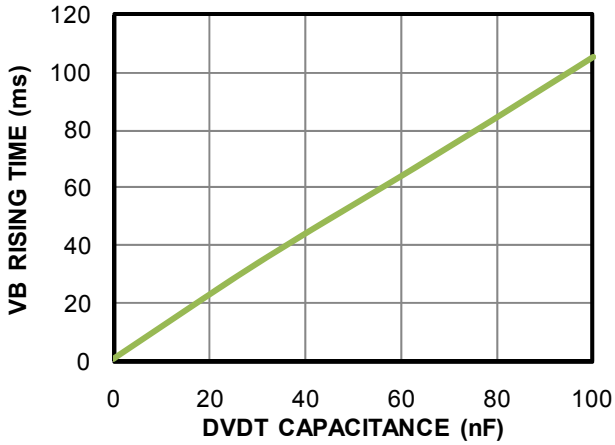
VIN = 5V, T_A = 25°C, unless otherwise noted.

Quiescent Current Vs. Input Voltage

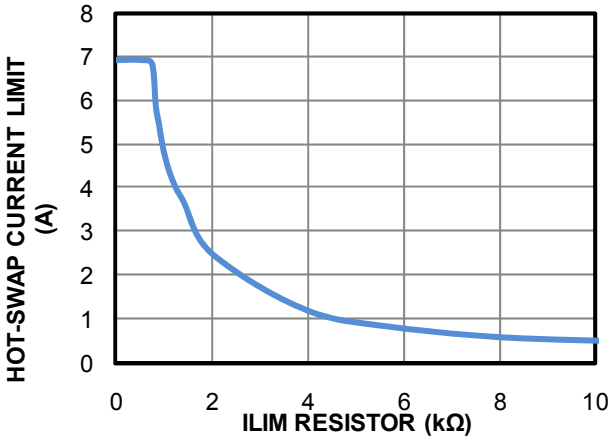
EN = ENCH = high, V_{FBB} = V_{FBS} = 1V



VB Rising Time vs. DVDT Capacitance

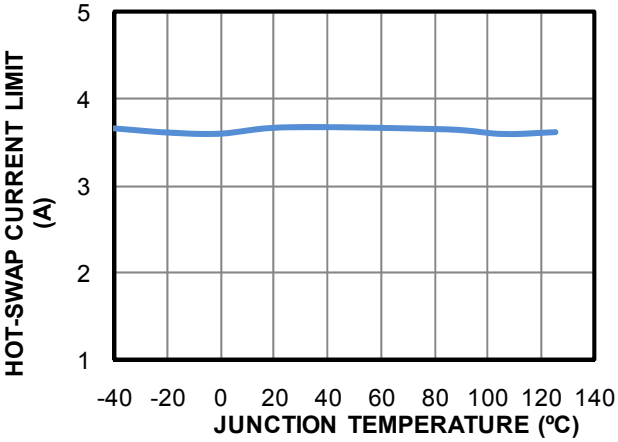


VIN to VB Current Limit vs. Limit Resistor

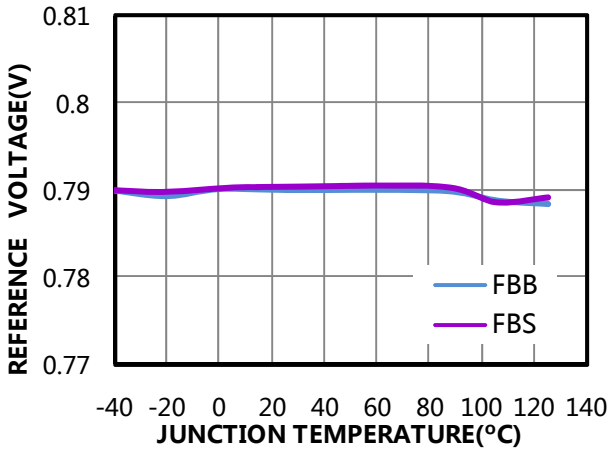


VIN to VB Current Limit vs. Temperature

R_{LIM} = 1.4kΩ



Reference Voltage vs. Temperature



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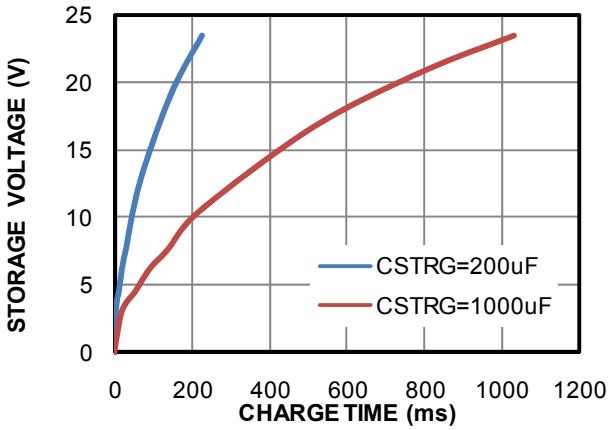
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

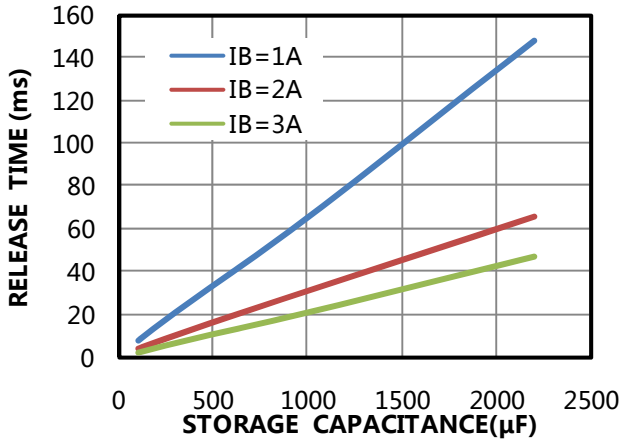
VIN = 3.5V, V_{STRG} = 23.5V, C_{STRG} = 100µFx2, $V_{RELEASE}$ = 3.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

Storage Voltage vs. Charging Time

R_{ICH} = 100kΩ

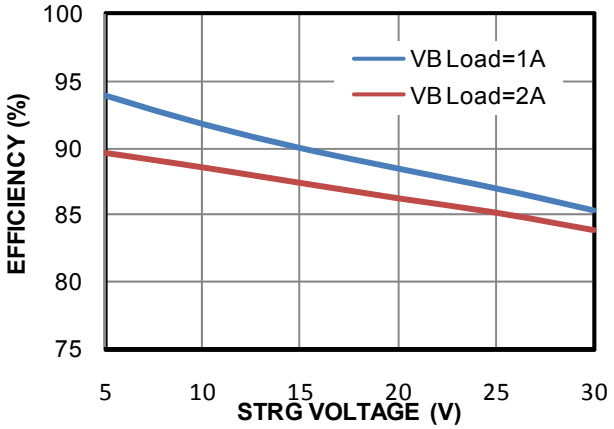


Release Time vs. Storage Capacitance



Release Efficiency

L = wurth_744311470



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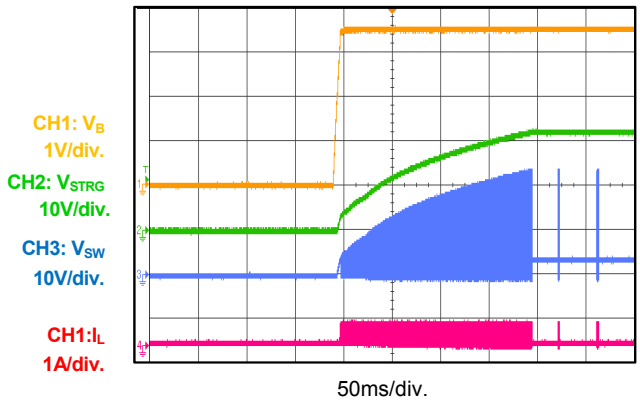
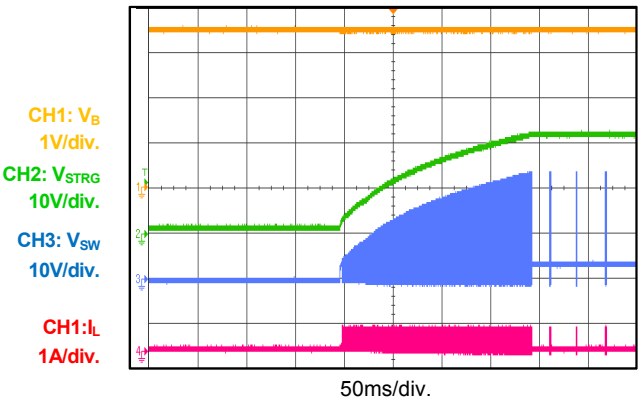
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.5V, V_{STRG} = 23.5V, C_{STRG} = 100µFx2, $V_{RELEASE}$ = 3.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

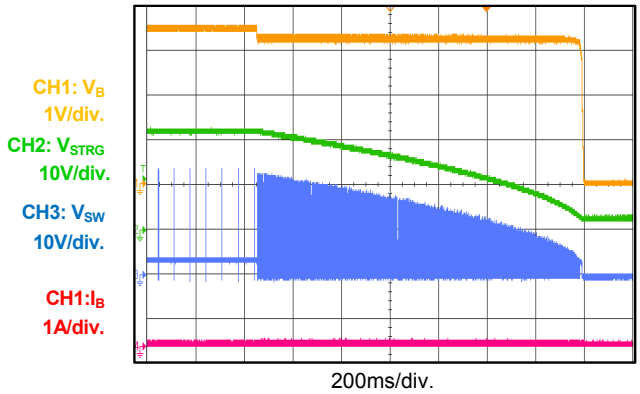
Input Power-On
VB Load = 1A



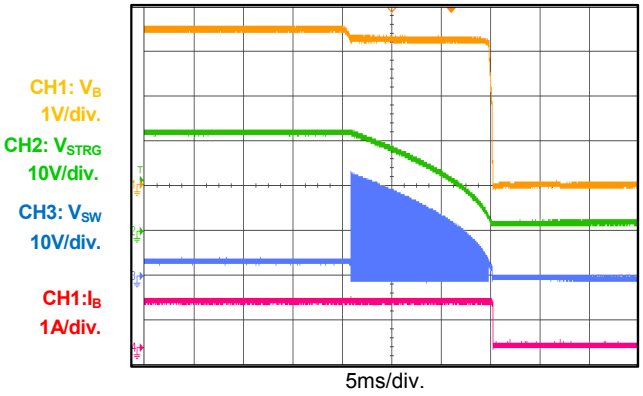
ENCH Turn-On
VB Load = 1A



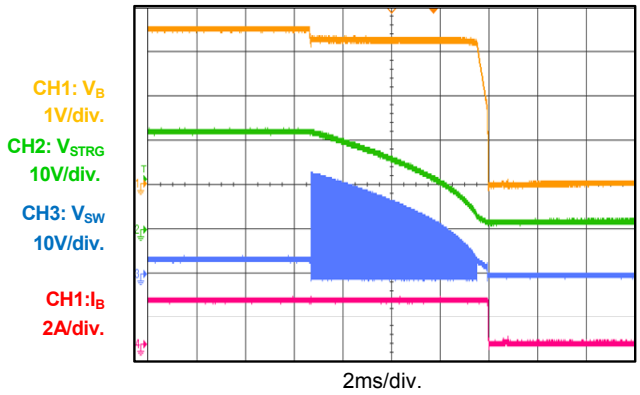
Storage Release
VB Load = 10mA, C_{STRG} = 100µFx2



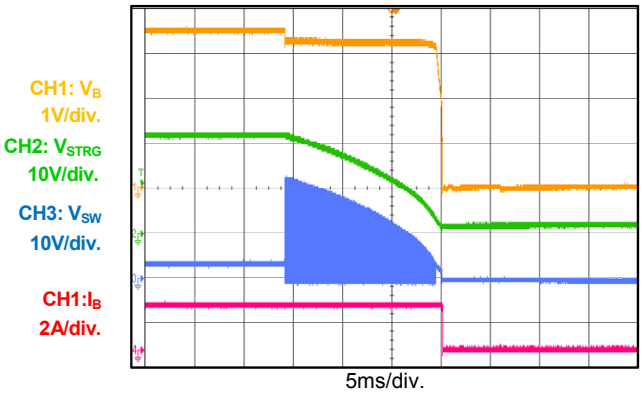
Storage Release
VB Load = 1A, C_{STRG} = 100µFx2



Storage Release
VB Load = 2A, C_{STRG} = 100µFx2



Storage Release
VB Load = 2A, C_{STRG} = 220µFx2



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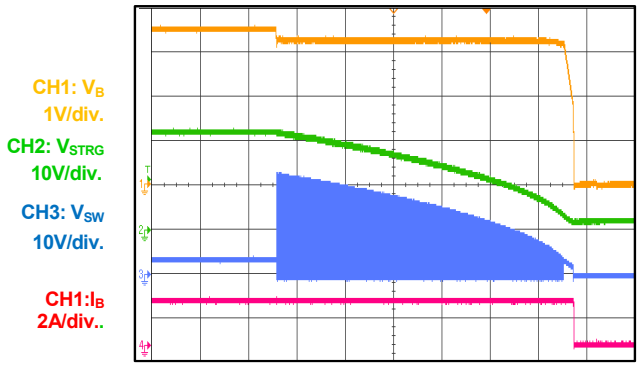
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.5V, V_{STRG} = 23.5V, C_{STRG} = 100µFx2, $V_{RELEASE}$ = 3.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

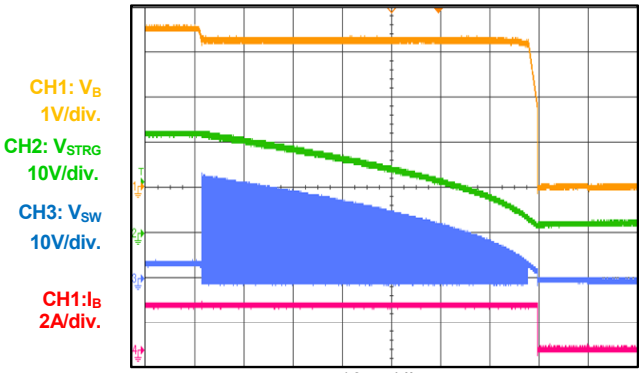
Storage Release

VB Load = 2A, C_{STRG} = 1000µF



Storage Release

VB Load = 2A, C_{STRG} = 2200µF



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PIN FUNCTIONS

Pin #	Name	Description
1	DVDT	**Slew rate control pin for VB during start-up.** Leave DVDT floating for the default soft-start time (around 0.9ms from 0V to 5V).
2	NC	**Factory use only.** Leave NC floating.
3	ILIM	**Input current limit setting.** Do not leave ILIM floating.
4	V_{IN_MON}	**Factory use only.** Leave V_{IN_MON} floating or pull V_{IN_MON} up to VB.
5	V_{S_MON}	**Factory use only.** Leave V_{S_MON} floating or pull V_{S_MON} up to VB.
6	EN	**On/off control pin for the MP5455.** When EN is pulled low, all functions of the MP5455 are disabled (for both the input current limiter and the charge/release circuitry). Ensure that the EN voltage is high during release.
7	ENCH	**On/off control pin for the charge/release circuitry.** When ENCH is pulled down, the release circuitry is disabled. Note that ENCH must be kept high to achieve energy release.
8	PGND	**Power ground.**
9	SW	**Switching node for the charge/release circuitry.** Connect a small inductor between SW and VBO.
10	STRG	**Storage voltage.** Connect the appropriate storage capacitors for the energy storage and release operation.
11	BST	**Bootstrap pin for the charge/release circuitry.** The internal bi-directional switcher requires a bootstrap capacitor (100nF) from BST to SW to supply the high-side switch driver voltage during release.
12	CST	**High-side switch driving voltage storage.** The MP5455 supports energy, even when the storage voltage is close to the VB-regulated voltage.
13	NC	**No connection.**
14	AGND	**IC signal ground.**
15	FBB	**Bus voltage feedback sense.** FBB sets the bus release voltage.
16	FBS	**Storage voltage feedback sense.** FBS sets the storage voltage.
17	ICH	**Boost mode current limit adjustment.** Do not pull ICH to VCC or an external voltage source.
18	VBO	**Internal boost.** VBO is the input voltage after passing through the input isolation MOSFET.
19	VB	**Internal bus voltage.** Place a 22μF to 47μF ceramic capacitor as close to VB as possible.
20	VIN	**Input supply voltage.** The MP5455 operates from an unregulated 2.7V to 7V input. Place a ceramic capacitor 0.1μF or larger as close to VIN as possible. A TVS diode at the input is necessary if the VIN spike is high. Refer to the Selecting the Input Capacitor and TVS section on page 12 for additional details.

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OPERATION

The MP5455 is an energy storage and management unit in a QFN-20 (3mmx4mm) package. The MP5455 provides a very compact and efficient energy management solution for applications requiring power back-up or hold-up supplies. MPS's patented lossless energy storage and release management circuits use a bidirectional buck/boost converter to achieve optimal energy transfer and provide the most cost-effective energy storage solution.

The integrated boost converter raises the energy-storage voltage level. The storage feedback resistor divider sets the storage voltage. If the input shuts down suddenly, the internal buck converter transfers the energy from the storage capacitor to the bus and holds the bus voltage when the system consumes energy from the storage capacitor. The buck converter can work in 100% duty cycle operation to deplete the stored energy completely.

Start-Up

When VIN starts up, the bus voltage (VB) is charged from 0 to VIN, approximately. The VB rising slew rate is controlled by the dV/dt capacitance. This function prevents input inrush current and provides protection to the entire system.

EHCH is used to enable the storage charge and release circuitry. If ENCH is already high before VB finishes the dV/dt process, the storage charge circuitry works automatically when VIN is higher than the under-voltage lockout (UVLO) threshold (typically 2.5V). The storage charge circuitry operates in two modes: pre-charge mode (where STRG is charged to VB using a current source) and boost mode (where STRG is charged to set the voltage). The pre-charge mode charges STRG up to VB using a near-constant current source (around 130mA). When STRG is close to VB and VB is higher than a certain threshold (where the corresponding FBB is higher than 0.813V), boost mode is initiated.

Boost mode charges STRG to the target voltage. Figure 1 shows the charging build-up process when ENCH is high before VB starts up.

It is strongly recommended to enable ENCH after VB has settled (see Figure 2). Since release mode is triggered when FBB is lower than 0.79V (although there is a 23mV hysteresis between boost mode and release mode), VB may be pulled back low and enter release mode accidently. To prevent this, enable ENCH after VB settles. In some high-current charges, boost mode can be programmed by ICH. Figure 2 shows the charging build-up process when ENCH is enabled after VB settles.

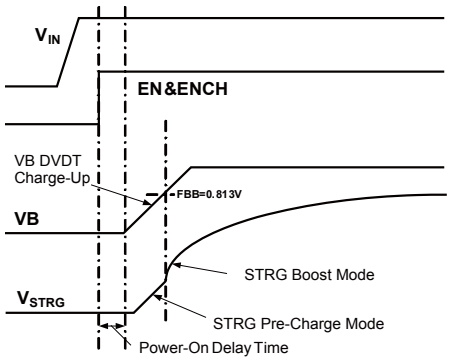

Figure 1: Charging Process

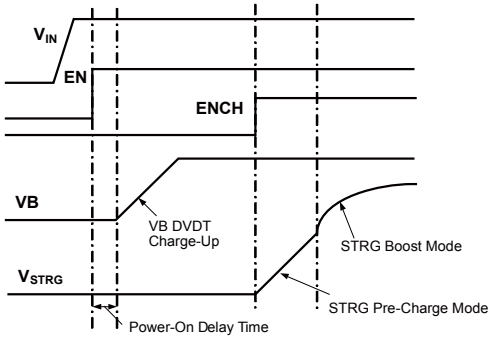

Figure 2: Charging Process when EN and ENCH Are Separated

Storage Voltage

After the start-up period, the internal boost converter regulates the storage voltage automatically to a set value. The MP5455 uses burst mode to minimize the converter's power loss. When the storage voltage drops below the set voltage, burst mode initiates and charges the storage capacitor. During the burst period, the current limit and the low-side MOSFET (LS-FET) control the switch. When the LS-FET turns on, the inductor current increases until it reaches its current limit. The boost-current limit can be programmed by an ICH resistor. By

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floating ICH, the boost current limit is set to around 500mA. After reaching the current limit, the LS-FET turns off for the set minimum off-time. At the end of this minimum off-time, if the feedback voltage remains below the 0.79V internal reference, the LS-FET turns on again. Otherwise, the MP5455 waits until the voltage drops below the threshold before turning on the LS-FET.

Release

The MP5455 monitors the input and bus voltages continuously. Once the bus voltage drops below the selected release voltage (such as when losing input power), the internal boost converter stops charging and works in buck-release mode. In buck mode, the MP5455 transfers energy from the high-voltage storage capacitor to the low-voltage bus capacitor. Determine the release voltage by selecting resistor values for the bus resistor divider.

The released buck applies fixed-frequency constant-on-time (COT) control and enables fast transition between the charge and release modes. The buck converter works at 100% duty cycle until the storage capacitor voltage approaches the bus voltage. Then the storage and bus voltages drop until they reach the DC/DC converter's UVLO threshold (see Figure 3).

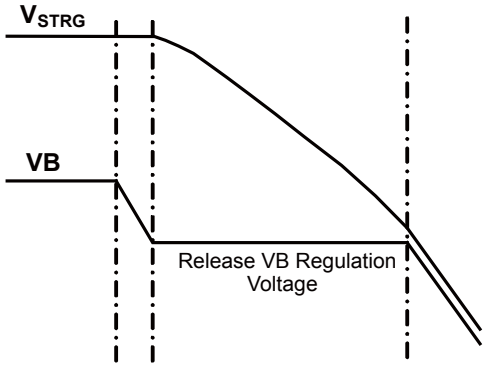

Figure 3: Release Times

Input Current Limit

The input current limiter controls the input inrush current of the internal hot-swap MOSFET carefully to prevent an inrush current from the input to the bus. A capacitor connected to DVDT sets the soft-start time. Despite the soft-start process, ILIM can limit the steady-state current.

Connect a resistor between ILIM and GND to set the current limit.

Reverse-Current Protection

The hot-swapping circuit uses reverse-current protection to prevent the storage energy from transferring back to the input when energy is released from the storage capacitors to bus. The hot-swap MOSFET turns on when the input voltage exceeds the VIN UVLO threshold during start-up or when input voltage is about 0.2V higher than VB. The hot-swap MOSFET turns off when input voltage falls below the bus voltage during release.

Start-Up Sequencing

Connect a capacitor across DVDT to program the soft-start time. During soft start, the energy storage capacitors charge. Very short dV/dt times can trigger the current-limit threshold. Select the DVDT capacitor based on the storage capacity.

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APPLICATION INFORMATION

Selecting Input Capacitor and TVS

Capacitors at VIN are recommended to absorb possible voltage spikes during input power turn-on, input switch hard-off (during power-off), or other special conditions. The application determines the capacitor. For example, if the input power trace is too long (with higher parasitic inductance) during the input switch hard-off period, more energy pumps into the input. This means more input capacitors are needed to ensure that the input voltage spike remains in a safe range. Use a capacitor 0.1μF or larger based on the spike condition.

Consider inrush current requirements when selecting an input capacitor. Typically, more input capacitors result in a higher input inrush current during hot-plugging. A smaller input capacitor is needed for a smaller inrush current. The MP5455 works normally with a very small input capacitor. However, this leads to a possible high voltage spike. An efficient solution is to add a TVS diode at the input to absorb the possible input voltage spike. At the same time, keep the inrush current small during hot-plugging. A typical TVS diode, like SMA6J5.0A, is recommended.

Setting the Storage Voltage

Set the storage voltage by choosing the external feedback resistors (R9 and R10) (see Figure 4).

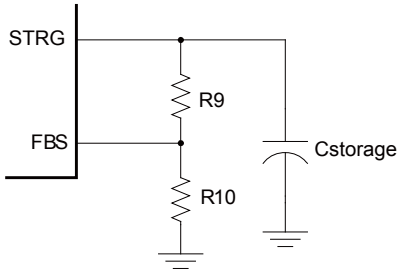

Figure 4: Storage Feedback Circuit

The storage voltage is determined with Equation (1):

$$V_{STORAGE} = (1 + \frac{R9}{R10}) \times V_{FBS} \quad (1)$$

Where V_{FBS} is 0.79V, typically. R9 and R10 are not critical for normal operation.

Select a higher R9 and R10 value to account for the bleed current. For example, if R10 is 14kΩ, calculate R9 with Equation (2):

$$R9 = \frac{14k\Omega \times (V_{STORAGE} - V_{FBS})}{V_{FBS}} \quad (2)$$

For a 12V storage voltage, R9 is 200kΩ.

Table 1 lists the recommended resistors for different storage voltages.

Table 1: Resistor Pairs for $V_{STORAGE}$

$V_{STORAGE}$ (V)	R9 (kΩ)	R10 (kΩ)
8	127	14
12	200	14
20	340	14

Selecting the Release Voltage and VB Capacitors

Select the release voltage by choosing the external feedback resistors R1 and R2 (see Figure 5).

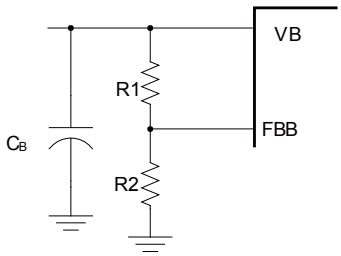

Figure 5. Release Feedback Circuit

Similarly, the release voltage is calculated with Equation (3):

$$V_{RELEASE} = (1 + \frac{R1}{R2}) \times V_{FBB} \quad (3)$$

Where V_{FBB} is 0.79V, typically. Generally, select R1 to be about 10kΩ and CB to be 22μF to 47μF. Table 2 lists the recommended resistor values for different release voltages.

Table 2: Resistor Pairs for $V_{RELEASE}$

$V_{RELEASE}$ (V)	R1 (kΩ)	R2 (kΩ)
4.2	10.5	2.43
2.9	10.7	4.02

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Selecting the Storage Capacitor

The storage capacitor stores energy during normal operation and releases this energy to VB when VIN loses input power. Use a general-purpose electrolytic capacitor or low-profile POS capacitor for most applications. One 4.7μF ceramic capacitor is recommended if the electrolytic capacitor ESR is high.

Select a storage capacitor with a voltage rating that exceeds the targeted storage voltage. Consider the capacitance reduction with the DC voltage offset when choosing the capacitors. Different capacitors have different capacitance de-rating performances. Choose a capacitor with enough voltage rating to guarantee enough capacitance.

The required capacitance depends on the length of the dying gasp for a typical application. Assume the release current is $I_{RELEASE}$ when VB is regulated at $V_{RELEASE}$ for the DC/DC converter, the storage is $V_{STORAGE}$, and the required dying gasp time is τ_{DASP}. The required storage capacitance is then calculated with Equation (4):

$$C_S = \frac{2 \times V_{RELEASE} \times I_{RELEASE} \times \tau_{DASP}}{V_{STORAGE}^2 - V_{RELEASE}^2} \quad (4)$$

Consider the power loss during release. The buck converter can run up to 85% efficiency in most applications. Select storage capacitance at $1.18xC_S$ to ensure enough releasing time. If $I_{RELEASE}$ = 1A, τ_{DASP} = 20ms, $V_{STORAGE}$ = 23.5V, and $V_{RELEASE}$ = 3.2V, then the required storage capacitance is 280μF.

For typical applications using a 5V input supply, set the storage voltage above 10V to utilize the high-voltage energy fully and minimize storage capacitance requirements. Use a 16V POS capacitor or 25V electrolytic capacitors.

Selecting the External Diode

An external diode parallel with the high-side power MOSFET (HS-FET) is optional for normal charge mode operation. This diode improves the boost efficiency if the boost peak current is high. The voltage rating should be higher than the storage voltage, and the current rating should be higher than the current programmed by ICH.

Setting the Input Hot-Swap Current Limit

Connect a resistor from ILIM to GND to set the current limit value. For example, a 1.2kΩ resistor sets the current limit to about 4.1A. Table 3 lists the recommended resistors for different current limit values.

Table 3: I_{LIM} vs. R_{LIM}

I_{LIM} (A)	R_{LIM} (kΩ)
4.6	1.07
4.1	1.2
3.7	1.4
1.6	3.2

Selecting the Inductor

The inductor is necessary to supply constant current to the load. Since boost mode and buck mode share the same inductor and the buck mode current is generally higher, an inductor that at least supports the buck mode releasing current is recommended.

Select the inductor based on the buck release mode. If the storage voltage is V_S, then the release voltage is V_R, and the buck running is fixed at 500kHz. The inductance value can be calculated with Equation (5):

$$L = \frac{V_R}{\Delta I_L \times F_{SW}} \times (1 - \frac{V_R}{V_S}) \quad (5)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which can be set in the range of 30% to 40% of the full releasing current.

The inductor should not saturate under the maximum inductor peak current.

Setting the Bus Voltage Rise Time

Connect a capacitor to DVDT to set the bus voltage start-up slew rate and soft-start time. Leave DVDT floating for the default soft-start time (around 0.9ms from 0V to 5V). Table 4 lists the recommended capacitors for different soft-start times at a 5V input condition.

Table 4: Soft Start vs. Capacitor Value

τ_R (mS)	$C_{dv/dt}$ (nF)
10	10
100	100

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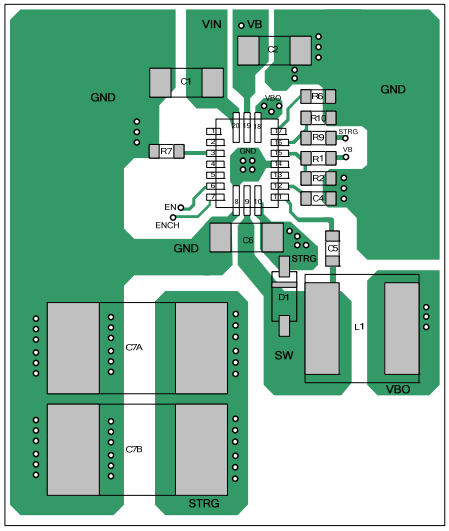
PCB Layout Guidelines [7]

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to achieve better thermal performance and simplify layout. For best results, refer to Figure 6 and follow the guidelines below.

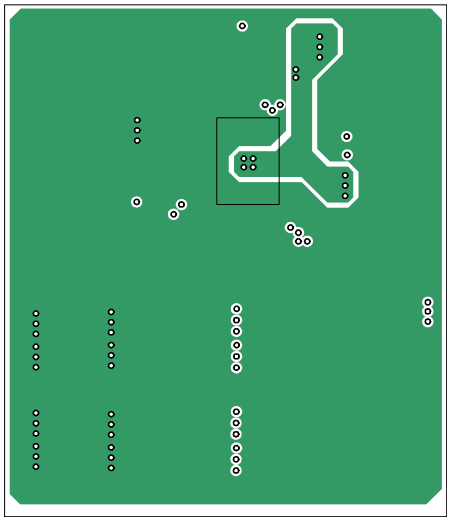
1) Use short, wide, and direct traces in the high-current paths (VIN, VB, VBO, SW, STRG, and GND).
2) Place the decoupling capacitor across VB and GND as close as possible.
3) Place the decoupling capacitor across STRG and GND as close to the pins as possible.
4) Keep the switching node SW short and away from the feedback network.
5) Place the external feedback resistors next to FB.
6) Keep the BST voltage path (BST, C5, and SW) as short as possible.

NOTE:

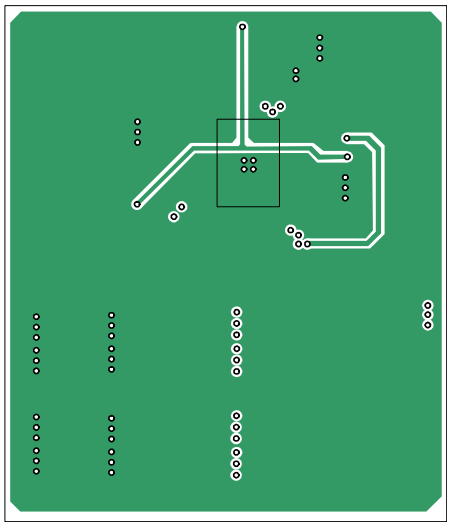
7) The corresponding schematic can be found on page 1. Note that the STRG bulk capacitors C7A and C7B are not shown in the schematic



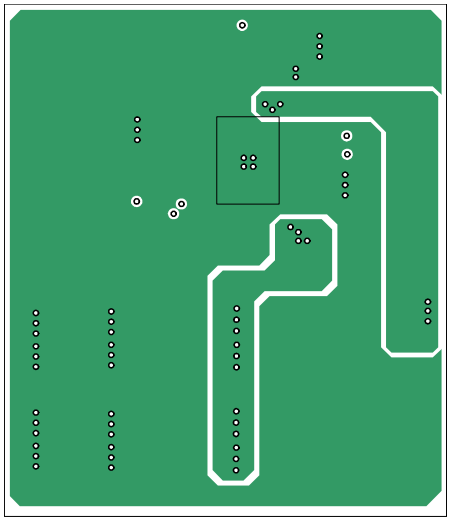
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 6: Recommended Layout

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Design Example

Table 5 shows a design example following the application guidelines for the specifications below.

Table 5: Design Example

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	3.5	V
Charge voltage	V_{STRG}	23.5	V
Bus release voltage	V_{RLS}	3.2	V
Boost inductor peak current	I_{CHARGE}	0.4	A
Buck max output current	$I_{RELEASE}$	2	A

The detailed application schematic is shown in Figure 7. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUIT

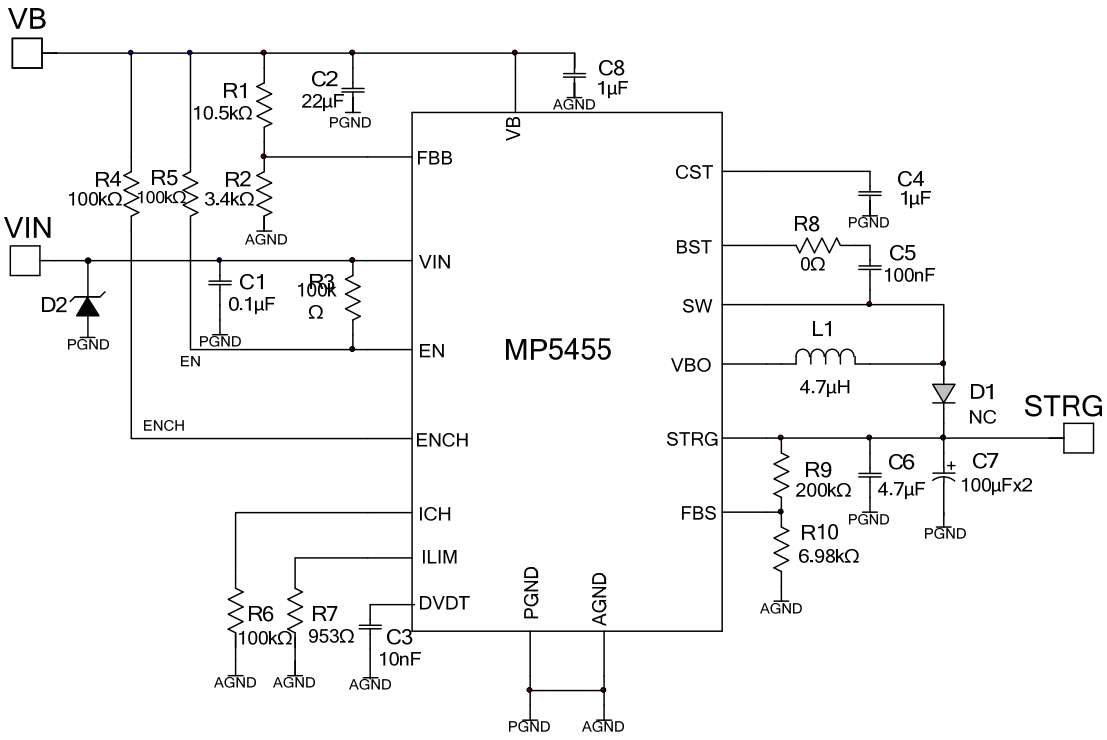

Figure 7: Detailed Application Schematic

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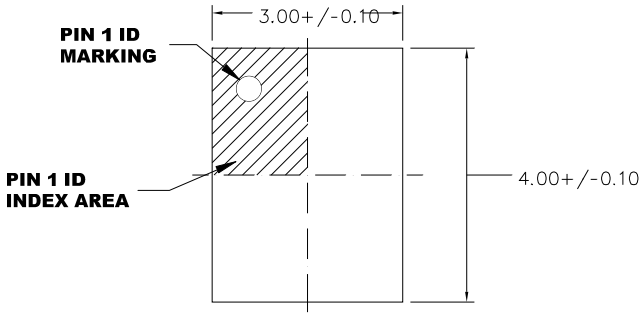
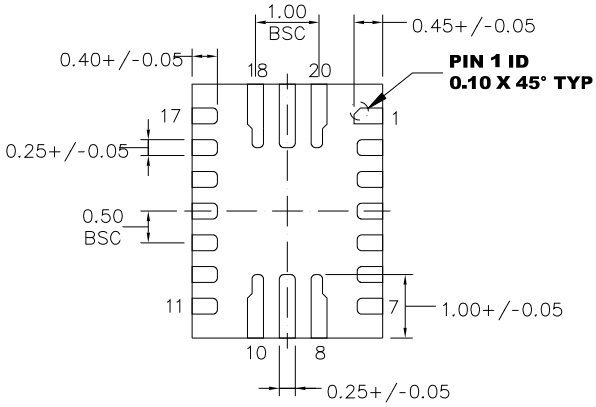
PACKAGE INFORMATION

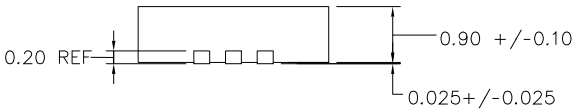
QFN-20 (3mmx4mm)



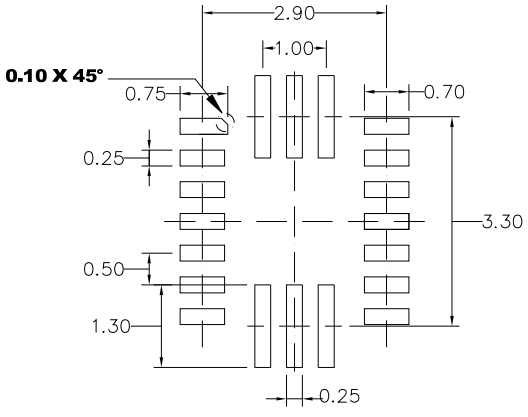
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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