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# NTMFS08N2D5C

## N-Channel Shielded Gate PowerTrench® MOSFET 80 V, 166 A, 2.7 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 2.7 mΩ at  $V_{GS} = 10$  V,  $I_D = 68$  A
- Max  $r_{DS(on)}$  = 6.7 mΩ at  $V_{GS} = 6$  V,  $I_D = 34$  A
- 50% lower  $Q_{rr}$  than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

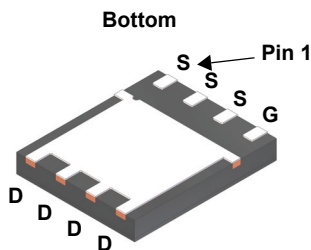
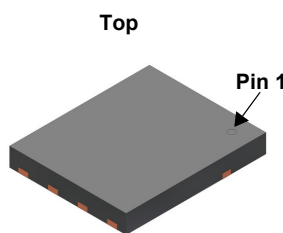


### General Description

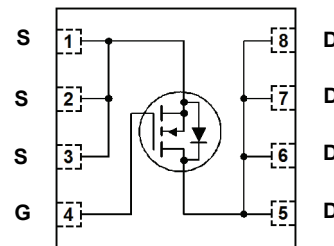
This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



Power 56



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	80	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25$ °C (Note 5)	166
	-Continuous	$T_C = 100$ °C (Note 5)	105
	-Continuous	$T_A = 25$ °C (Note 1a)	24
	-Pulsed	(Note 4)	823
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	600
$P_D$	Power Dissipation	$T_C = 25$ °C	138
	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.7
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
NTMFS08N2D5C	NTMFS08N2D5C	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		62		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 380\ \mu\text{A}$	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 380\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-8.3		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 68\ \text{A}$		2.2	2.7	m $\Omega$
		$V_{GS} = 6\ \text{V}, I_D = 34\ \text{A}$		3.3	6.7	
		$V_{GS} = 10\ \text{V}, I_D = 68\ \text{A}, T_J = 125^\circ\text{C}$		3.7	4.5	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 68\ \text{A}$		148		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 40\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		4455	6240	pF
$C_{oss}$	Output Capacitance			1480	2070	pF
$C_{rss}$	Reverse Transfer Capacitance			59	85	pF
$R_g$	Gate Resistance			0.8	1.6	$\Omega$

### Switching Characteristics

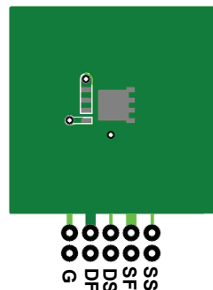
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\ \text{V}, I_D = 68\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		21	34	ns
$t_r$	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			29	47	ns
$t_f$	Fall Time			7	13	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 10\ \text{V}$		60	84
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 6\ \text{V}$	$V_{DD} = 40\ \text{V},$ $I_D = 68\ \text{A}$	38	54	nC
$Q_{gs}$	Gate to Source Charge			19		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			12		nC
$Q_{oss}$	Output Charge	$V_{DD} = 40\ \text{V}, V_{GS} = 0\ \text{V}$		84		
$Q_{sync}$	Total Gate Charge Sync	$V_{DS} = 0\ \text{V}, I_D = 68\ \text{A}$		51		nC

### Drain-Source Diode Characteristics

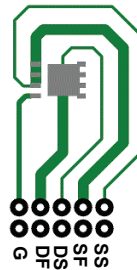
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 2.2\ \text{A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\ \text{V}, I_S = 68\ \text{A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 34\ \text{A}, di/dt = 300\ \text{A}/\mu\text{s}$		30	48	ns
$Q_{rr}$	Reverse Recovery Charge			55	88	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 34\ \text{A}, di/dt = 1000\ \text{A}/\mu\text{s}$		24	39	ns
$Q_{rr}$	Reverse Recovery Charge			139	222	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\ \text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\ \text{in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a.  $45^\circ\text{C}/\text{W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper.



b.  $115^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

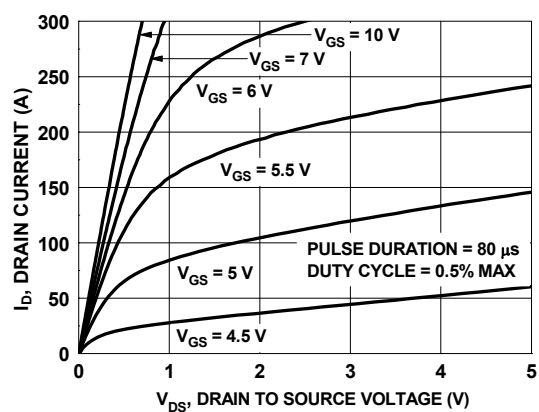
2. Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 600 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3\ \text{mH}, I_{AS} = 20\ \text{A}, V_{DD} = 80\ \text{V}, V_{GS} = 10\ \text{V}$ . 100% test at  $L = 0.1\ \text{mH}, I_{AS} = 63\ \text{A}$ .

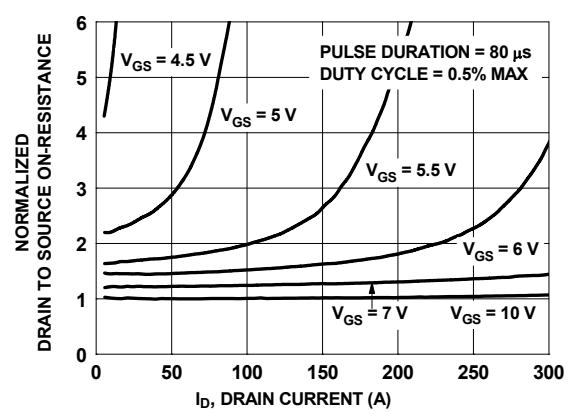
4. Pulsed  $I_D$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

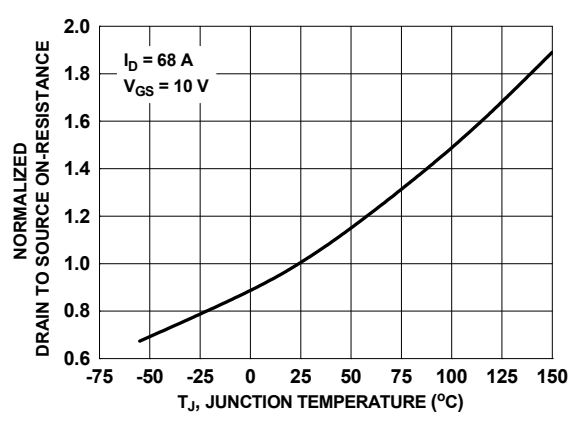
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



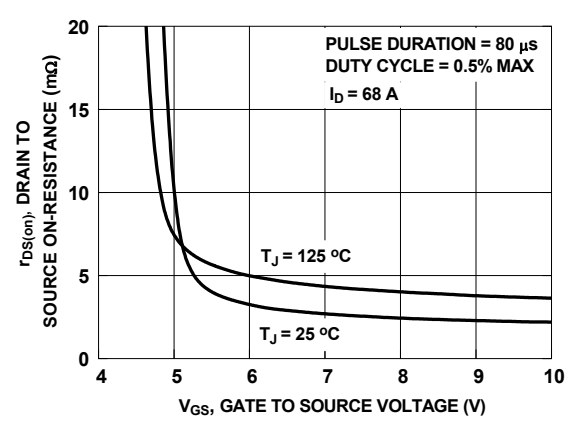
**Figure 1. On Region Characteristics**



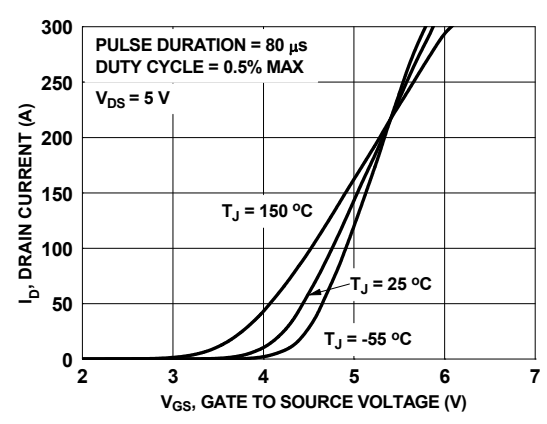
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



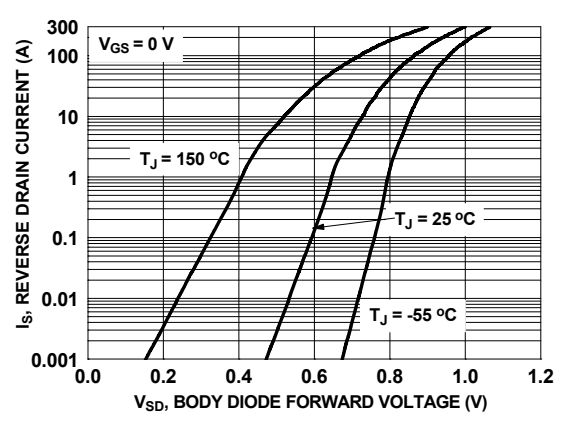
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

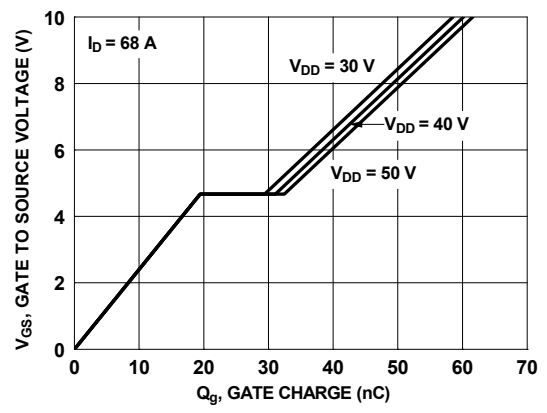


**Figure 5. Transfer Characteristics**

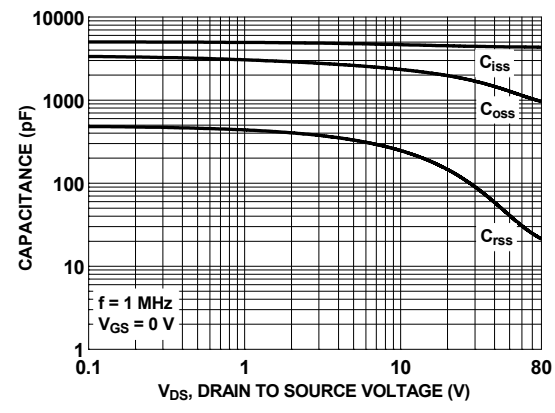


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

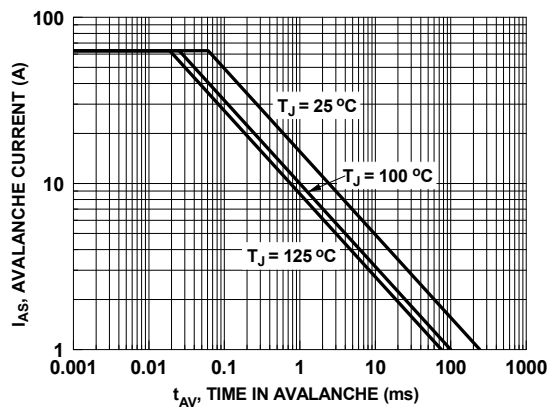
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



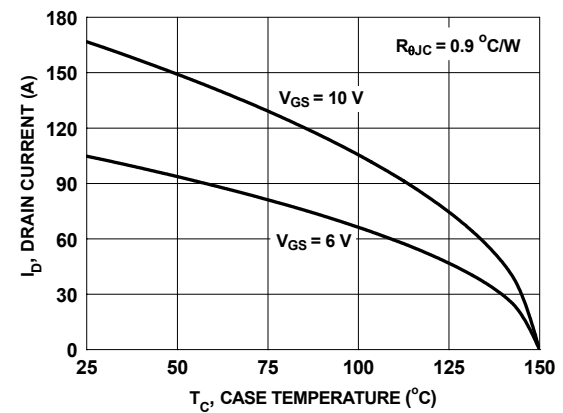
**Figure 7. Gate Charge Characteristics**



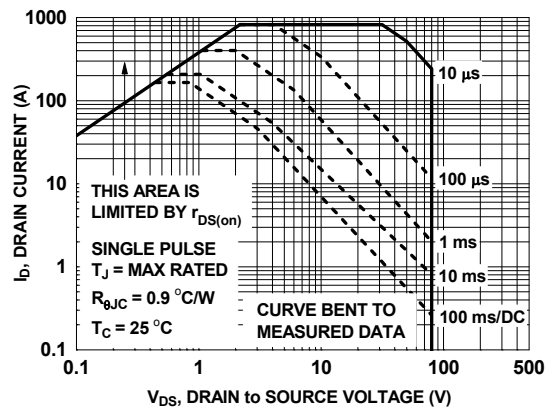
**Figure 8. Capacitance vs. Drain to Source Voltage**



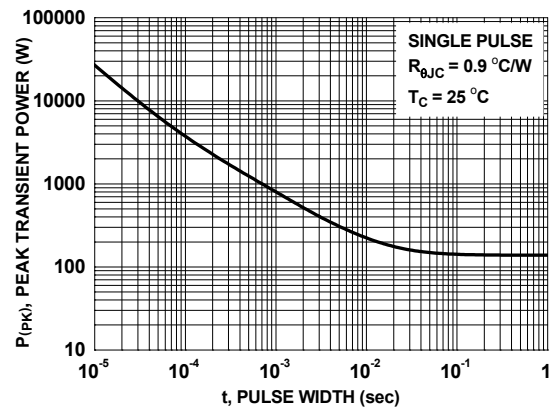
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

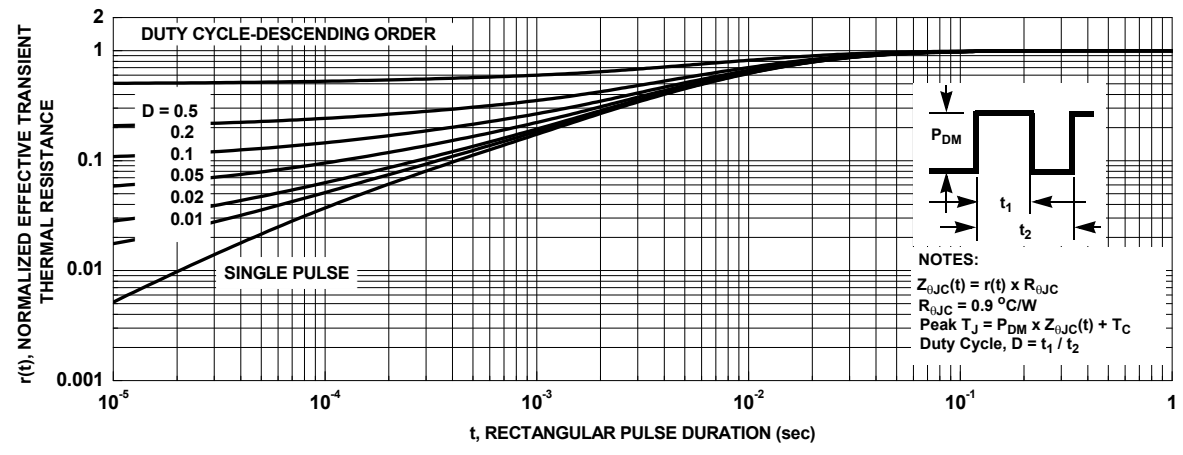


**Figure 11. Forward Bias Safe Operating Area**

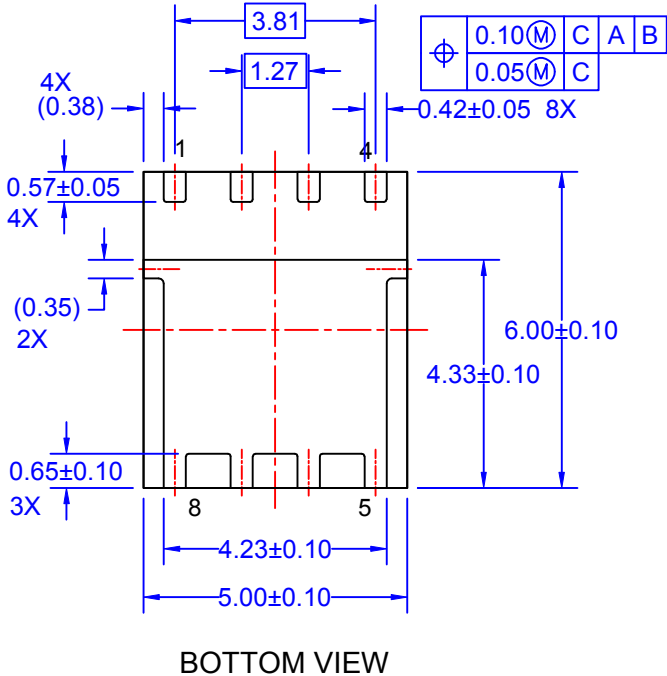
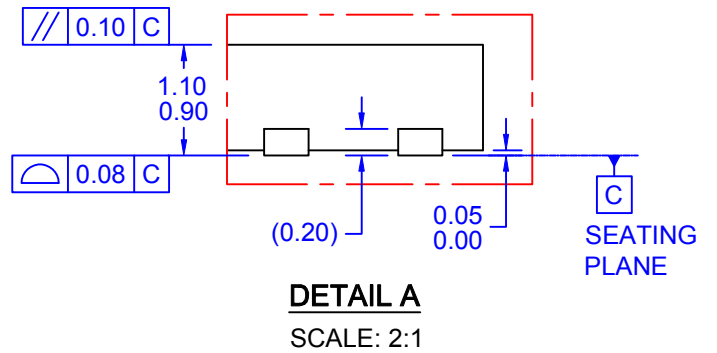
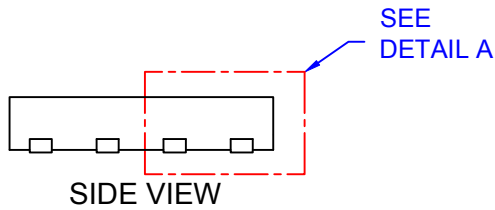
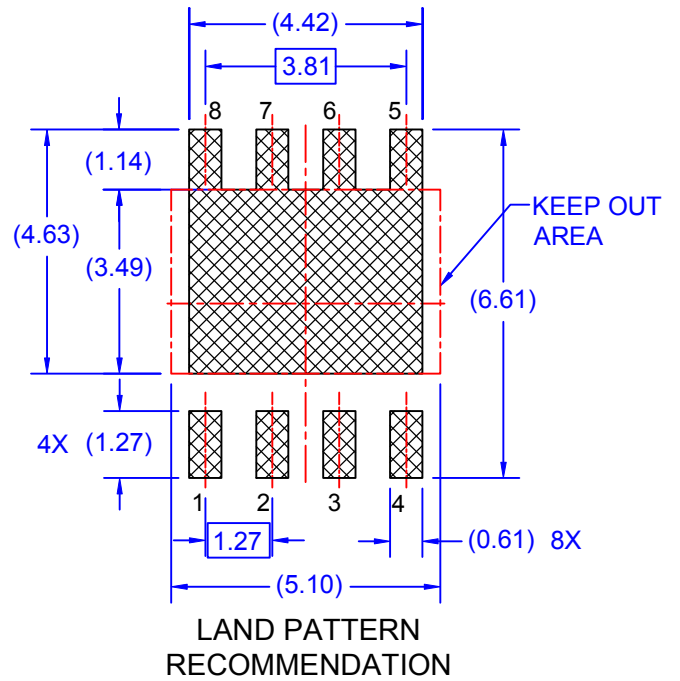
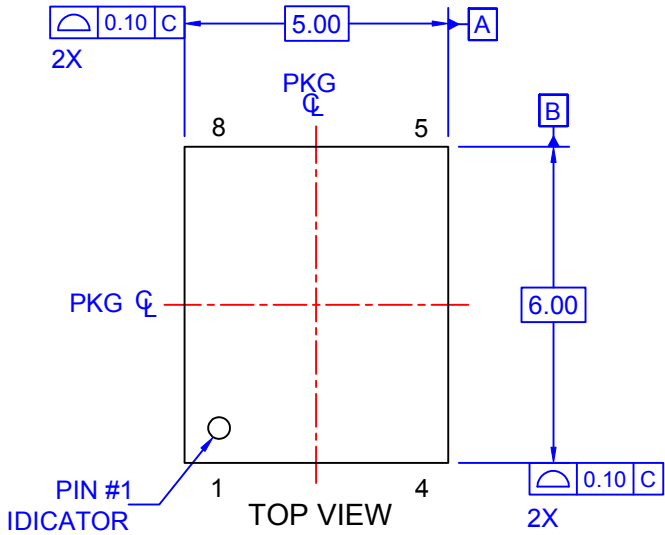


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08TREV1.



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