STD52P3LLH6

P-channel 30 V, 0.01 Ω typ., 52 A, STripFET™ H6 Power MOSFET in a DPAK package

Datasheet - preliminary data

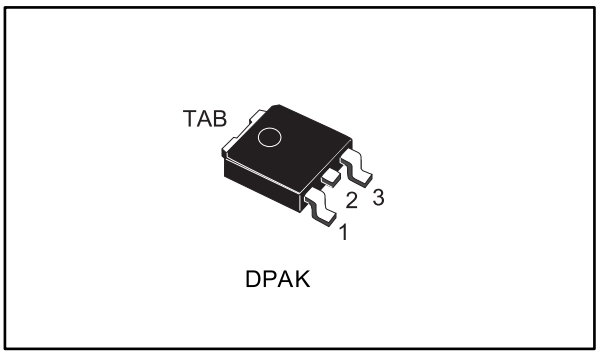
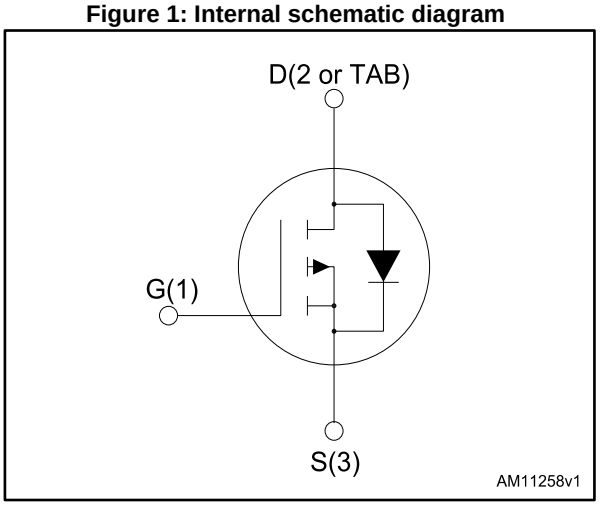


Figure 1: Internal schematic diagram



Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STD52P3LLH6	30 V	0.012 Ω	52 A	70 W

- Very low on-resistance
- Very low gate charge
- High avalanche
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STD52P3LLH6	52P3LLH6	DPAK	Tape and reel

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	52	A
I_D	Drain current (continuous) at T_C = 100 °C	37.5	A
I_{DM} (1)	Drain current (pulsed)	208	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature	175	°C

Notes:

(1)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.14	°C/W

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 30 V			1	µA
		V_{GS} = 0, V_{DS} = 30 V, Tc = 125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{GS} = ± 20 V, V_{DS} = 0			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 26 A		0.01	0.012	Ω
		V_{GS} = 4.5 V, I_D = 26 A		0.014	0.017	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	3350	-	pF
C_{oss}	Output capacitance		-	414	-	pF
C_{rss}	Reverse transfer capacitance		-	287	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 52 A V_{GS} = 4.5 V (see *Figure 14: "Gate charge test circuit"*)	-	33	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC
R_g	Gate input resistance	ID = 0 Gate bias = 0 Test signal level = 20 mV f = 1MHz	-	1.5		Ω

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 6: Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 24 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Switching times test circuit for resistive load"*)	-	12.8	-	ns
t_r	Rise time		-	112	-	ns
$t_{d(off)}$	Turn-off delay time		-	61	-	ns
t_f	Fall time		-	45	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 52 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 52 A, di/dt = 100 A/µs, V_{DD} = 24 V (see *Figure 15: "Source-drain diode forward characteristics"*)	-	25.2		ns
Q_{rr}	Reverse recovery charge		-	17.4		nC
I_{RRM}	Reverse recovery current		-	1.4		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

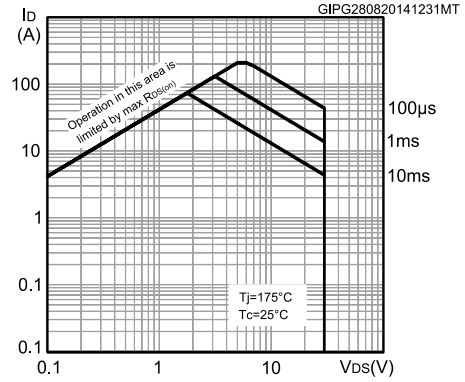


Figure 3: Thermal impedance

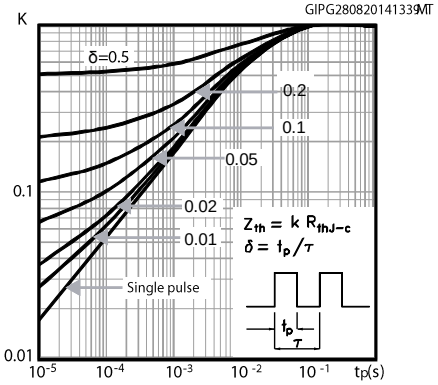


Figure 4: Output characteristics

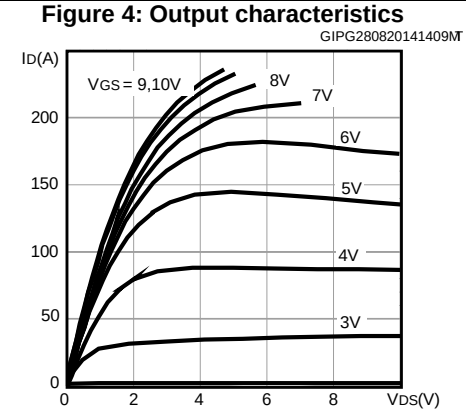


Figure 5: Transfer characteristics

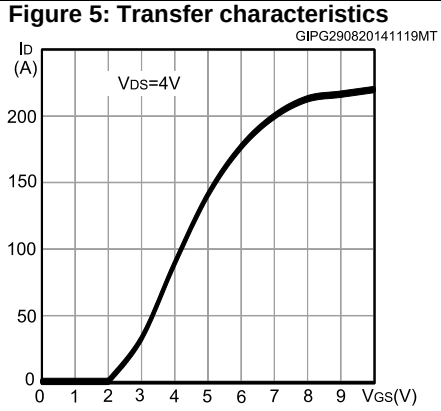


Figure 6: Gate charge vs gate-source voltage

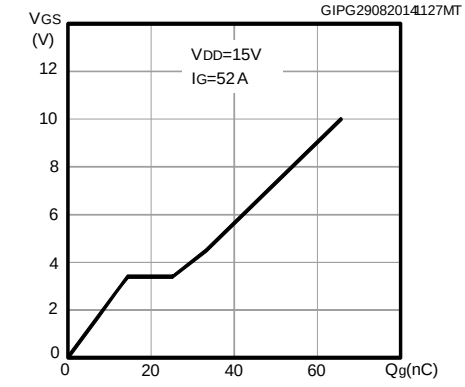


Figure 7: Static drain-source on-resistance

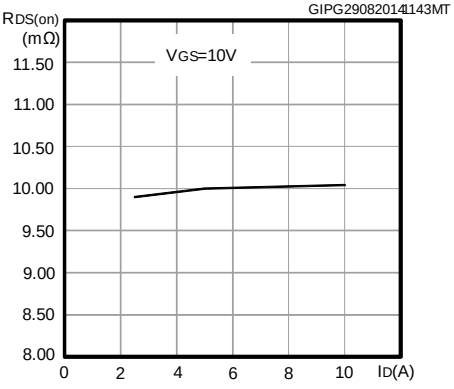


Figure 8: Capacitance variations

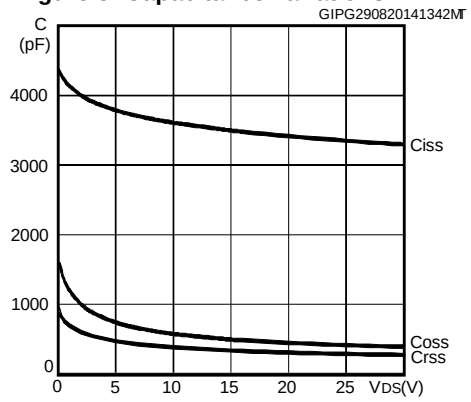


Figure 9: Normalized gate threshold voltage vs temperature

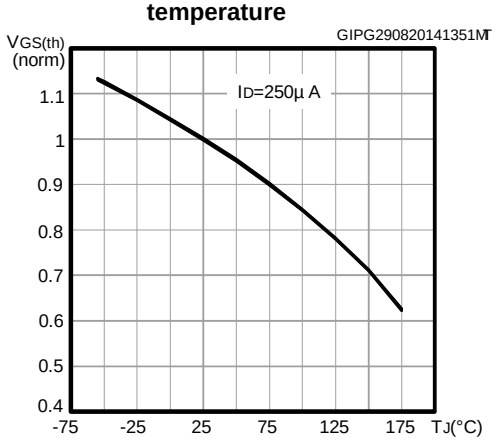


Figure 10: Normalized on-resistance vs temperature

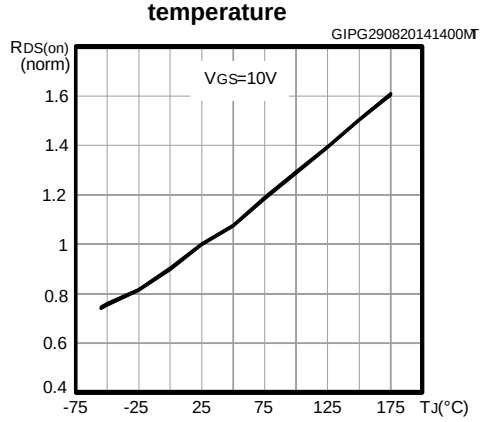


Figure 11: Normalized V(BR)DSS vs temperature

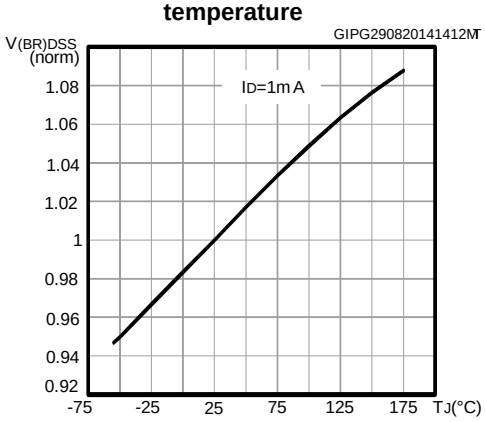
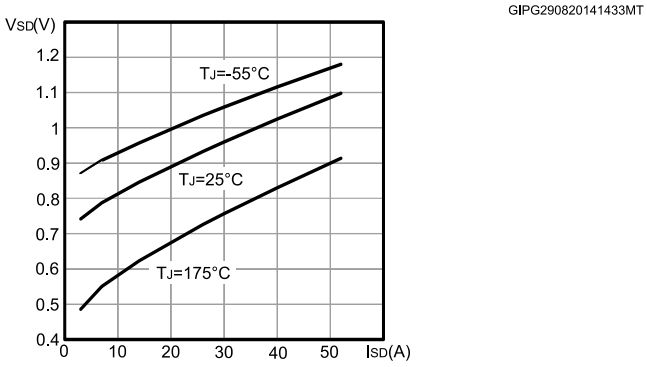


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

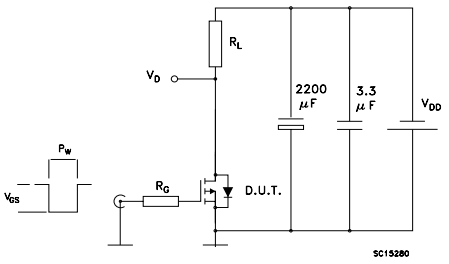


Figure 14: Gate charge test circuit

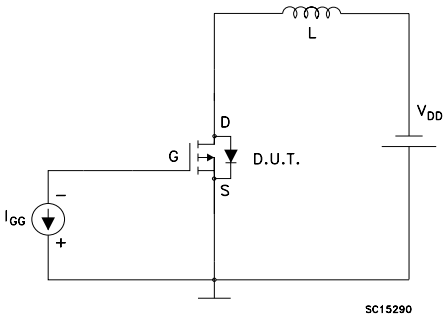
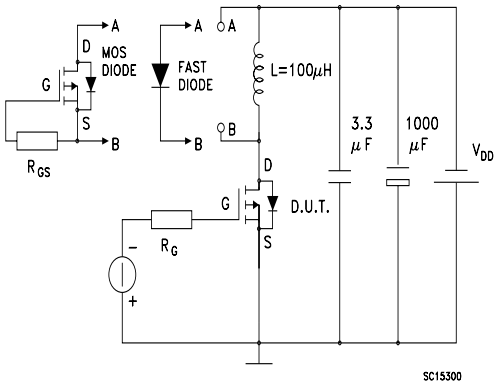


Figure 15: Source-drain diode forward characteristics



4 Package mechanical data

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4.1 DPAK (TO-252) mechanical data

Figure 16: DPAK (TO-252) type A drawings

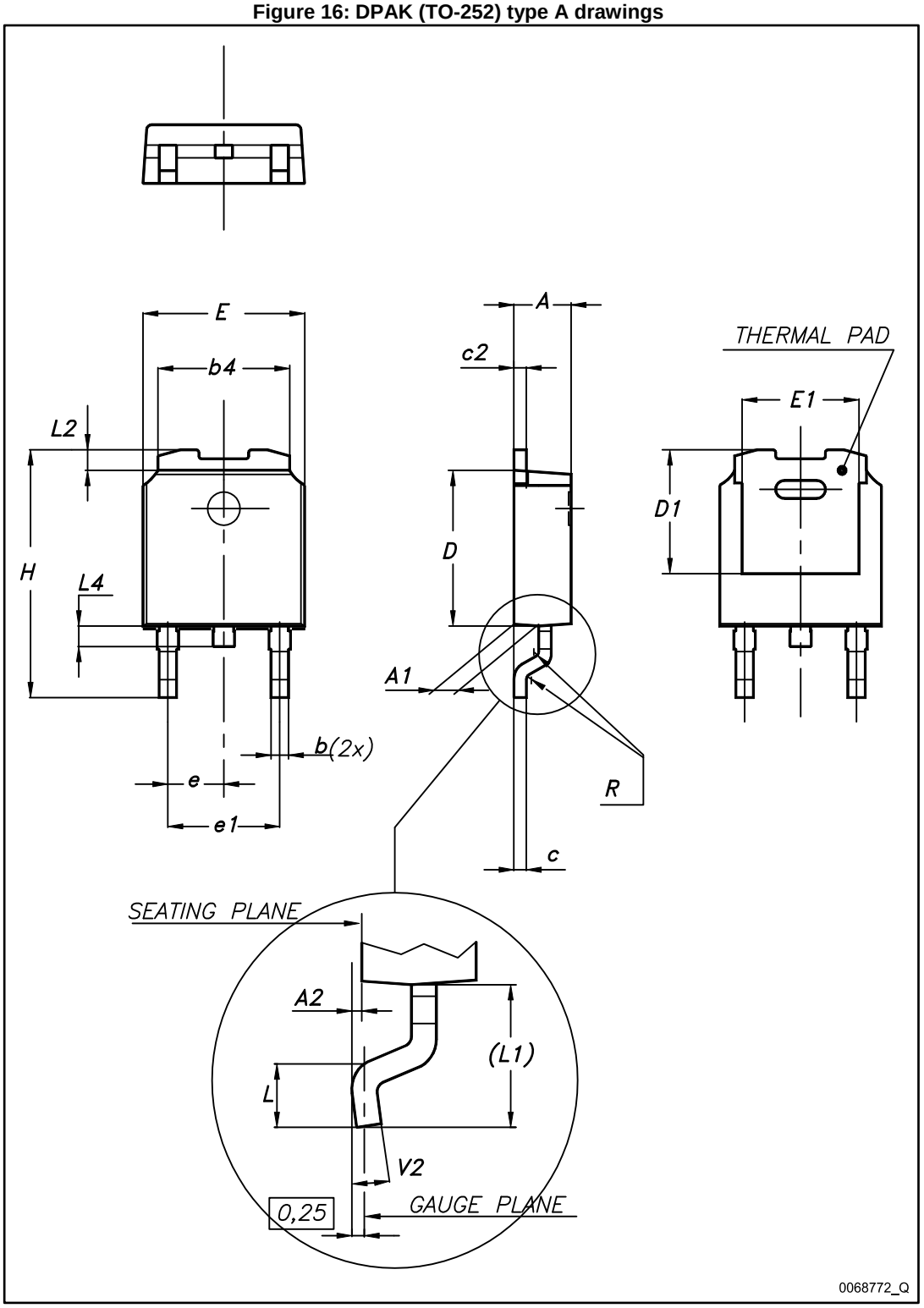
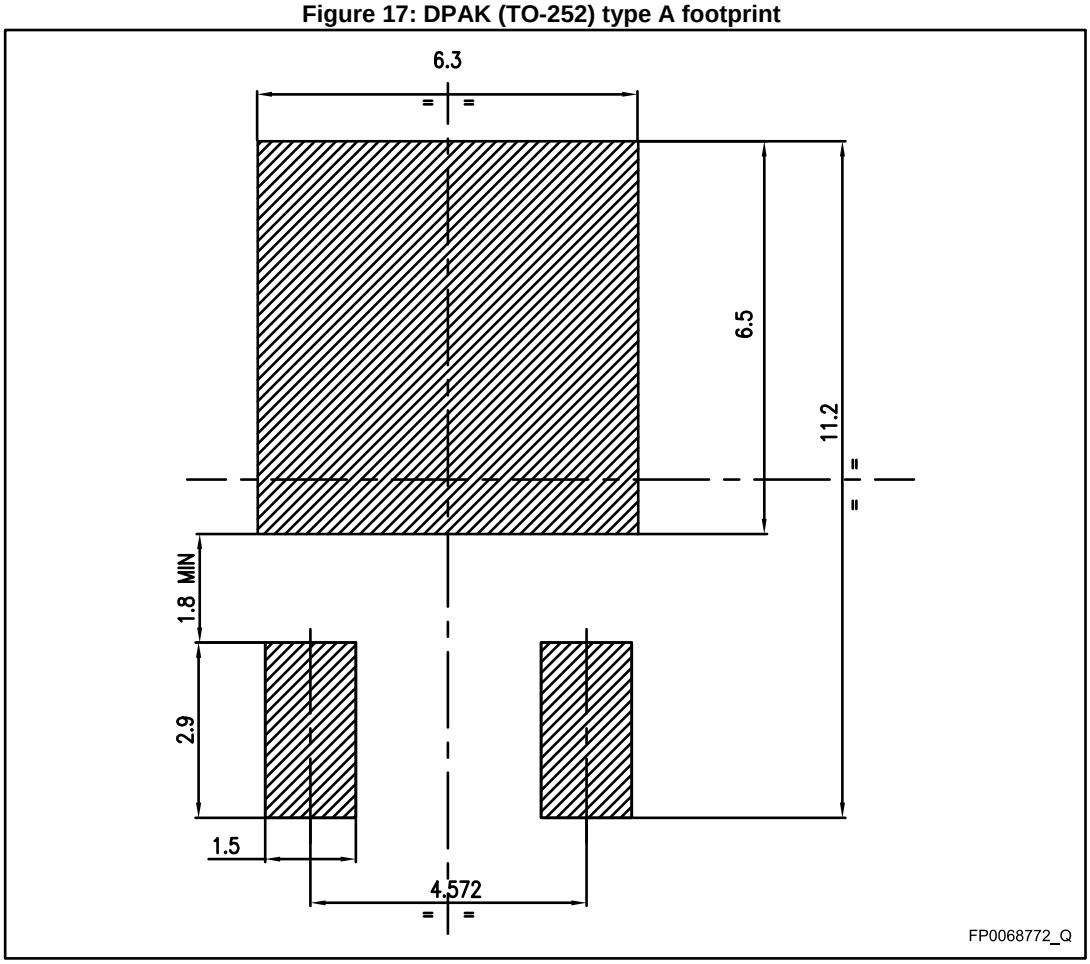


Table 8: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) type A footprint



All dimensions are in mm

5 Packaging mechanical data

5.1 DPAK (TO-252) tape and reel mechanical data

Figure 18: Tape for DPAK (TO-252)

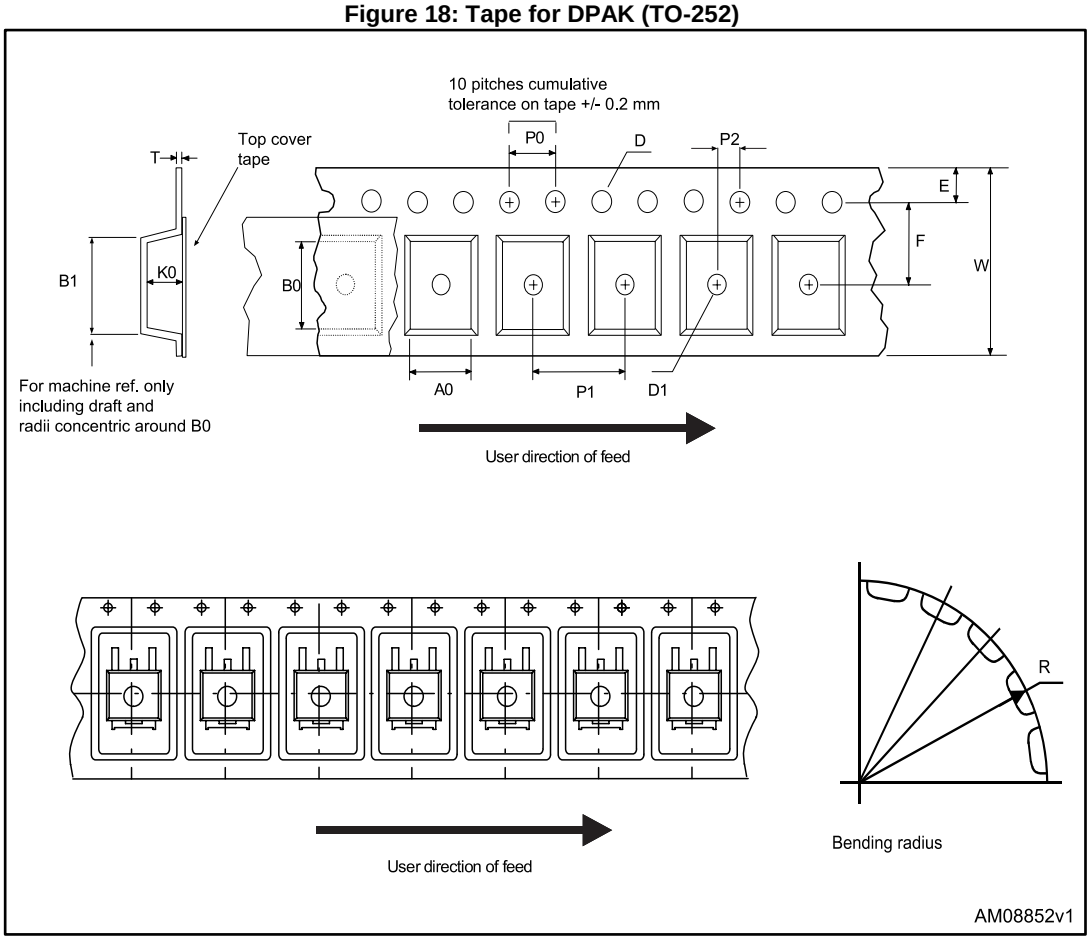


Figure 19: Reel for DPAK (TO-252)

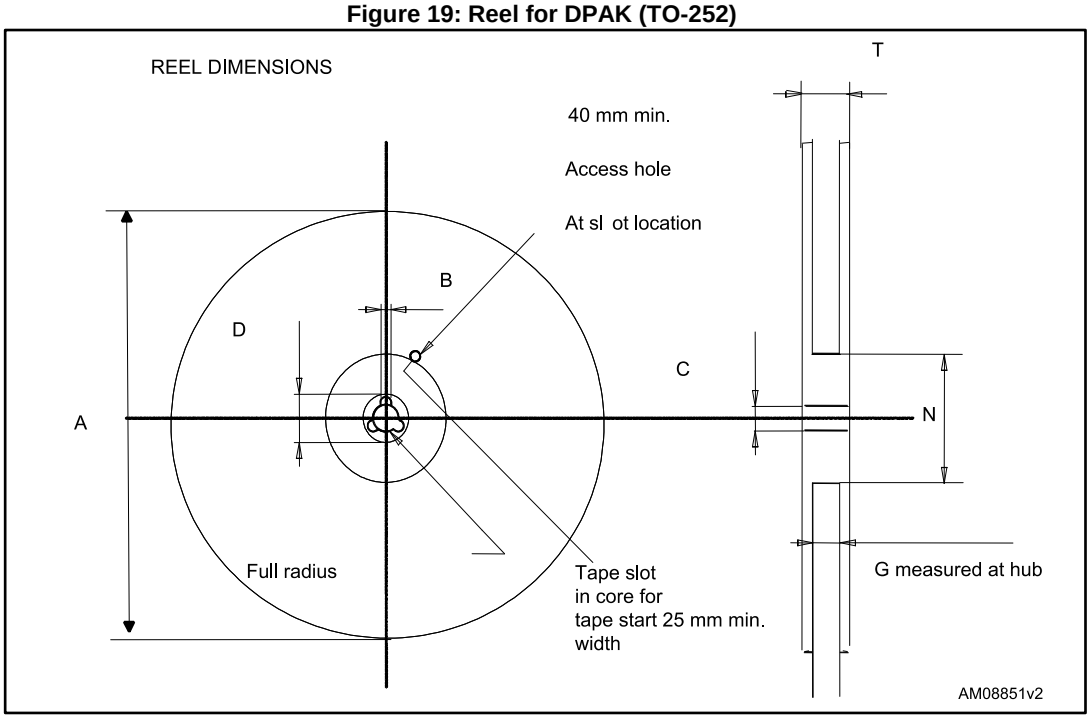


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 10: Document revision history

Date	Revision	Changes
02-Jun-2014	1	First release
24-Sep-2014	2	Updated the title, the features and the description in cover page. Updated *Table 2: "Absolute maximum ratings"*, *Section 2: "Electrical characteristics"*. Added *Section 2.1: "Electrical characteristics (curves)"* . Minor text changes.

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