

# DATA SHEET

## **CBTD16210**

20-bit level shifting bus switch  
with 10-bit output enables

Product specification  
Supersedes data of 2000 Sep 25

2000 Oct 12

# 20-bit level shifting bus switch with 10-bit output enables

## CBTD16210

### FEATURES

- 5Ω switch connection between two ports
- TTL compatible control input levels
- Designed to be used in 5.5 V to 3.3 V level shifting applications
- Package options include shrink small outline (SSOP) and thin shrink small outline (TSSOP)

### DESCRIPTION

The CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

A diode to  $V_{CC}$  is integrated in the circuit to allow for level shifting between 5 V inputs and 3.3 V outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and a high-impedance state exists between the ports.

The CBTD16210 is characterized for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

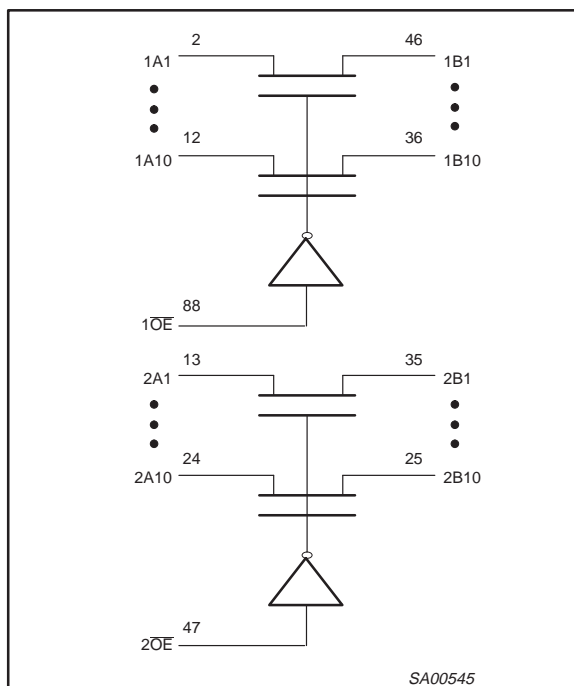
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Yn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	0.25	ns
$C_{\text{IN}}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	4.3	pF
$C_{\text{OUT}}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or $V_{CC}$	6.9	pF
$I_{\text{CCZ}}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	4.0	$\mu\text{A}$

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	CBTD16210 DL	SOT370-1
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	CBTD16210 DGG	SOT362-1

### LOGIC SYMBOL



### FUNCTION TABLE

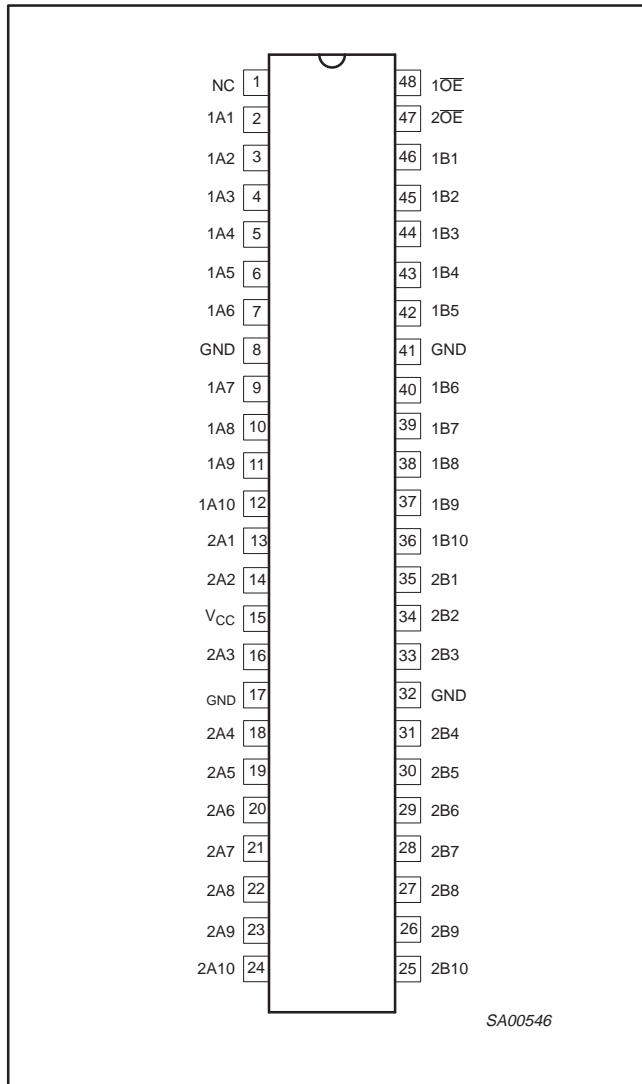
INPUTS		OUTPUTS	
$1\overline{OE}$	$2\overline{OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level  
 L = Low voltage level  
 Z = High impedance "off" state

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CBTD16210

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	NC	No internal connection
48, 47	1OE, 2OE	Output enables
2, 3, 4, 5, 6, 7, 9, 10, 11, 12	1A1-1A10	Inputs
46, 45, 44, 43, 42, 40, 39, 38, 37, 36	1B1-1B10	Outputs
13, 14, 16, 18, 19, 20, 21, 22, 23, 24	2A1-2A10	Inputs
35, 34, 33, 31, 30, 29, 28, 27, 26, 25	2B1-2B10	Outputs
8, 17, 32, 41	GND	Ground (0V)
15	V <sub>CC</sub>	Positive supply voltage

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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	128	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level Input voltage		0.8	V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			
			Min	Typ <sup>1</sup>	Max	
$V_{IK}$	Input clamp voltage	$V_{CC} = 4.5\text{ V}; I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	Output high pass voltage	See Figure 1, page 6				V
$I_I$	Input leakage current	$V_{CC} = 0\text{ V}; V_I = 5.5\text{ V}$			10	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}; V_I = \text{GND or } 5.5\text{ V}$			$\pm 1$	
$I_{CC}$	Quiescent supply current <sup>2</sup>	$V_{CC} = 5.5\text{ V}; I_O = 0, V_I = V_{CC}\text{ or GND}; 1OE=2OE=GND$			1.5	mA
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC} = 5.5\text{ V}$ , one input at 3.4 V, other inputs at $V_{CC}$ or GND			2.5	mA
$C_I$	Control pins	$V_I = 3\text{ V or } 0$		4.5		pF
$C_{IO(OFF)}$	Power-off leakage current	$V_O = 3\text{ V or } 0, \overline{OE} = V_{CC}$		8		pF
$r_{on}^3$		$V_{CC} = 4.5\text{ V}; V_I = 0\text{ V}; I_I = 64\text{ mA}$		5	7	$\Omega$
		$V_{CC} = 4.5\text{ V}; V_I = 0\text{ V}; I_I = 30\text{ mA}$		5	7	
		$V_{CC} = 4.5\text{ V}; V_I = 2.4\text{ V}; I_I = -15\text{ mA}$		16	50	

### NOTES:

- All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.  
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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CBTD16210

## AC CHARACTERISTICS

GND = 0 V;  $t_R$ ;  $C_L = 50$  pF

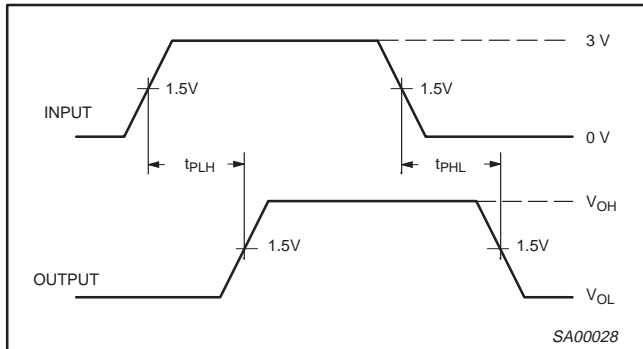
SYMBOL	PARAMETER DESCRIPTION	LIMITS -40°C to +85°C $V_{CC} = 5 V \pm 0.5 V$			UNITS
		Min	Mean	Max	
$t_{pd}$	Propagation delay <sup>1</sup>			250	ps
$t_{pZH}$	Output enable time to HIGH level	1.5	5.0	7.5	ns
$t_{pHZ}$	Output disable time from HIGH level	1.0	2.5	4.5	ns
$t_{pZL}$	Output enable time to LOW level	1.5	6.0	9.0	ns
$t_{pLZ}$	Output disable time from LOW level	1.5	3.5	6.0	ns

### NOTES:

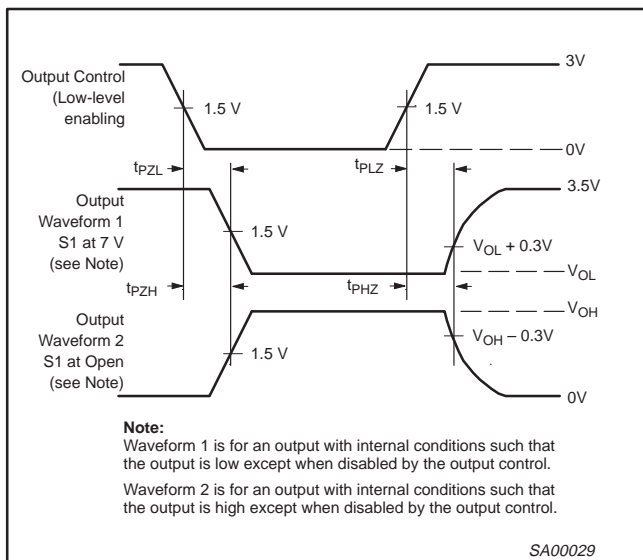
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

## AC WAVEFORMS

$V_M = 1.5 V$ ,  $V_{IN} = GND$  to 3.0 V

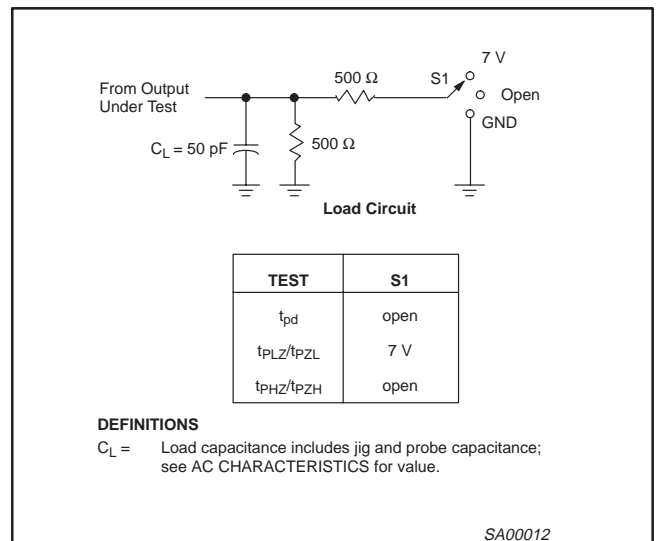


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

## TEST CIRCUIT AND WAVEFORMS



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CBTD16210

## TYPICAL CHARACTERISTICS

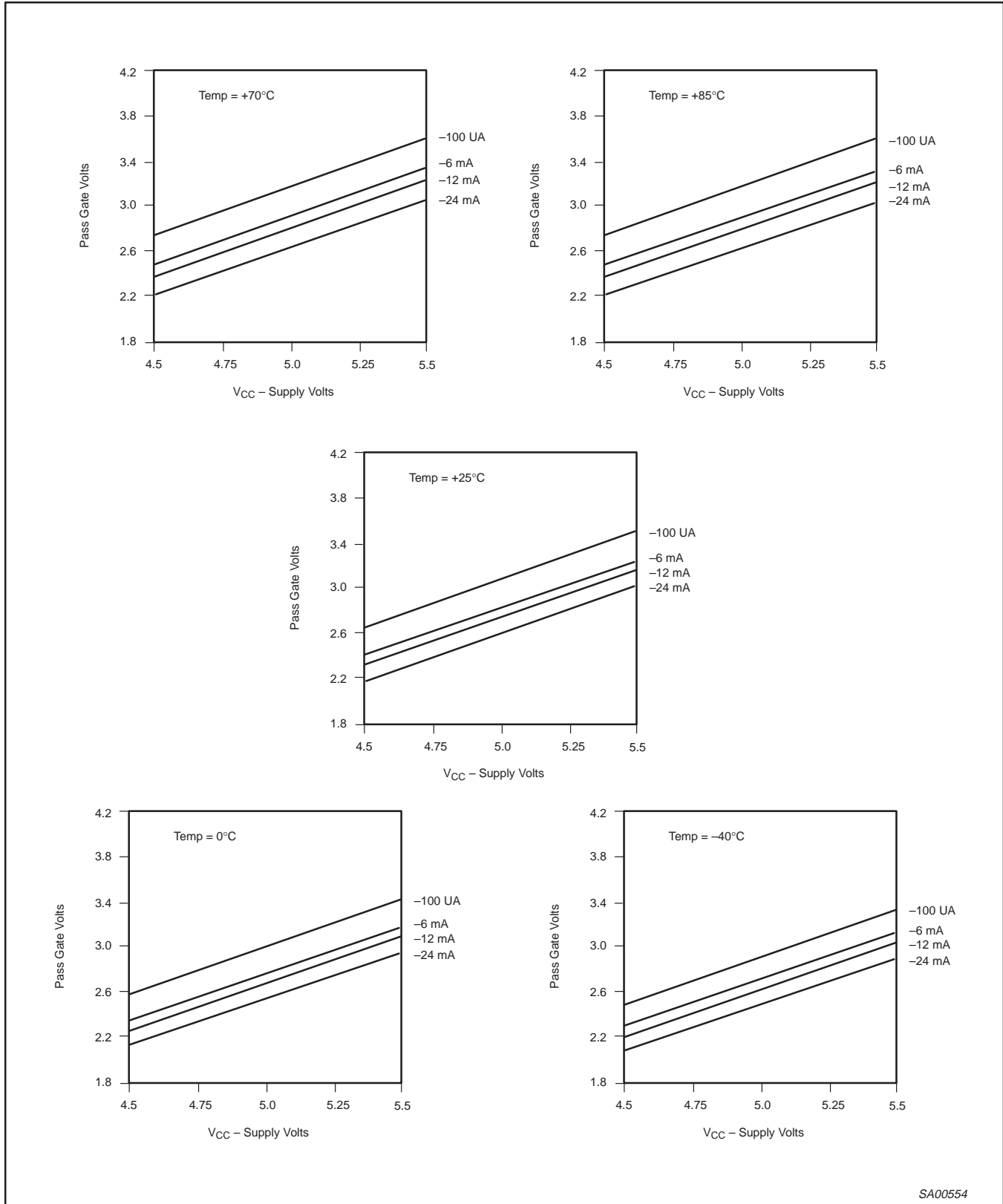


Figure 1.  $V_{OH}$  values ( $V_{in} = V_{CC}$ )

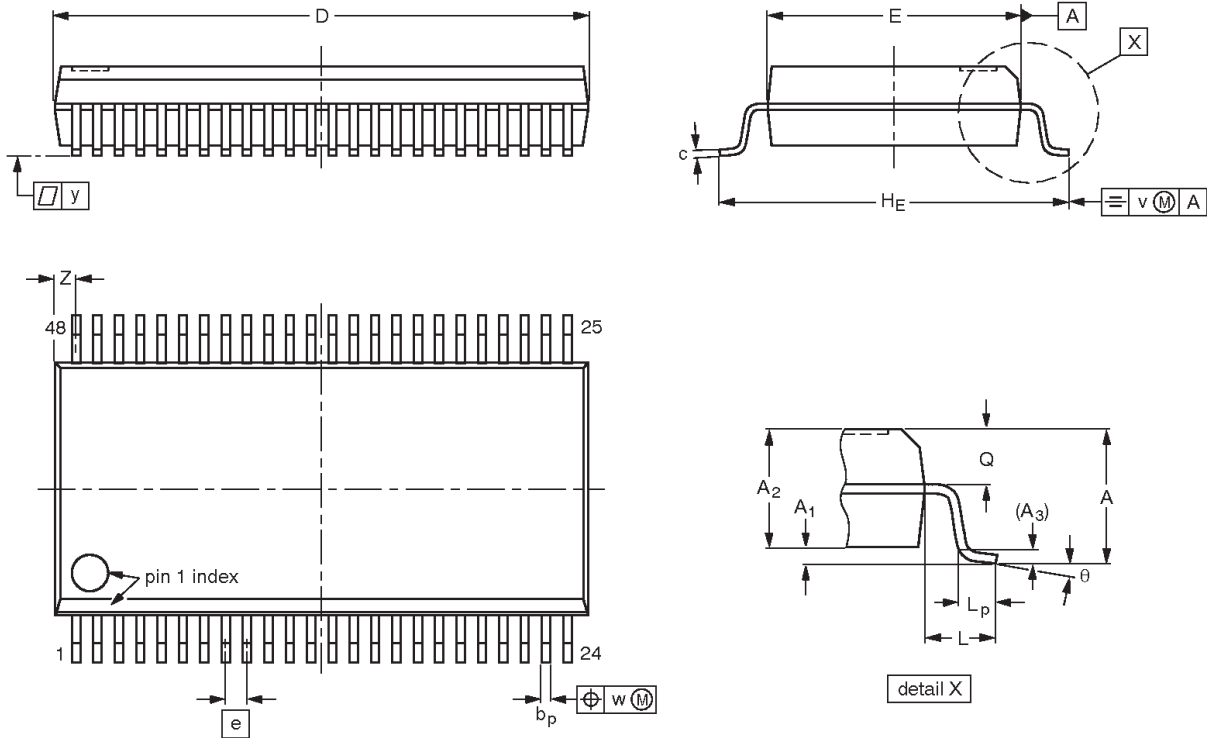
SA00554

# 20-bit level shifting bus switch with 10-bit output enables

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

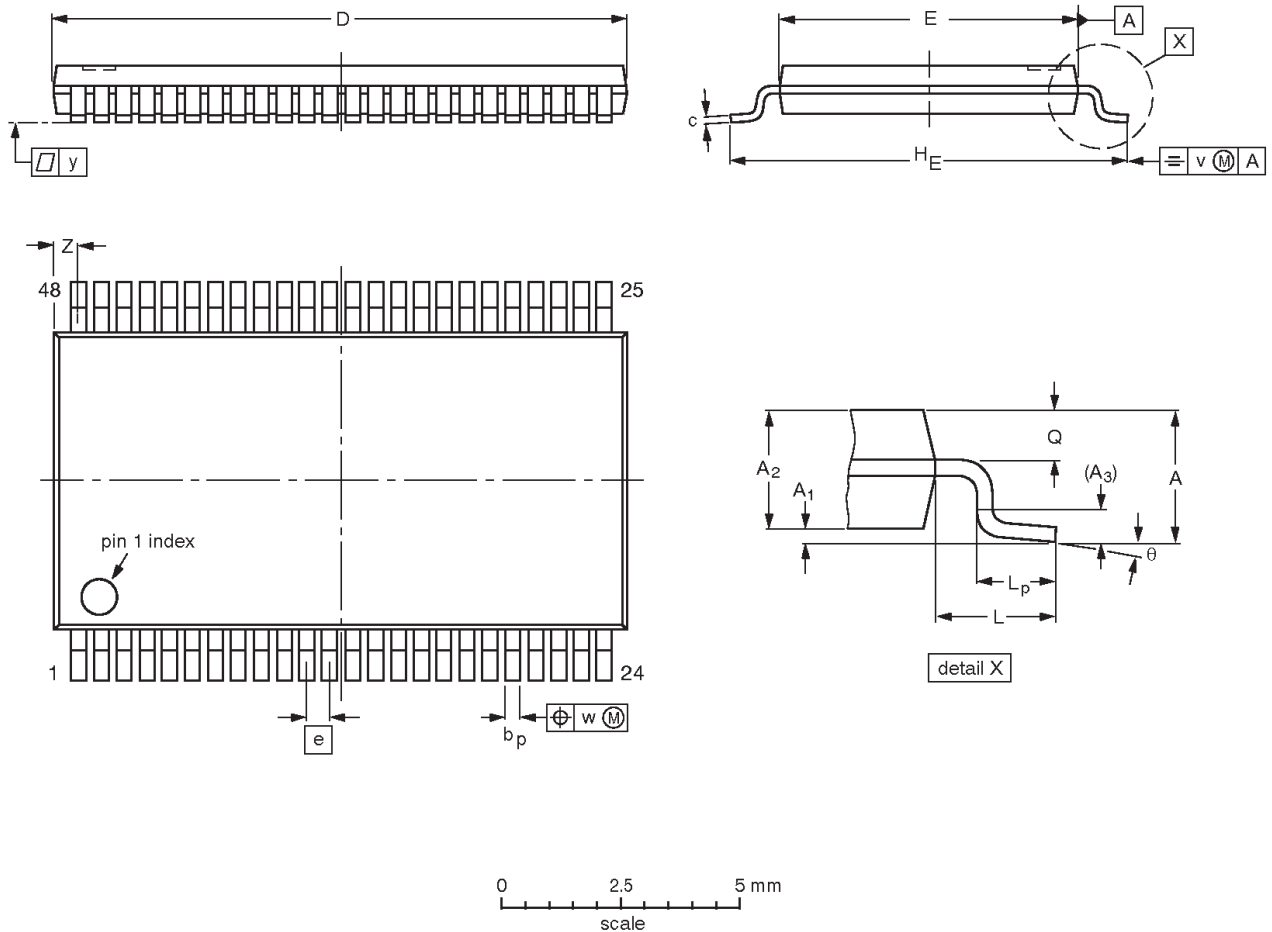
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118				95-02-04 99-12-27

# 20-bit level shifting bus switch with 10-bit output enables

CBTD16210

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27



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CBTD16210

**NOTES**

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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