

### General Description

The QPL9097 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 3.8 GHz, the amplifier typically provides 22 dB gain, +32 dBm OIP3, and 1.0 dB noise figure while drawing 50 mA current from a +4.2 V supply.

The QPL9097 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The QPL9097 is optimized for the 3.3–4.2 GHz frequency band and is targeted for wireless infrastructure. The QPL9097 is packaged in a 2x2 mm DFN.

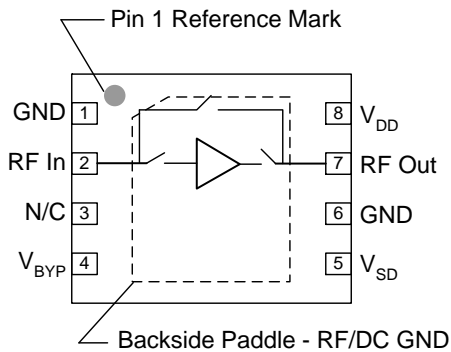


8 Pin 2X2 mm DFN Package

### Product Features

- 3.3 – 4.2 GHz Operational bandwidth
- LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra low noise, 1.0 dB at 3.8 GHz
- 22 dB Gain at 3.8 GHz
- +32 dBm Output IP3 in LNA Mode
- +35 dBm Input IP3 in Bypass Mode
- Internally matched
- Positive supply only, +3.3 to +5 V
- 2x2 mm 8-pin DFN plastic package

### Functional Block Diagram



Top View

### Applications

- Base-station Receivers
- Repeaters / DAS
- Tower Mounted Amplifiers
- Mobile Infrastructure
- General Purpose Wireless
- TDD or FDD systems

### Ordering Information

Part No.	Description
QPL9097SR	100 pcs on 7" reel
QPL9097TR7	2500 pcs on 7" reel
QPL9097EVBP01 <sup>(1)</sup>	Evaluation Board

1. Refer board details and performance on pgs. 3 & 4.

## Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
Supply Voltage (V <sub>DD</sub> )	+7 V
RF Input Power, CW, 50Ω, T=25°C	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V <sub>DD</sub> )	3.0	4.2	5.25	V
T <sub>CASE</sub>	-40		+105	°C
T <sub>j</sub> at T <sub>CASE</sub> = 125°C			+142	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted: V<sub>DD</sub> = +4.2 V, Temp.=+25°C.

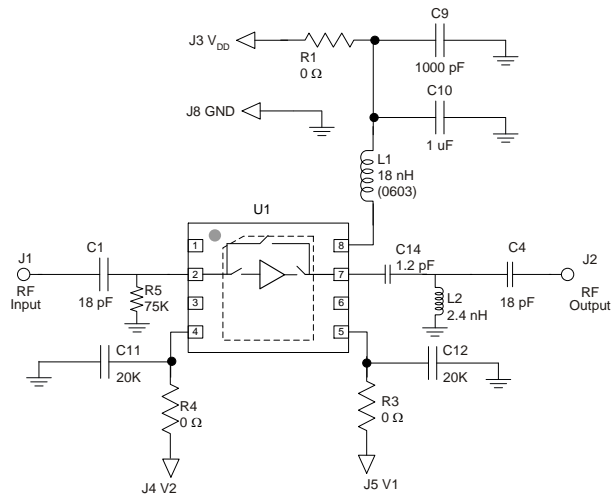
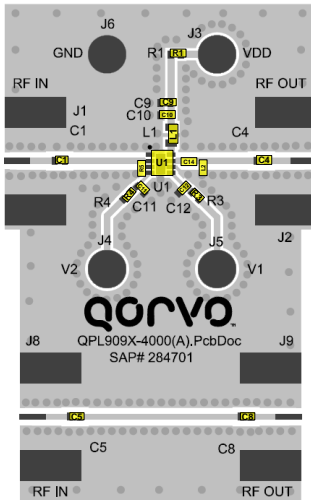
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3300		4200	MHz
Test Frequency			4200		MHz
Gain	LNA ON, Bypass OFF		22		dB
Input Return Loss	LNA ON, Bypass OFF		12		dB
Output Return Loss	LNA ON, Bypass OFF		11.5		dB
Noise Figure <sup>(2)</sup>	LNA ON, Bypass OFF		1.1		dB
Output P1dB	LNA ON, Bypass OFF		+15.5		dBm
Output IP3	LNA ON, Bypass OFF, P <sub>out</sub> =+0 dBm/tone, Δf=5 MHz		+32.5		dBm
Insertion Loss	LNA OFF, Bypass ON		2.0		dB
Return Loss	LNA OFF, Bypass ON		13		dB
Isolation <sup>(1)</sup>	LNA OFF, Bypass OFF		20		dB
Output IP3	LNA OFF, Bypass ON P <sub>in</sub> =+3 dBm/tone, Δf=5 MHz		+35		dBm
Control Voltage, V <sub>1</sub> , V <sub>2</sub>	V <sub>IH</sub>	1.17		V <sub>DD</sub>	V
	V <sub>IL</sub>	0		0.63	V
Current, I <sub>D</sub>	Bypass OFF		50		mA
	Bypass ON		5		mA
Switching Speed	LNA-Bypass (50% V <sub>ctrl</sub> to 10% RF)		137		ns
	Bypass-LNA(50% V <sub>ctrl</sub> to 90% RF)		354		ns
	LNA-OFF(50% V <sub>ctrl</sub> to 10% RF)		26		ns
	OFF-LNA(50% V <sub>ctrl</sub> to 90% RF)		55		ns
Thermal Resistance, θ <sub>jc</sub>	Channel to case		44		°C/W

1. Minimum specification listed is guaranteed by design. Not tested in production.
2. Input trace loss de-embedded from noise figure data.

## Control Truth Table

V <sub>BYP</sub>	V <sub>SD</sub>	State
0	0	LNA ON, Bypass OFF
0	1	LNA OFF, Bypass OFF
1	x	LNA OFF, Bypass ON

**QPL9097 Evaluation Board**



**Notes:**

1. A through line is included on the evaluation board to de-embed the board losses.
2. C14 and L2 are placed as close to device as possible. Any trace length between the device and components will add parasitics that will affect the tune.

**Bill of Material – QPL9097 Evaluation Board**

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise, Bypass LNA	Qorvo	QPL9097
C11,C12	20K ohm	RES, 0402, 1%, 1/10W	Various	
R1, R3,R4, C4	0 Ω	RES, 0402, +/-5%, 1/16W	Murata	
C1,5,8	18 pF	CAP, 0402, +/-5%, 50V	Murata	
C10	1000pF	CAP, 0402, 10%, 50V, X7R	Various	
C9	1.0uF	CAP, 0402, 10%, 10V, X5R	various	
C14	1.2 pF	CAP, 0402, 0.1pF, 50V, C0G	Murata	GJM1555C1H1R2BB01D
L2	2.4 nH	IND, 0402, 5%, WW	Coilcraft	0402CS-2N4XJLW
R5	75K	RES, 0402, 5%		

### Typical Performance (LNA Mode)

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$ ,  $V_1 = 0.63\text{V}$ ,  $V_2 = 0.63\text{V}$ ,  $I_D = 50\text{ mA}$ , Temp. = +25 °C.

Parameter	Typical Value				Units
Frequency	3.4	3.6	3.8	4.0	MHz
Gain	24	23	22	20	dB
Noise Figure	0.9	1.0	1.1	1.2	dB
Input Return Loss	14	12.5	12	11	dB
Output Return Loss	11	11	11.5	12	dB
OIP3 (Pout/tone=+0 dBm, $\Delta f = 1\text{ MHz}$ )	32.5	32.6	32.2	32.2	dBm
P1dB	15.5	15.6	15.5	15.4	dBm

### Typical Performance (Bypass Mode)

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$ ,  $V_1 = 1.17\text{V}$ ,  $V_2 = 1.17\text{V}$  or  $0.63\text{V}$ ,  $I_d = 5\text{ mA}$ , Temp. = +25 °C.

Parameter	Typical Value				Units
Frequency	3.4	3.6	3.8	4.0	MHz
Insertion Loss	2.2	2.0	2.0	2.0	dB
Input Return Loss	13.5	13	12.5	12	dB
Output Return Loss	14	16.5	17.5	17	dB
Input IP3 (Pin/tone=+3 dBm, $\Delta f = 1\text{ MHz}$ )	39.2	38.2	38	38	dBm

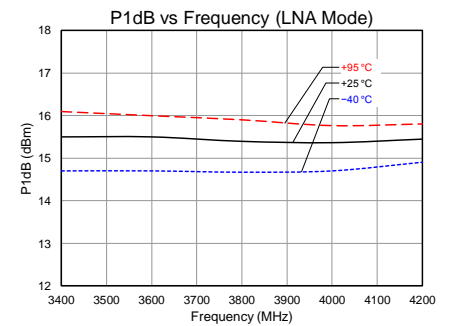
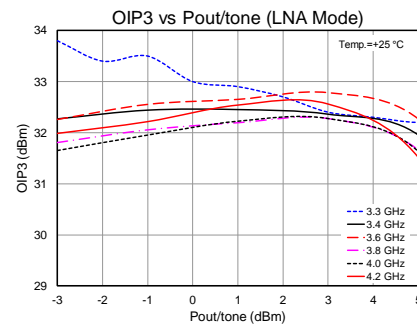
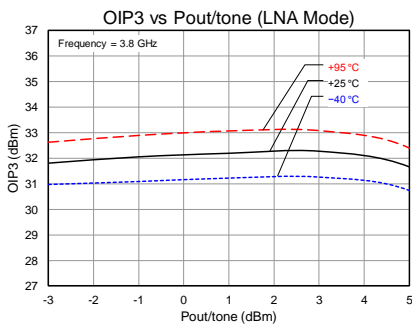
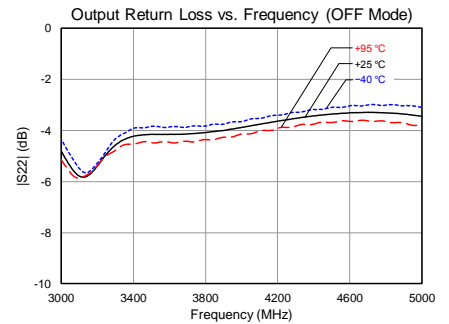
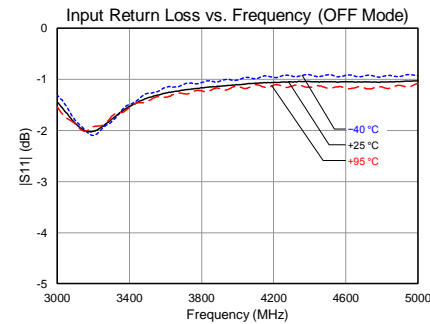
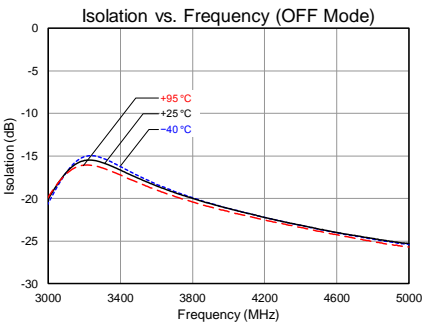
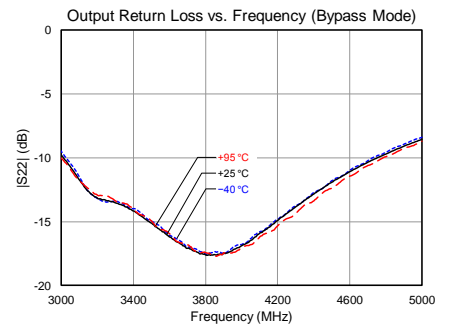
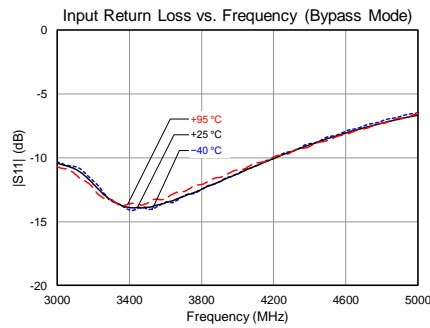
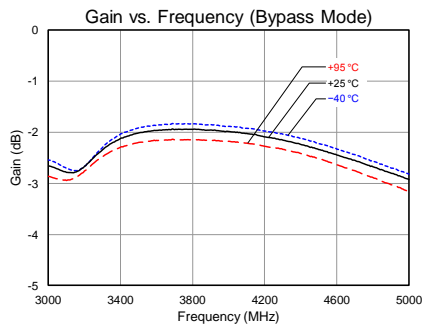
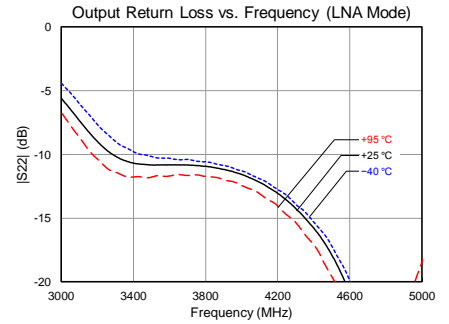
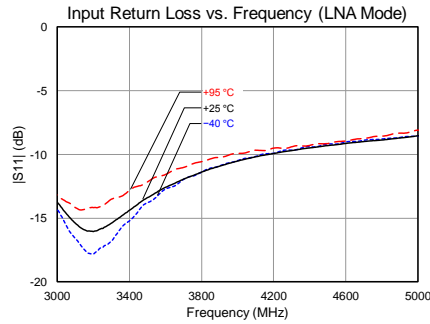
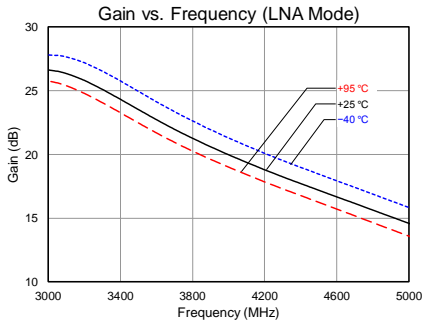
### Typical Performance (LNA OFF, Bypass OFF Mode)

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$ ,  $V_1 = 0.63\text{V}$ ,  $V_2 = 1.17\text{V}$ , Temp. = +25 °C.

Parameter	Typical Value				Units
Frequency	3.4	3.6	3.8	4.0	MHz
Isolation	16.5	18	20	22	dB

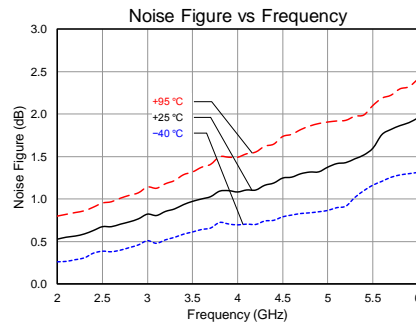
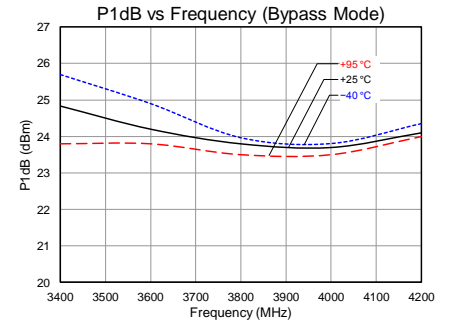
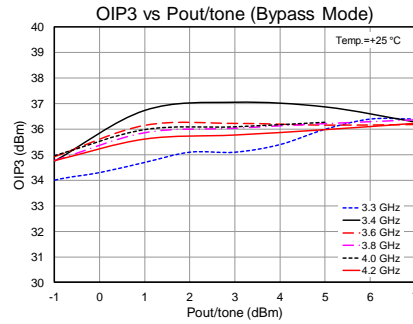
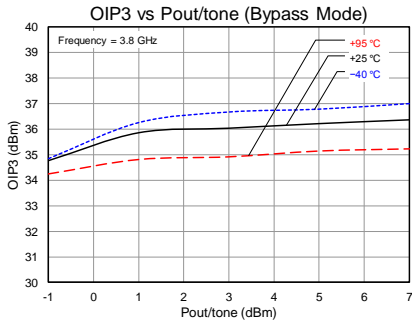
## Performance Plots

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$

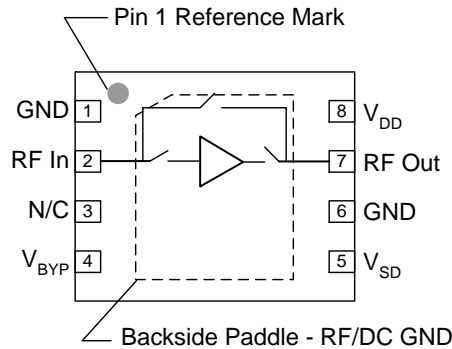


## Performance Plots Contd.

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$



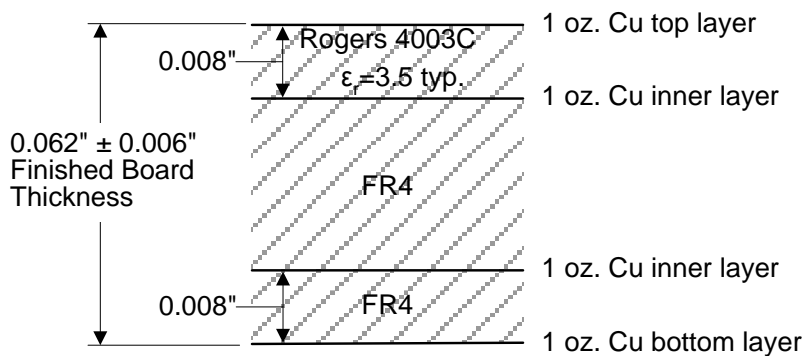
## Pin Configuration and Description



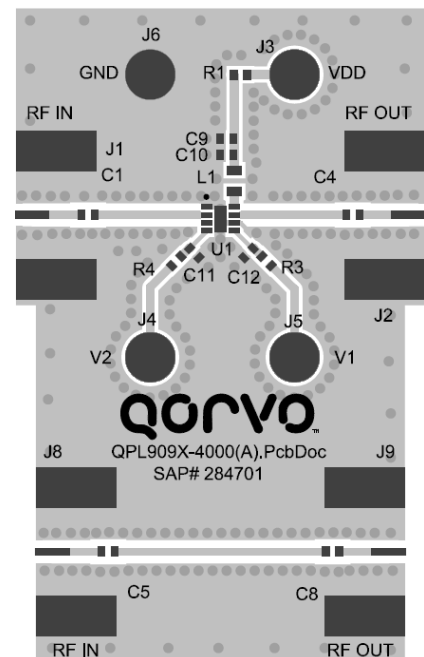
Pin No.	Label	Description
1, 6	GND	RF/DC Ground pin.
2	RFin	RF input pin. DC block required.
3	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
4	V <sub>BYP</sub>	Control pin for bypass mode. The LNA is automatically turned off when the bypass mode is activated. Refer to truth table on pg 2.
5	V <sub>SD</sub>	Control pin to disable the LNA. Refer to truth table on pg. 2.
7	RFout	RF output pin. DC block required.
8	V <sub>DD</sub>	Supply voltage pin. External choke and bypass capacitors needed.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

## Evaluation Board PCB Information

Qorvo PCB 284701 Material and Stack-up

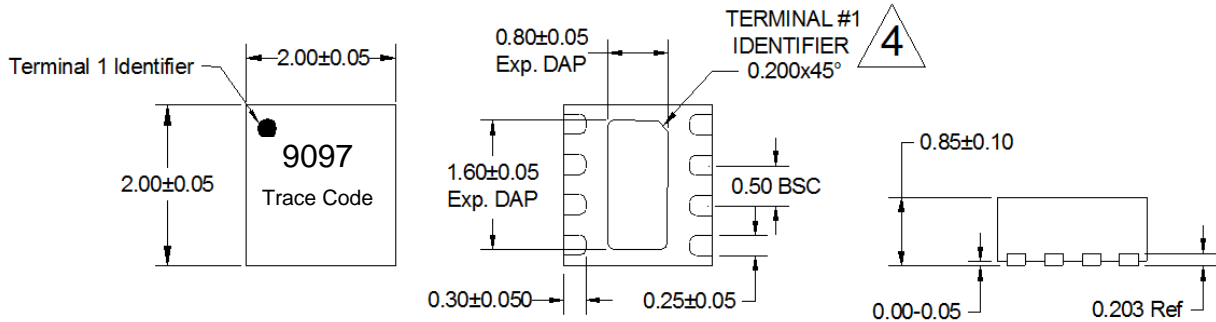


50 ohm line dimensions: width = 0.0182", spacing = 0.020"



Mechanical Information

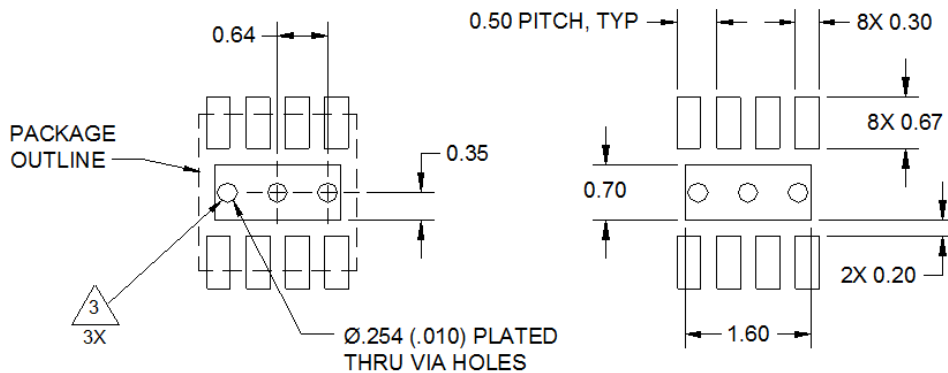
Package Marking and Dimensions



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a  $0.35$  mm ( $\#80/.0135$ " ) diameter bit for drilling via holes and a final plated thru diameter of  $0.25$  mm ( $0.10$ " ).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.



## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020



Caution!  
ESD-Sensitive Device

## Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.  
Solder profiles available upon request.

Contact plating: NiPdAu

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** 1-844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

For technical questions and application information: **Email:** [appsupport@qorvo.com](mailto:appsupport@qorvo.com)

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