Performance Improvements in Class D Audio Amplifiers Using Si824x Audio Drivers

1. Introduction

The Si8241/44 Audio Gate Drivers facilitate high-fidelity, Class D amplification while offering many other advantages over competing gate drivers. Based on Silicon Labs' proprietary CMOS isolation technology, these drivers offer the benefits of:

- Precise dead time adjustment for low total harmonic distortion (THD) and high system efficiency
- Individually-isolated drivers to facilitate simpler system topologies and external component flexibility
- High functional integration for small installed size and competitive cost

The gate driver IC is a critical system component because it influences both system architecture and system performance. The Si8241 Audio Gate Driver is a high-voltage driver capable of switching at frequencies up to 8 MHz to realize pre- or post-filter control. These devices have integrated precision dead time generators for low THD and high efficiency, as well as isolated output drivers that eliminate the need for input level shifting and facilitate the straightforward implementation of a two-state, half-bridge Class D amplifier.

This application note discusses the Silicon Labs Class D reference design, a stereo, two-state, half-bridge Class D amplifier that delivers 120 W per channel into 8 Ω or 150 W into 4 Ω. The reference design and demo board is available at www.silabs.com/isolation and uses the Si8241 Audio Gate Driver driven by a self-oscillating PWM modulator, as shown in Figure 1.

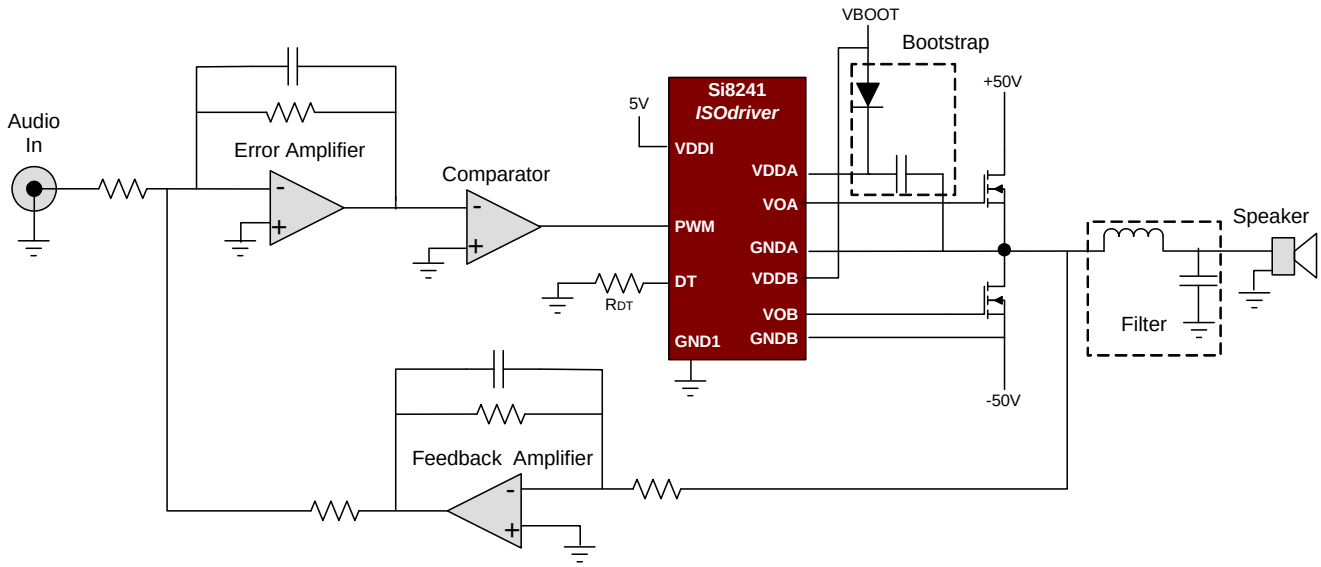


Figure 1. Si8241-Based Class D Amplifier Block Diagram

2. The Si8241 Audio Gate Driver

Every so often, a new IC is introduced that challenges the current technological hegemony. With features that make these products the perfect drivers for Class D amplification, the Silicon Labs Si8241/44 Audio Gate Drivers represent a new standard for the Class D amplifier industry. Key features are outlined in the following sections.

2.1. Programmable Dead Time

It is well documented that a precise dead time setting is critical in Class D amplifiers. During dead time, both the high-side and low-side MOSFETs are off. However, the low-side MOSFET body diode continues to conduct current, which manifests itself as output distortion. Too short a dead time causes shoot-through current that reduces system efficiency; too long a dead time increases THD, negatively impacting audio quality. While competing audio drivers typically have coarse, digital dead-time settings (i.e. 1 of *n* delay values), the Si8241/44 Audio Gate Drivers have a precise linear dead time setting that programs with a single external resistor. This feature provides the resolution necessary to precisely set dead time for optimal system performance. The Audio Gate Driver dead time equation is shown in Equation 1.

$$DT = 10R_{DT}$$

where Dead Time (DT) is in ns and R_{DT} is in kΩ

Equation 1. Audio Gate Driver Dead Time

Per Equation 1, the Silicon Labs Class D amplifier uses a 2 kΩ resistor to generate 20 ns of dead time. Changing this dead time value to 18 ns only requires changing the RDT to 1.8 kΩ (connected from the dead-time pin (DT) input to ground). This setting mechanism allows dead time to be incrementally increased or decreased in nanosecond increments, instead of tens of nanoseconds like competitive products.

2.2. Input/Output Isolation

Implementing a two-state, Class D amplifier can be difficult due to input level shifting requirements, and most available Class D drivers lack the capability to eliminate level shifting. Drivers that do eliminate level shifting have other peculiarities making them less-than-ideal for Class D operation (example: driver output ground terminal referenced to the –VBUS rail, requiring the input drive signal to be level-shifted). This is not the case with the Si8241 Audio Gate Driver where the isolation (i.e. level shift function) is implemented internally and is transparent to the user. The Si8241 Audio Gate Driver controlled by TTL input signal levels drives the outputs to ±VBUS, and only a single TTL PWM input signal is required to drive a two-state Class D amplifier.

2.3. High-Voltage Outputs

The Si8241 is capable of switching very high voltages (up to a 1,500 Vdc peak driver-to-driver differential voltage is possible) allowing a ±750 VBUS. For practical Class D amplifier designs, a voltage of ±100 Vdc can deliver an astounding 600 W of audio power into 8 Ω.

2.4. Output Current Drive

Class D amplifier switching MOSFETs should not be "slammed" on and off by excessively high current gate drivers. With its 0.5 A peak current outputs, the Si8241 Audio Gate Driver hits the sweet spot for Class D operation up to 400 W. Power levels beyond 400 W typically require larger MOSFETs and, consequently, more gate drive. For applications of this type, the Si8244 (4A) Audio Gate Driver provides the required added gate drive, where rise and fall times can be adjusted with a series gate resistor.

2.5. High-Frequency Operation

One of the best attributes of the Si8241 Audio Gate Driver is its 8 MHz maximum switching frequency, making it the fastest driver on the market for Class D operation. The Silicon Labs Class D reference design operates at approximately 500 kHz, and operating the amplifier between 500 kHz and 1 MHz dramatically reduces the high-frequency artifacts, resulting in a remarkably clean audio waveform.

3. Gate Drive Structure

Figure 2 illustrates the simplicity of the Si8241 driving a two-state, half-bridge Class D amplifier. The boot supply tied to D1 must be 12 V higher than the –50 V reference (–38 V) so that the MOSFETs each have a 12 V drive signal.

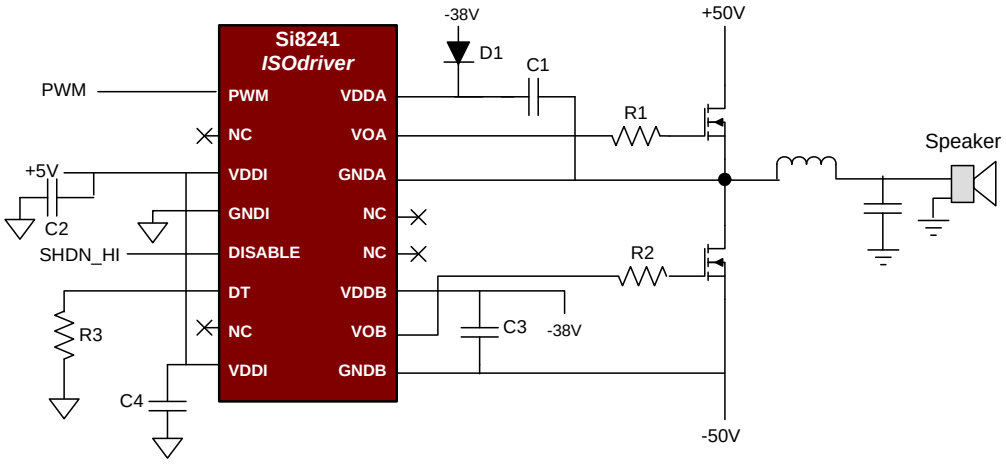


Figure 2. Si8241 Audio Gate Driver Gate Drive Circuit

4. Filter Inductor Selection

In early Class D amplifiers, the most common type of inductor used was a toroid of Type 2 iron material manufactured by Micrometals (Figure 3). This was because Type 2 material has a very low magnetic permeability (μ in Equation 2), slightly higher than an air core inductor, which has a linear BH curve and will not saturate.

$$\mu = \frac{B}{H}$$

Equation 2. Magnetic Permeability

However, when an iron core inductor operates further up on the BH curve, its permeability decreases with the falling slope of the BH curve and approaches zero as the core saturates. When this happens, there are no more iron particles to align within the core, and the inductance approaches zero.

Recently, a number of manufacturers developed inductors specifically for Class D amplification, such as Sagami Elec. Co., whose inductors are used in the Silicon Labs Class D reference design. The inductance value of these devices does not decrease with current as happens in most inductors. Instead, it remains relatively flat over the range of interest and is a good choice for Class D amplifier applications.

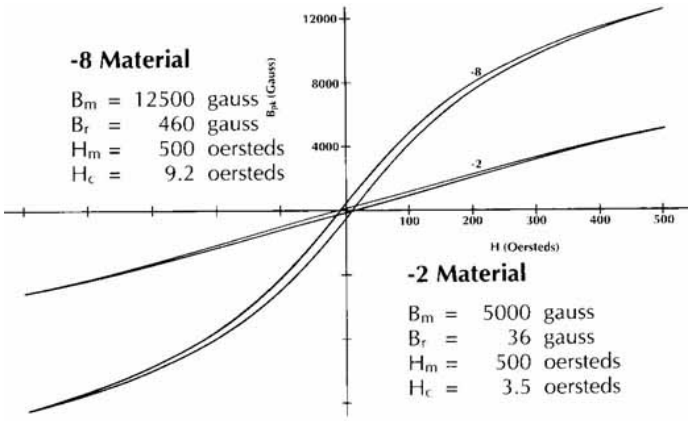


Figure 3. Micrometal Inductor BH Plot

5. Reference Design Board Architecture

The Silicon Labs Class D reference design architecture uses a phase-shift, self-oscillating modulation approach capable of achieving a far greater signal-to-noise ratio than that of a clock-driven amplifier. This self-oscillating implementation eliminates the circuitry necessary to generate the triangle waveform (see "8. Self Oscillation" on page 6 for details). To keep the circuit as simple as possible, a two-state, half-bridge is implemented and demonstrates the benefits of using the Si8241 Audio Gate Driver.

5.1. Control Theory Basics

Looking at the equation derivation in the frequency domain, Figure 4 shows input signal R(s), which is the Laplace transform of the time domain regulation input signal R(t). C(s) is the Laplace transform of the time-domain-controlled output signal C(t), where s = jω.

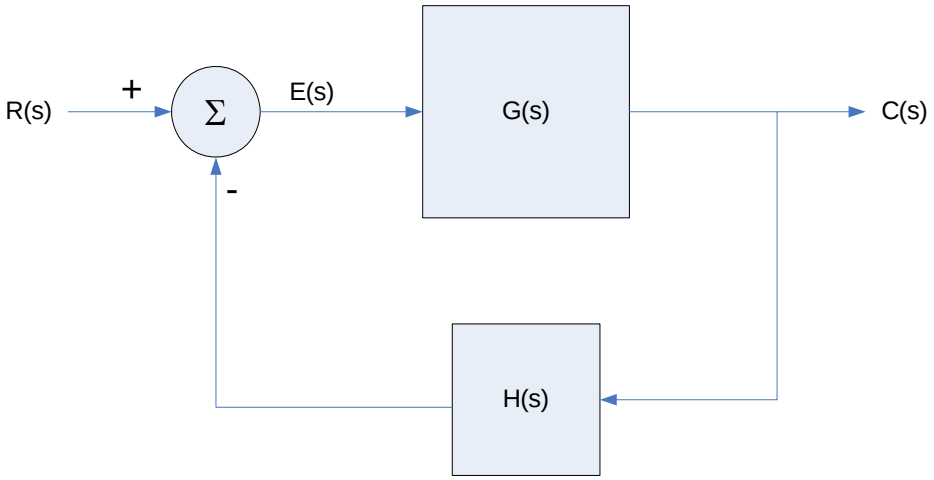


Figure 4. First Order Control Loop Model

$$E(s) = R(s) - C(s)H(s)$$

Equation 3.

$$C(s) = E(s)G(s)$$

Equation 4.

Substituting C(s) from Equation 4 into Equation 1, and solving for E(s)/R(s) yields:

$$\frac{E(s)}{R(s)} = \frac{1}{1 + G(s)H(s)}$$

Equation 5.

Similarly, substituting E(s) from Equation 4 into Equation 3 and solving for C(s)/R(s) yields:

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

Equation 6.

Examining these equations within the context of a Class D control loop, G(s) is the forward transfer function; H(s) is the feedback transfer function, and E(s) is the error signal (i.e., the difference between the input and output).

6. Closed Loop Transfer Function

The closed loop transfer function is defined as the ratio of the controlled variable to the input variable. The controlled variables are the speaker terminals, and the input variable is the MP3 player input, the CD input, or some other input source connected to the amplifier. Therefore, the equation for the closed-loop transfer function is given by Equation 7.

$$\text{Closed\_Loop\_Transfer\_Function} = \frac{G(s)}{1 + G(s)H(s)}$$

Equation 7. Closed Loop Transfer Function

The closed loop gain describes how the output responds over the audio bandwidth to the input regulation signal. It is understood that the output should have a specific closed loop gain with respect to the input regulation signal, and that gain should be as flat as possible over the audio bandwidth. The inductor between the controlled variable and the speaker terminals plays a crucial role in the performance of the amplifier as previously discussed. The closed loop gain of the Silicon Labs Class D reference design is implemented such that approximately 1 Vpp input will yield full output power into an 8 Ω load.

7. Open Loop Transfer Function

The open-loop transfer function is obtained by breaking the loop at some arbitrary point and traversing the entire loop back to the same point. When H(s) = 1, the open loop and the forward transfer functions are identical. Therefore, the open loop transfer function is given by Equation 8.

$$\text{Open\_Loop\_Transfer\_Function} = G(s)H(s)$$

Equation 8.

The open loop transfer function determines whether the loop is stable, as well as determining what the overall open loop gain of the amplifier will be over the audio bandwidth. The higher the open loop gain, the lower the error signal and, therefore, the more easily the control loop can keep the output following the input command. Some early Class D amplifier designs used an integrator for the error amplifier. This produced high gain at low frequencies but low gain at high frequencies due to the pole produced by the integrator. This caused the THD to increase dramatically above 5 kHz, destroying the high-frequency response of the amplifier. A better solution is to keep the open loop gain constant and as high as possible throughout the audio bandwidth. This should yield a constant THD response, and, indeed, it does, as will be shown in the performance curves in "13. Performance" on page 8.

Care should be taken in designing the open loop response of the amplifier. The three key elements are the bandwidth, phase margin, and gain margin. In designing a Class D amplifier, the target is to have 45° of phase margin with a bandwidth of approximately half the switching frequency. The control loop cannot compensate for the LC filter response since the filter is outside of the loop. The entire LC filter is designed as a Bessel function with a load resistance of 6 Ω. Therefore, the filter is slightly underdamped at 8 Ω and slightly overdamped at 4 Ω. This can be seen by placing a 100 mVpp square wave into the input and looking at the output response with an 8 Ω load and a 4 Ω load.

8. Self Oscillation

The amplifier is self-oscillating, enabling its signal-to-noise ratio to far exceed that of a clock driven system. The main mechanism for this is the delta-sigma effect of shifting in-band noise to a much higher out-of-band frequency. The amplifier is a basic, phase-shift type, which has significant advantages over an amplifier running as a hysteretic oscillator. There is a pole in the forward path G(s) and a pole in the feedback path H(s). The 180 ° phase shift, coupled with the transport delay, yields an oscillation frequency of nearly 500 kHz. The transport delay is given by Equation 9, where “t” is the delay of the comparator plus the Si8241.

$$T_{Delay} = e^{-tj\omega}$$

Equation 9.

Taking into consideration the delay tolerances of the comparator and Si8241 driver, the total delay can range from 90 ns to 140 ns. The frequency of oscillation occurs at the point when the open loop transfer function phase response times the transport delay is equal to –180 °.

$$F_{OSC} \text{ occurs when: } Arg(G(s)H(s)\ e^{-ts}) = -180°$$

Equation 10.

The frequency of oscillation is set by capacitors in each audio channel where reducing capacitance value increases oscillation frequency. Tight tolerance capacitors are used to keep the channel frequencies as close to each other as possible.

9. Drive Voltage

The upper and lower gate drive voltages can be generated by a linear regulator (the regulator used in the Silicon Labs Class D reference design is a high-voltage regulator able to withstand a 125 V input). When referenced to the negative supply, the regulator generates a low-side MOSFET drive voltage of –38 V (i.e., 12 V of gate drive with respect to the source). Likewise, the bootstrap capacitor charges to 12 V when the phase lead swings to the negative rail. The only downside to using a linear regulator is the power dissipation, which is directly-proportional to the frequency of the switching amplifier and the bus voltage. Alternatively, a small, high-frequency switching regulator may be used to reduce the power dissipation of the MOSFET gate drive supply, but this can add unwanted system noise.

10. Overcurrent Protection

The Silicon Labs Class D reference design has an overcurrent protection circuit consisting of a low-power comparator floating off the upper and lower bus voltages. The upper rail circuit is shown in Figure 5 and is duplicated on the lower rail. It monitors the current flowing through the 0.005 Ω resistor (RSENSE) (Zener diode D1 and resistor R5 supply power to the comparator and the Silicon Labs Si8410 digital isolator). The Si8410 performs the necessary level shifting to interface to the shutdown circuitry.

The circuit is set to trip at roughly a 20 A fault, usually caused by a short-circuit across the speaker terminals or a large overdrive signal at the audio inputs. Note that the upper and lower overcurrent circuits are ORd together through a pair of diodes and sent to the reset control circuit. The normally low Si8410 A1 input is driven high upon detection of an overcurrent condition and asserts the SHUTDOWN signal, forcing the reset controller to assert a reset signal, momentarily halting amplifier operation. The reset control circuit attempts restart after one second, and, if the fault is still present, again cycles reset in "hiccup" mode with a frequency of one second. This process continues until the fault is removed.

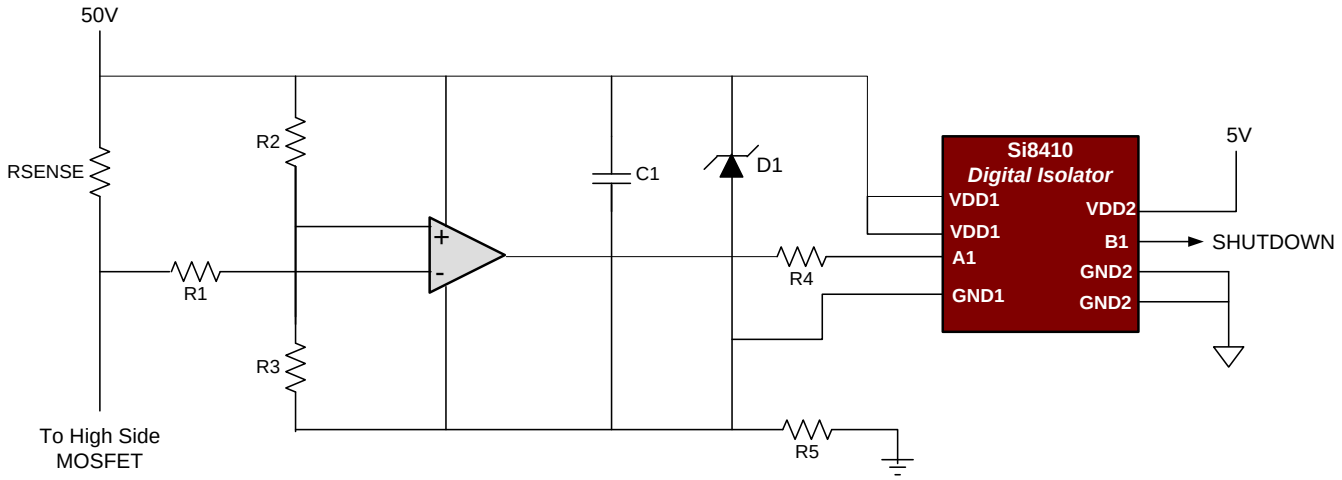


Figure 5. Overcurrent Protection Circuit

11. Undervoltage Protection

The undervoltage protection comparator monitors the positive bus voltage and releases the undervoltage lockout when the voltage is above 37 V, and the amplifier starts-up after a one-second delay. Note that the red LED remains lit when the amplifier is in shutdown mode and turns off when the amplifier is enabled.

12. Other Features

A protection circuit jumper option is included that allows the amplifier to be manually shut down. This jumper can be replaced with a switch or other control circuit, allowing the amplifier to be muted. The one-second undervoltage lockout delay allows the opamps and comparator to settle before the shutdown circuit is released, thereby preventing speaker pops. There are also individual jumper options on each channel that allow the user to enable or disable each channel independently to aid in system performance evaluation.

13. Performance

The Silicon Labs Class D reference design board was tested for THD + N, SNR, DFD and IFD with an Audio Precision analyzer. Power efficiency was also measured using conventional lab equipment. The following graphs show the results of this testing. For more performance data, please visit www.silabs.com/isolation. Figure 6 shows a 1 kHz sine wave input signal swept over the entire power range of the amplifier from 1 W to 120 W. Note the maximum THD+N is 0.06%, occurring at 1 W.

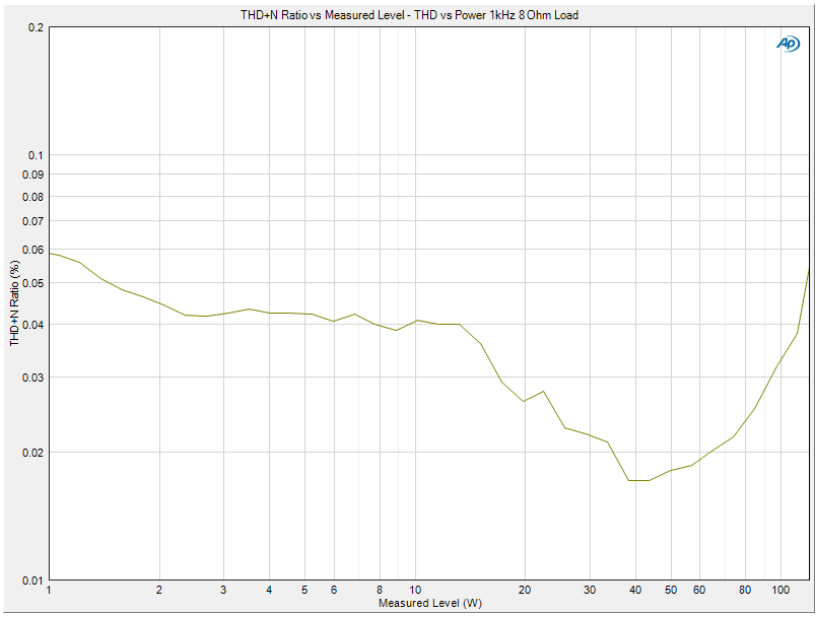


Figure 6. 1 kHz Sweep Across Amplifier Power Range

Figure 7 shows an SNR measurement amplifier of approximately 92 dB. An equivalent clock-driven amplifier would likely produce an SNR in the range of 70 to 80 dB.

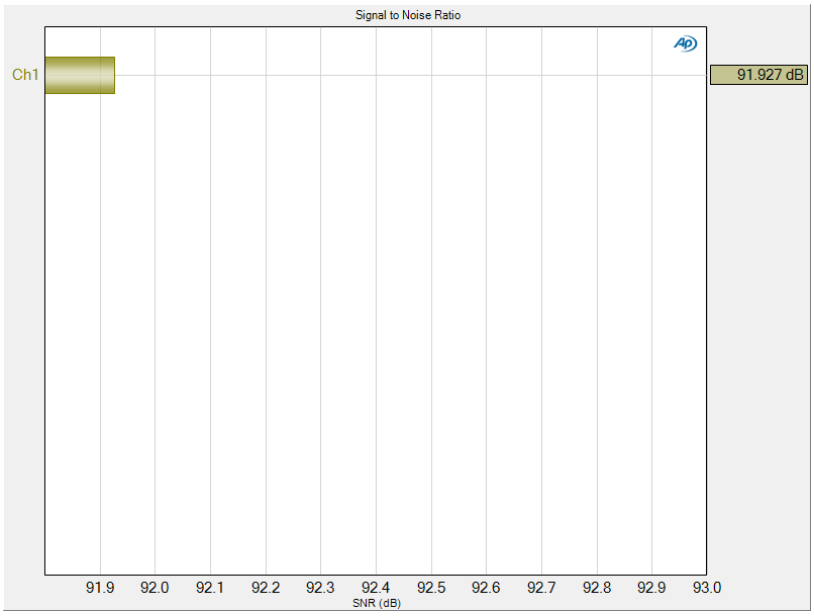


Figure 7. SNR Measurement

Figure 8 shows a dynamic range measurement, while Figure 9 shows the Difference Frequency Distortion (DFD) plot. DFD is a technique for measuring intermodulation distortion (IMD); note that the two tones at 18 kHz and 19 kHz cause a difference frequency of 1 kHz. The sidebands generated are located at 17 kHz and 20 kHz and, ideally, should be as low as possible (IMD levels are about –80 dB in this plot). Figure 10 is identical to Figure 9, but with the DFD Ratio in percent (%) instead of dB. Figure 11 shows amplifier efficiency.

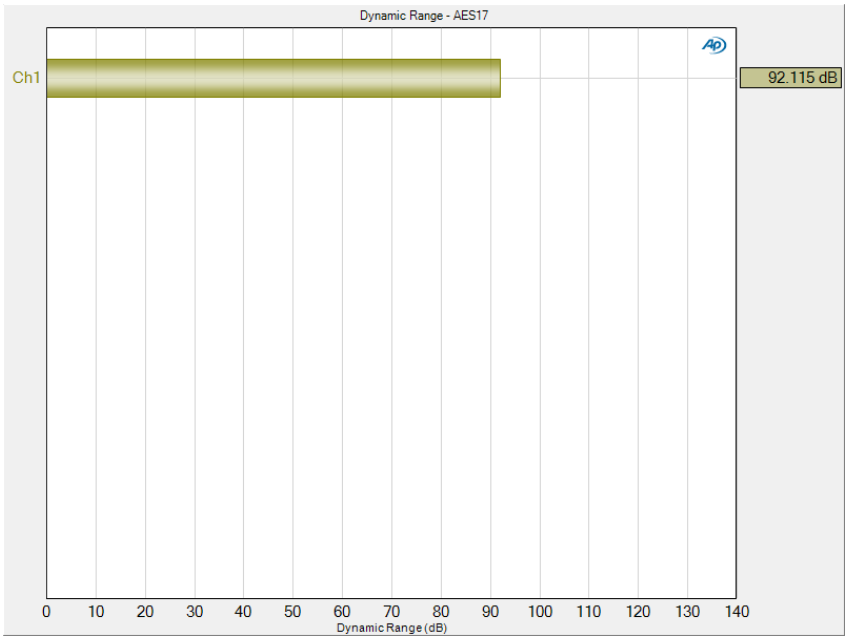


Figure 8. Dynamic Range Measurement

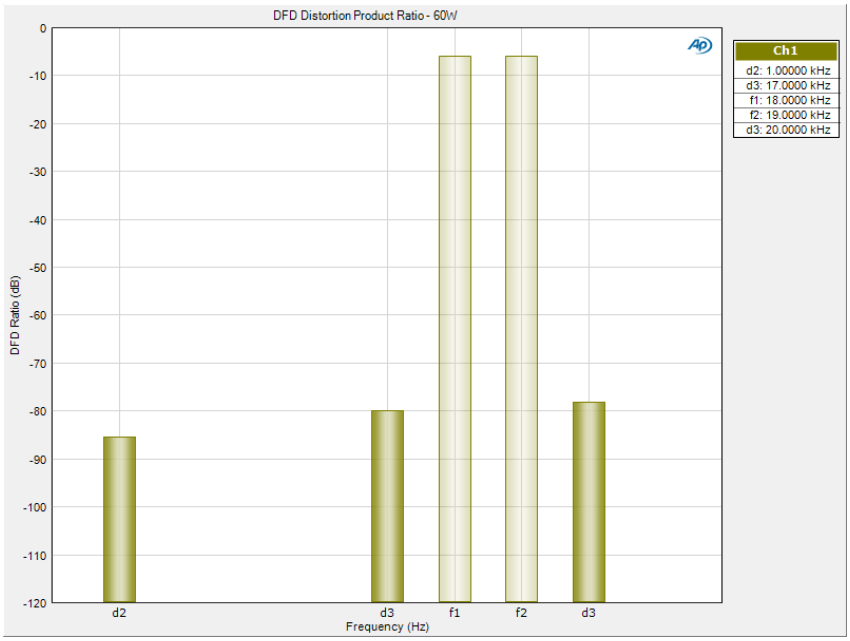


Figure 9. IMD Plot (db)

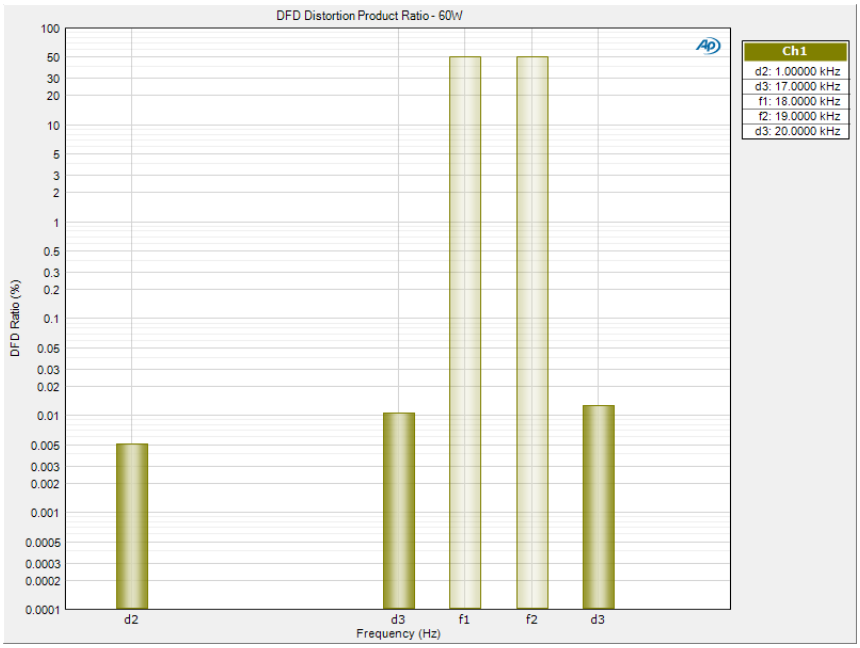


Figure 10. IMD Plot (%)

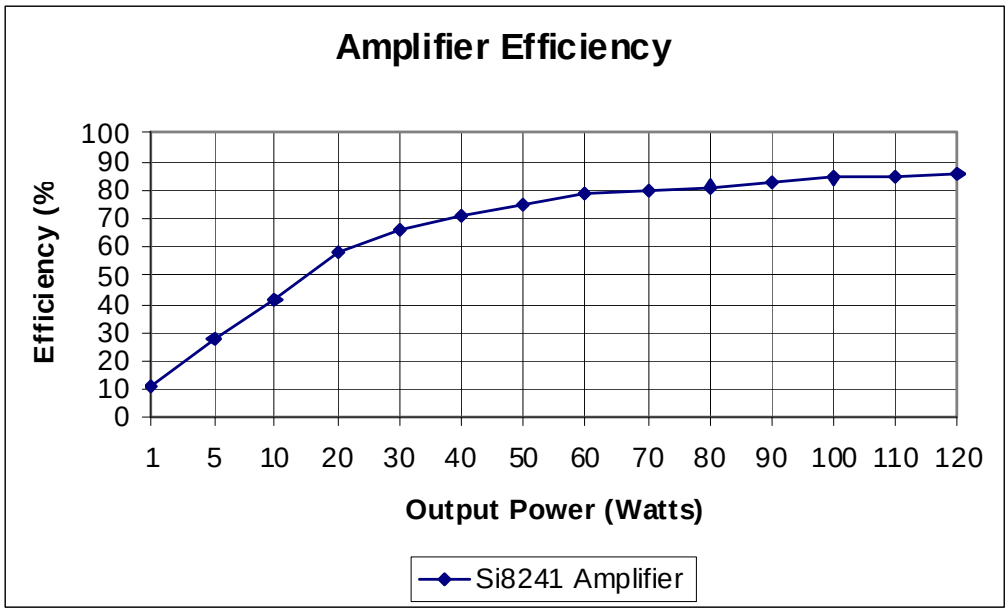


Figure 11. Amplifier Efficiency from Zero to Full Load

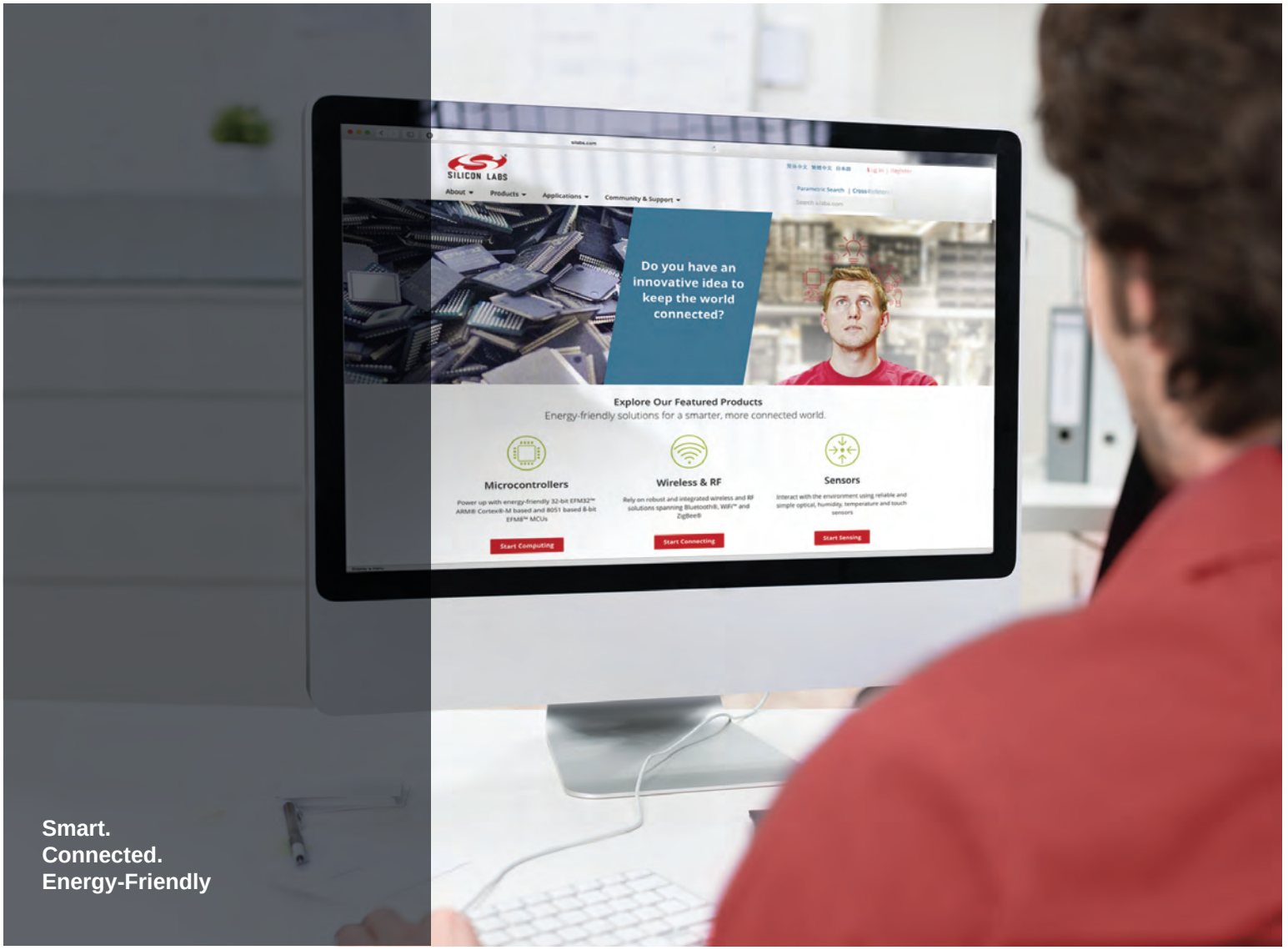
14. Summary

Class D amplification offers advantages far above traditional analog amplifiers, including lower total harmonic distortion (THD), smaller size, higher power efficiency, and lower cost. The gate driver IC can impact both system architecture and performance.

Silicon Labs Si824x Audio Gate Drivers offer benefits not available in competitive driver solutions. These benefits include high resolution dead time setting for the lowest possible THD and best efficiency, no input signal level shift circuits to complicate design and increase component count, and isolated output drivers for easy two-state switcher implementation.

15. References

- Simple Self-Oscillating Class D Amplifier with Full Output Filter Control - Putzeys, AES convention paper, 2005 May 28
- Introduction to Control Systems Design, Eveleigh - McGraw-Hill, 1972



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