Octal E1 Framer

FEATURES

- Monolithic single-chip device that integrates eight datacom E1 framers and transmitters for terminating duplex E1 signals.
- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals and is consistent with ITU-T G.706 specifications.
- Extracts/inserts up to three HDLC links from/to arbitrary time slots to support the D-channel for ISDN Primary Rate Interfaces, the datalink in the National Use Bits and the C-channels for V5.1/ V5.2 interfaces as per ITU-T G.964, ITU-T G.965, ETS 300-324-1, and ETS 300-347-1.
- Provides an optional backplane interface which is compatible with Mitel ST®-bus, AT&T CHI® and MVIP PCM backplanes, supporting data rates of 2.048 Mbit/s and 8.192 Mbit/s.
- Supports transfer of PCM data to and from 2.048 Mbit/s backplane buses.
- Supports fractional E1 backplane interface.
- Provides jitter attenuation in both the receive and transmit directions.
- Provides per-timeslot line loopback and per-link diagnostic and line loopbacks.
- Provides signaling extraction and insertion on a per-channel basis.
- Provides a Pseudo Random Binary Sequence (PRBS) generator and detector which may be configured for insertion/detection on a per-timeslot or multiple timeslot basis.
- Software-compatible with the PM6341 E1XC Single E1 Transceiver, the PM6344 EQUAD Quad E1 Framer, the PM4388 TOCTL Octal T1 Framer, and PM4351 COMET Combined E1/T1 Transceiver.
- Pin-compatible with the PM4388 TOCTL with a seamless interface to the PM4314 QDSX quad line interface unit.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3 V CMOS technology with 5 V tolerant inputs.
- Supports standard 5-signal P1149.1 JTAG boundary scan.
- Provides a -40 to +85° industrial temperature operating range.
- Available in a rectangular 128-pin PQFP (14 by 20 mm) package.

RECEIVE SECTION

- Red and AIS alarm detection and integration are done according to ITU-T Q.516 specifications.
- Can be programmed to generate an interrupt on change of signaling state.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Accumulators are provided for counting ESF CRC-6 errors, framing bit errors, Far-End Block Errors (FEBEs) and PRBS bit errors.
- Provides a 2-frame buffer for jitter and wander attenuation.

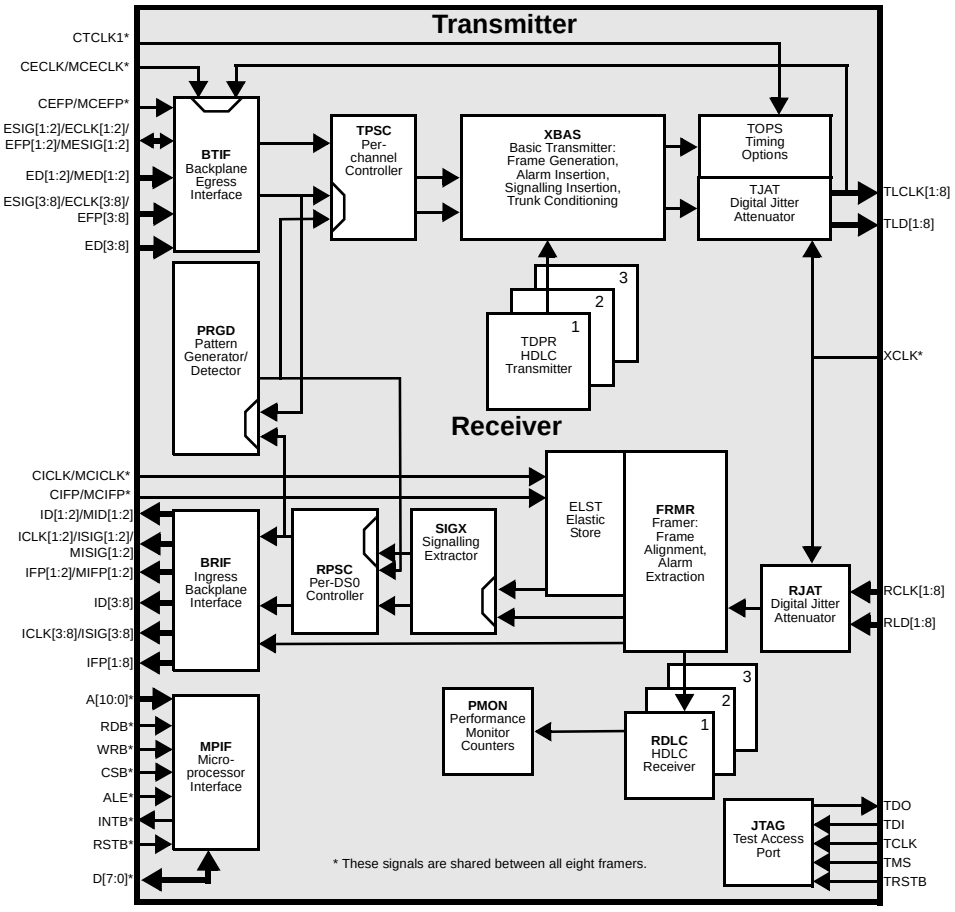
TRANSMIT SECTION

- Transmits G.704 basic and CRC-4 multiframe formatted signals with support for unframed mode.
- May be timed to its associated receive clock (loop timing) or may derive its timing from a common egress clock or a common transmit clock; the transmit line clock may be synthesized from an $n \times 8$kHz reference.
- Provides a digital PLL for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and transmit rate conversion.

APPLICATIONS

- High density Internet E1 interfaces for multiplexers, switches, routers, and digital modems
- Frame Relay Switches and Access Devices (FRADS)
- Digital Access and Cross-Connect Systems (DACS)
- SDH Add/Drop Multiplexers (ADMs)

BLOCK DIAGRAM



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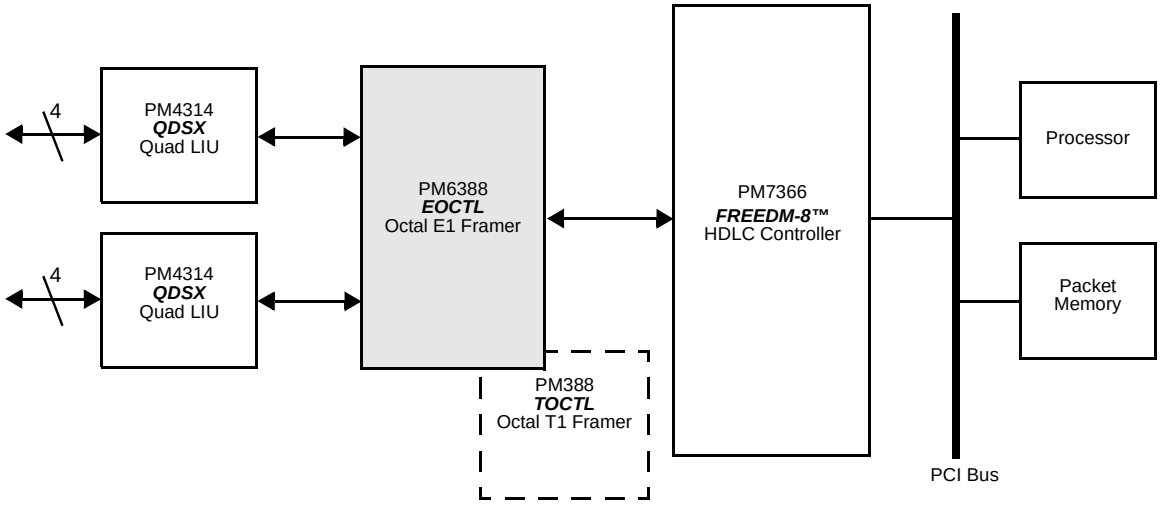
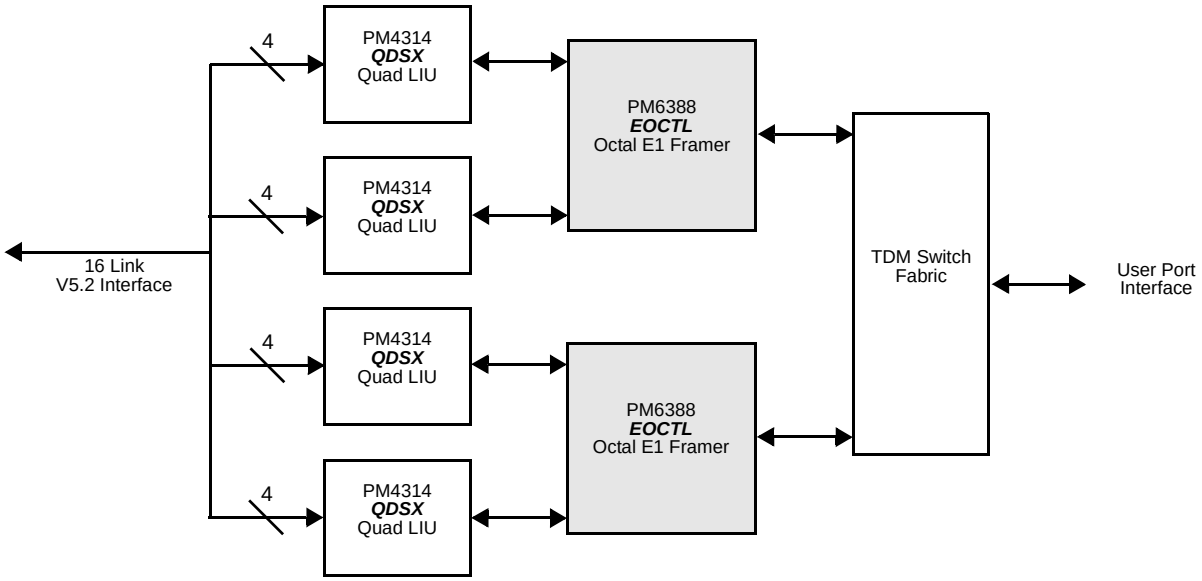
TYPICAL APPLICATIONS

EIGHT-CHANNEL T1/E1 PORT CARD ADAPTER USING PIN-COMPATIBLE TOCTL AND EOCTL



SIXTEEN-PORT V5.2 INTERFACE USING TWO EOCTLS



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