NX5P1100

Logic controlled high-side power switch

Rev. 1 — 21 March 2014 Product data sheet

1. General description

The NX5P1100 is an advanced power switch and ESD-protection device for USB OTG applications. It includes under voltage and over voltage lockout, over-current, over-temperature, reverse bias and in-rush current protection circuits. These circuits are designed to isolate a VBUS OTG voltage source from a VBUS interface pin automatically when a fault condition occurs. The device features two power switch terminals, one input (VINT) and one output (VBUS). It has a current limit input (ILIM) for defining the over-current and in-rush current limit. A voltage detect output (VDET) is used to determine when VINT is in the correct voltage range. An open-drain fault output ($\overline{\text{FAULT}}$) indicates when a fault condition has occurred, and an enable input (EN) controls the state of the switch. When EN is set LOW the device enters a low-power mode, disabling all protection circuits except the undervoltage lockout. The low-power mode can be entered at anytime unless the over temperature protection circuit has been triggered.

Designed for operation from 3 V to 5.5 V, it is used in power domain isolation applications to protect from out of range operation. The enable input includes integrated logic level translation making the device compatible with lower voltage processors and controllers.

2. Features and benefits

- Wide supply voltage range from 3 V to 5.5 V
- 30 V tolerant on VBUS
- I_{SW} maximum 1 A continuous current
- Very low ON resistance: 100 mΩ (maximum) at a supply voltage of 4.0 V
- Low-power mode (ground current 20 μA typical)
- 1.8 V control logic
- Soft start turn-on slew rate
- Protection circuitry
  - Over-temperature protection
  - Over-current protection with low current output mode
  - Reverse bias current/Back drive protection
  - Overvoltage lockout
  - Undervoltage lockout
  - Analog voltage limited VBUS monitor path
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JDS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-011 category C6 exceeds 1 kV
  - IEC61000-4-2 contact discharge exceeds 8 kV for pins VBUS, D–, D+ and ID
- Specified from –40 °C to +85 °C

3. Applications

- USB OTG applications

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX5P1100UK	–40 °C to +85 °C	WLCSP12	wafer level chip-scale package; 12 bumps; 1.36 x 1.66 x 0.51 mm, 0.4 mm pitch (Backside coating included)	NX5P1100

5. Marking

Table 2. Marking codes

Type number	Marking code
NX5P1100UK	NX5PB

6. Functional diagram

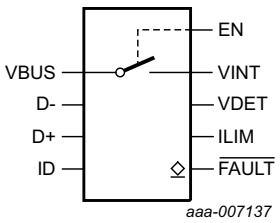


Fig 1. Logic symbol

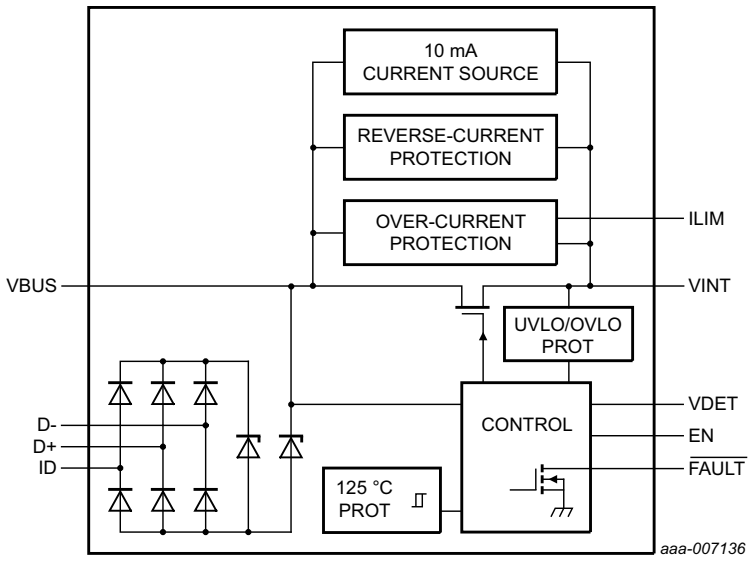


Fig 2. Logic diagram (simplified schematic)

7. Pinning information

7.1 Pinning

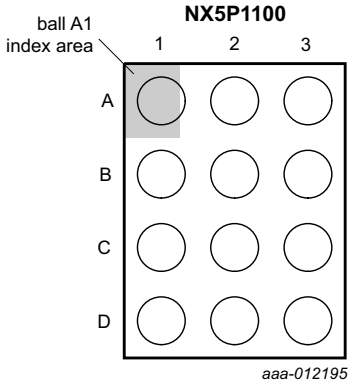


Fig 3. Pin configuration WLCSP12 package

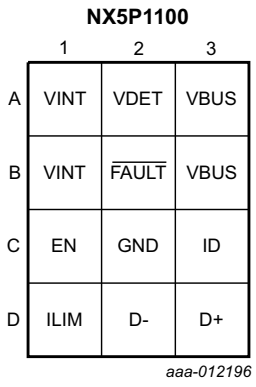


Fig 4. Ball mapping for WLCSP12

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VINT	A1, B1	internal circuitry voltage I
VBUS	A3, B3	external connector voltage O
EN	C1	enable input (active HIGH) I
ILIM	D1	current limiter I/O

Table 3. Pin description *...continued*

Symbol	Pin	Description
VDET	A2	VBUS voltage level indicator O
$\overline{\text{FAULT}}$	B2	fault condition indicator (open-drain; active LOW)
GND	C2	ground (0 V)
D-	D2	ESD-protection I/O
D+	D3	ESD-protection I/O
ID	C3	ESD-protection I/O

8. Functional description

Table 4. Function table[1]

EN	VINT	VBUS	$\overline{\text{FAULT}}$	Operation mode
X	0 V	Z	L	no supply
X	0 V	< 30 V	Z	disabled; switch open
X	< 3.2 V	Z	L	undervoltage lockout; switch open
H	> 5.5 V	Z	L	overvoltage lockout; switch open
H	3.2 V to 5.5 V	Z	L	over-temperature; switch open
L	3.2 V to 5.5 V	Z	Z	disabled; switch open
H	3.2 V to 5.5 V	VBUS = VINT	Z	enabled; switch closed; active
H	3.2 V to 5.5 V	0 V to VINT	L	over-current; switch open; constant current on VBUS
H	3.2 V to 5.5 V	0 V to VINT	L	when ILIM is connected to GND, VBUS is supplied with 10 mA current source
H	3.2 V to 5.5 V	VINT + 30 mV < VBUS < VINT + 0.45 V (> 4 ms)	L	reverse bias current/back drive; switch open
H	3.2 V to 5.5 V	VBUS > VINT + 0.45 V	L	reverse bias current/back drive; switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state, X = Don't care.

Table 5. Function table VDET versus VBUS

VBUS	VDET	Operation mode
3 V < VBUS < 30 V	1.5 < VDET < 5.5 V	VDET detects VBUS voltage; See Figure 22.

8.1 EN input

A LOW on EN disables the N-channel MOSFET and the device enters low-power mode. In low-power mode, all protection circuits are disabled except for the undervoltage lockout circuit. A HIGH on EN, enables the protection circuits and then enables the N-channel MOSFET.

8.2 $\overline{\text{FAULT}}$ output

The $\overline{\text{FAULT}}$ output is an open-drain output that requires an external pull-up resistor. If any of the UVLO, OVLO, RCP, OCP or OTP circuits are activated the $\overline{\text{FAULT}}$ output is set LOW. A LOW indicates that a fault has occurred. The $\overline{\text{FAULT}}$ output returns to the high impedance state automatically once the fault condition is removed.

8.3 VDET output

VDET is an analog output that allows a controller to monitor the voltage level on VBUS.

8.4 Undervoltage lockout (UVLO)

When VINT < 3.2 V, the UVLO circuit is triggered. It disables the N-channel MOSFET sets the $\overline{\text{FAULT}}$ output LOW and the device enters low-power mode. Once VINT > 3.2 V, the EN pin controls the state of the N-channel MOSFET. The UVLO circuit remains active in low-power mode.

8.5 Overvoltage lockout (OVLO)

When EN is HIGH and VINT > 5.75 V, the OVLO circuit is triggered. It disables the N-channel MOSFET and sets the FAULT output LOW. The OVLO circuit is disabled in low-power mode and does not influence the FAULT output state. If the OVLO circuit is triggered, setting the EN pin LOW returns the device to low-power mode.

8.6 Over-current protection (OCP)

If either of these two conditions occur for longer than 8 ms, the OCP circuit is triggered.

1. Current through the N-channel MOSFET exceeds I_{trig}.
2. VBUS < VINT − 200 mV.

During the 8 ms trigger delay, the maximum current is clamped at I_{ocp}. The OCP disables the N-channel MOSFET; supplies VBUS from the 10 mA current source (I_O), and sets $\overline{\text{FAULT}}$ LOW. When VINT > VBUS > VINT - 200 mV for 20 μs, the OCP circuit is disabled. EN controls the state of the N-channel MOSFET, the 10 mA current source is disconnected and $\overline{\text{FAULT}}$ is set high impedance. If the OCP circuit is active, setting the EN pin LOW returns the device to low-power mode. (see Figure 23, Figure 24, Figure 25, Figure 26)

8.7 ILIM

The OCP trigger value I_{trig}, is set using an external resistor R_{ILIM} connected to the ILIM pin (see Figure 6). When EN is HIGH and ILIM is grounded, VBUS is supplied by the 10 mA current source and $\overline{\text{FAULT}}$ is set LOW.

8.8 Over-temperature protection (OTP)

When EN is HIGH, if the device temperature exceeds 125 °C, the OTP circuit is triggered. It disables the N-channel MOSFET and sets $\overline{\text{FAULT}}$ LOW. Any transition on EN has no effect. Once the device temperature decreases to below 115 °C the device returns to the defined state. The OTP circuit is disabled in low-power mode. If the OTP circuit is active, setting the EN pin LOW does not return the device to low-power mode.

8.9 Reverse bias current/back drive protection

If either of these two conditions occur, the RCP circuit is triggered.

1. (VINT + 30 mV) < VBUS < (VINT + 0.45 V) for longer than 4 ms.
2. VBUS > (VINT + 0.45 V)

It disables the N-channel MOSFET and sets $\overline{\text{FAULT}}$ LOW. Once VBUS < VINT for longer than 4 ms the device returns to the defined state. If the RCP circuit is active, setting the EN pin LOW returns the device to low-power mode.

8.10 In-rush current protection

The N-channel MOSFET can be enabled via the EN pin or via a recovering fault condition. When enabled, the in-rush current protection circuit limits the current while VBUS increases to VINT − 200 mV. The resistor connected to ILIM determines the current limit. The in-rush current protection circuit is disabled in low-power mode.

9. Application diagram

The NX5P1100 typically connects a voltage source on VINT to the VBUS of a USB connector supporting USB3 OTG in a portable, battery operated device. The external resistor R_{ILIM} sets the maximum current limit threshold. The $\overline{\text{FAULT}}$ signal requires an external pull-up resistor.

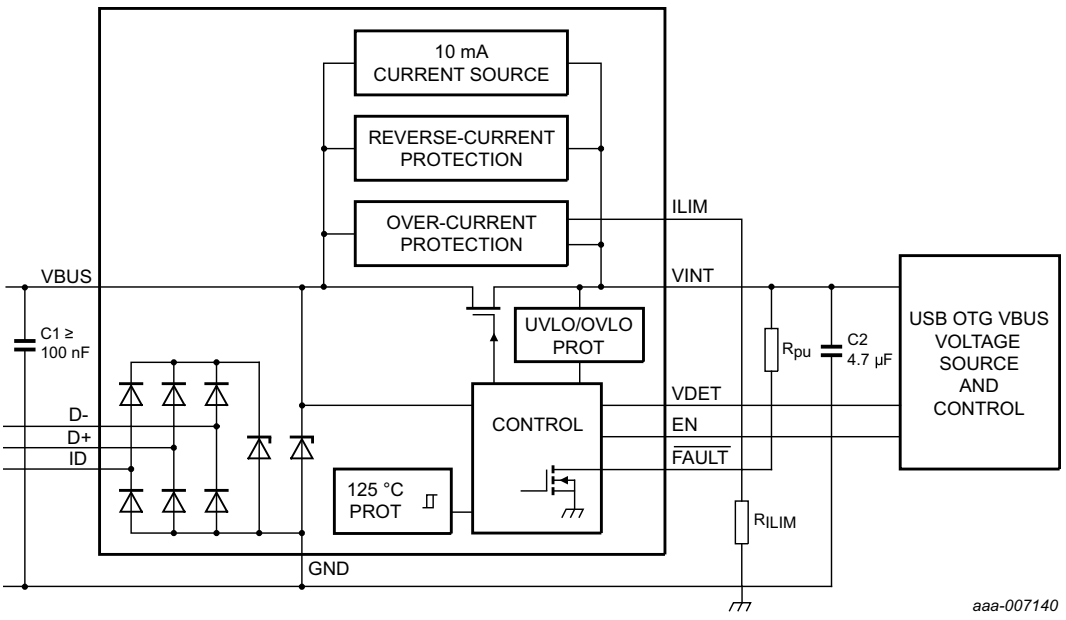


Fig 5. NX5P1100 application diagram

10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUS	[1]	−0.5	+32	V
		VINT	[1]	−0.5	+6.0	V
		EN, ILIM	[2]	−0.5	VINT + 0.5	V
		D-, D+, ID	[1]	−0.5	+6.0	V
V_O	output voltage	$\overline{FAULT}$		−0.5	+6.0	V
I_{IK}	input clamping current	EN: V_I < −0.5 V		−50	-	mA
I_{SK}	switch clamping current	VBUS; VINT; V_I < −0.5 V		−50	-	mA
I_{SW}	switch current	T_{amb} = 85 °C		-	±1000	mA
$T_{j(max)}$	maximum junction temperature			−40	+125	°C
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation		[3]	-	100	mW

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed at lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two layer PCB.

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VINT	3.0	5.5	V
		EN, ILIM	0	VINT	V
V_O	output voltage	VBUS; EN = LOW	0	30	V
$V_{I/O}$	input/output voltage	D-, D+, ID	0	5.5	V
T_{amb}	ambient temperature		−40	+85	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	73	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure that all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

Table 9. Static characteristics

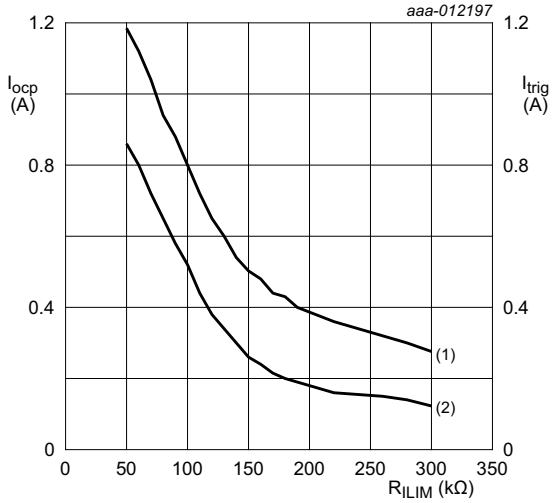
$V_{I(VINT)}$ = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	EN input	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	EN input	-	-	0.4	-	0.4	V
V_O	output voltage	VDET; I_{VDET} = −2 mA; 3 V < VBUS < 30 V	1.5	-	5.5	1.5	5.5	V
V_{OL}	LOW-level output voltage	$\overline{FAULT}$, I_O = 8 mA	-	-	0.5	-	0.5	V
I_O	output current	Current source; EN = HIGH	-	10	-	8	15	mA
I_{trig}	trigger current	OCP trigger; EN = HIGH; see Figure 6	-	-	-	-	-	mA
I_{ocp}	overcurrent protection current	EN = HIGH; see Figure 6	-	I_{trig}+250	-	I_{trig}+150	I_{trig}+350	mA
R_{pu}	pull-up resistance	$\overline{FAULT}$	20	-	200	-	-	kΩ
V_{pu}	pull-up voltage	$\overline{FAULT}$	-	-	VINT	-	VINT	V
R_{ILIM}	current limit resistance	ILIM	40	-	300	40	300	kΩ
I_{GND}	ground current	VBUS open; EN = LOW; see Figure 7 and Figure 8	-	20	-	-	40	µA
		VBUS open; EN = HIGH; see Figure 7 and Figure 8	-	220	-	-	360	µA
I_{OFF}	power-off leakage current	VBUS = 0 V to 30 V; VINT = 0 V; see Figure 9 [2]	-	2	-	-	22	µA
$I_{S(OFF)}$	OFF-state leakage current	VBUS = 0 V to 30 V; see Figure 10 and Figure 11 [2]	-	2	-	-	22	µA
V_{UVLO}	undervoltage lockout voltage		3.0	3.2	3.4	3.0	3.4	V
V_{OVLO}	overvoltage lockout voltage		5.5	5.75	6.0	5.5	6.0	V
$V_{hys(OVLO)}$	overvoltage lockout hysteresis voltage		-	150	-	-	-	mV
$C_{I/O}$	input/output capacitance	D-, D+, ID	-	3	-	-	-	pF
C_I	input capacitance	EN	-	2	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	0.2	-	-	1	nF

[1] Typical values are measured at T_{amb} = 25 °C and $V_{I(VINT)}$ = 5.0 V unless otherwise specified.

[2] Typical value is measured at T_{amb} = 25 °C and $V_{I(VBUS)}$ = 5.0 V.

13.1 Graphs

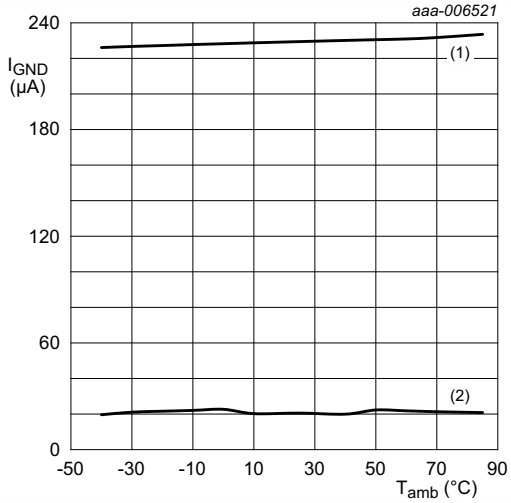


$V_{I(VINT)}$ = 5 V; T_{amb} = 25 °C.

(1) I_{ocp}

(2) I_{trig}

Fig 6. Typical OCP trigger current and overcurrent protection current versus the external resistor value.



(1) Enabled

(2) Disabled

Fig 7. Typical ground current versus temperature

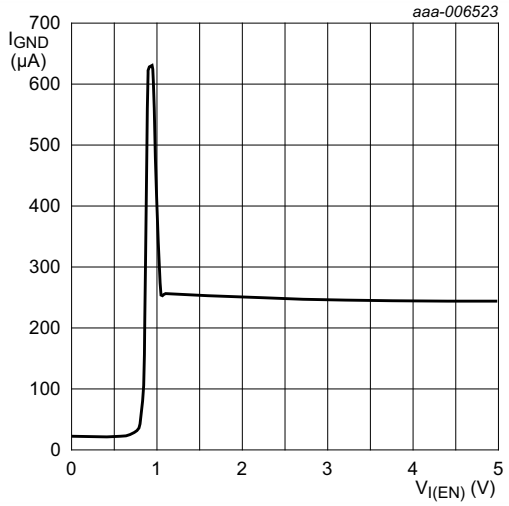
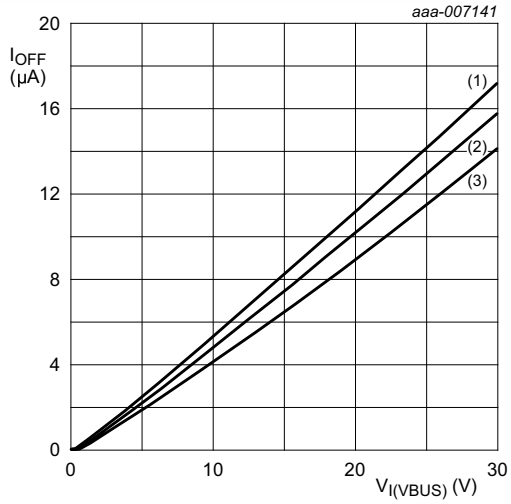


Fig 8. Typical ground current versus input voltage

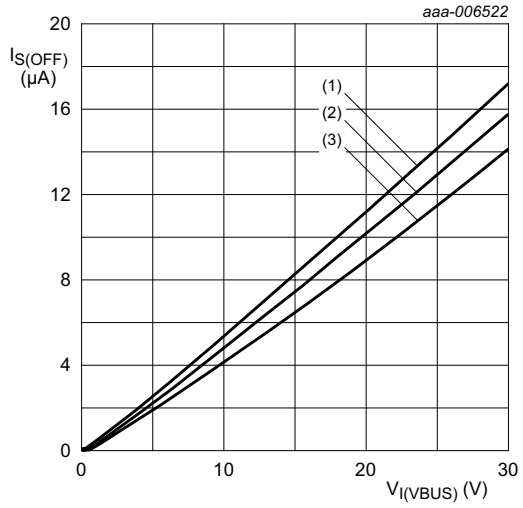


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

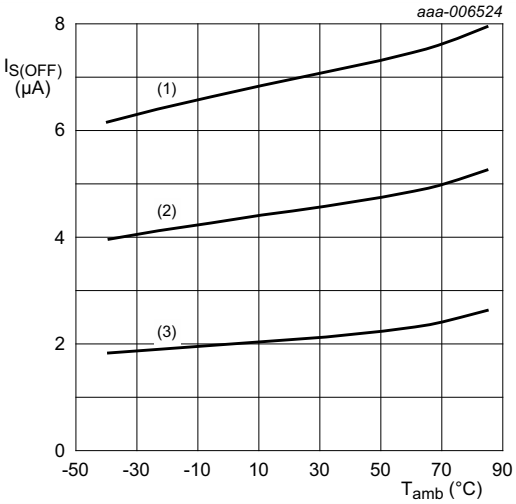
(3) T_{amb} = −40 °C

Fig 9. Typical power-off leakage current versus input voltage on pin VBUS



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig 10. Typical OFF-state leakage current versus input voltage on pin VBUS



(1) $V_{I(VBUS)}$ = 15.0 V
(2) $V_{I(VBUS)}$ = 10.0 V
(3) $V_{I(VBUS)}$ = 5.0 V

Fig 11. Typical OFF-state leakage current versus temperature

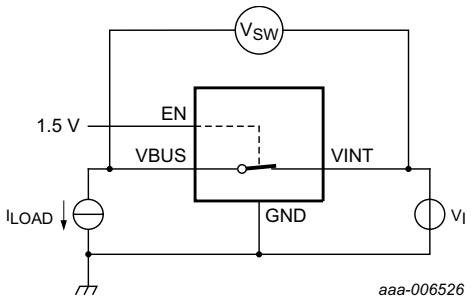
13.2 ON resistance

Table 10. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

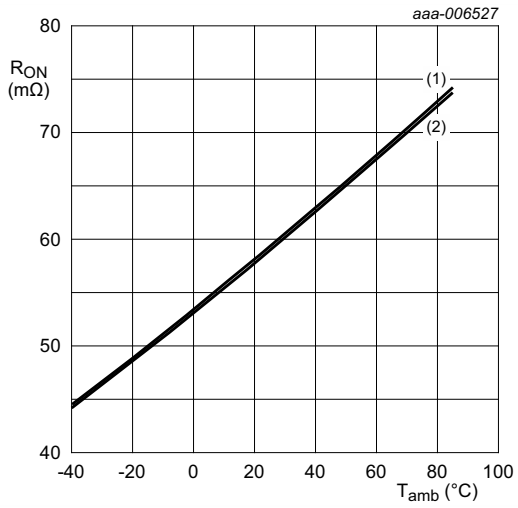
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	switch enabled; I_{LOAD} = 200 mA; see Figure 12, Figure 13 and Figure 14						
		$V_{I(VINT)}$ = 4.0 V to 5.5 V	-	60	-	-	100	mΩ

13.3 ON resistance test circuit and waveforms



$R_{ON} = V_{SW} / I_{LOAD}$.

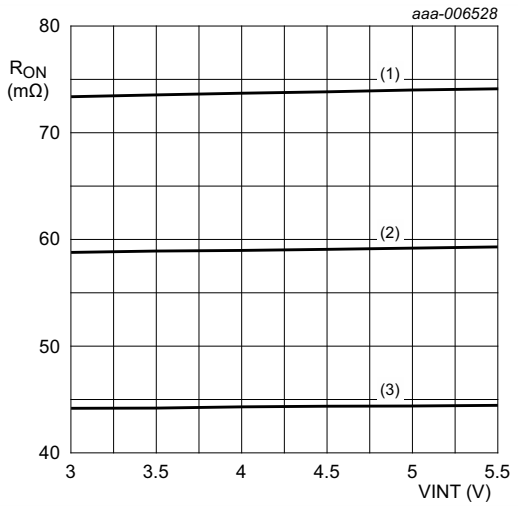
Fig 12. Test circuit for measuring ON resistance



(1) $V_{I(VINT)}$ = 5.5 V

(2) $V_{I(VINT)}$ = 4.0 V

Fig 13. Typical ON resistance versus temperature



(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 14. Typical ON resistance versus input voltage

14. Dynamic characteristics

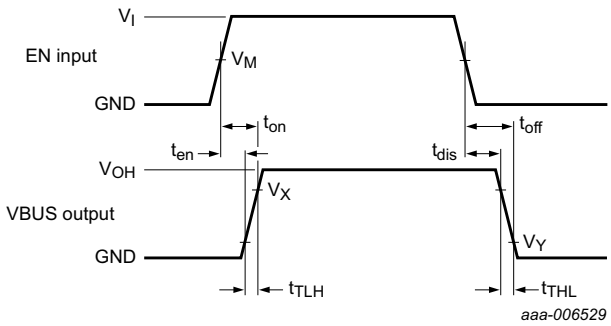
Table 11. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 16.
$V_{I(VINT)}$ = 4.0 V to 5.5 V.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	EN to VBUS; see Figure 15	-	0.18	-	0.14	-	ms
t_{dis}	disable time	EN to VBUS; see Figure 15	-	1.5	-	-	-	ms
t_{on}	turn-on time	EN to VBUS; see Figure 15	-	0.63	-	0.52	-	ms
t_{off}	turn-off time	EN to VBUS; see Figure 15	-	34.5	-	-	-	ms
t_{TLH}	LOW to HIGH output transition time	VBUS; see Figure 15	-	0.39	-	0.16	-	ms
t_{THL}	HIGH to LOW output transition time	VBUS; see Figure 15	-	33	-	-	-	ms
t_{degl}	deglitch time	VINT; while enabled; see Figure 23 [1]	-	8	-	-	-	ms

[1] Guarantee by design.

14.1 Waveforms, graphs and test circuit



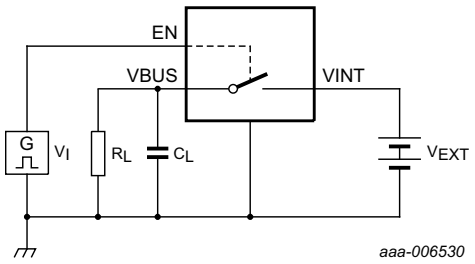
Measurement points are given in Table 12.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 15. Switching times

Table 12. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VINT)}$	V_M	V_X	V_Y
4.0 V to 5.5 V	$0.5 \times V_I$	$0.9 \times V_{OH}$	$0.1 \times V_{OH}$



Test data is given in Table 13.

Definitions test circuit:

R_L = Load resistance.

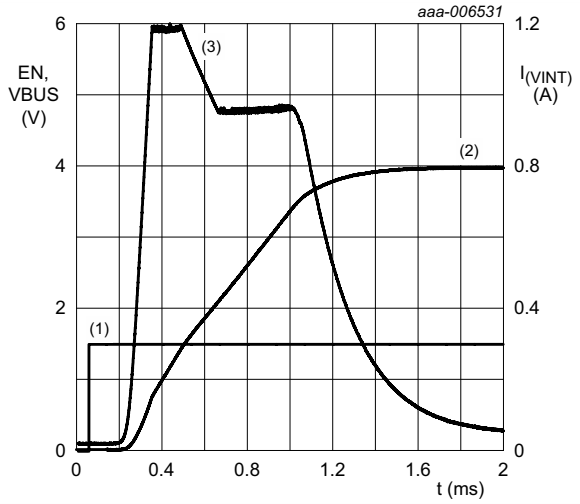
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 13. Test data

Supply voltage	Input	Load	
V_{EXT}	V_I	C_L	R_L
4.0 V to 5.5 V	1.5 V	100 μF	150 Ω



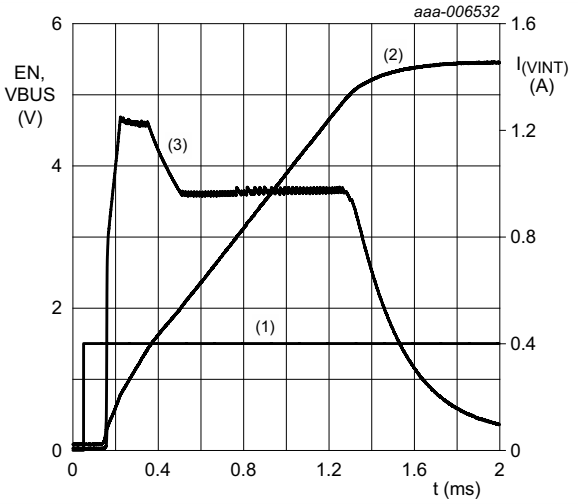
EN = 1.5 V; VINT = 4 V; R_L = 150 Ω; C_L = 220 µF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

(1) EN

(2) VBUS

(3) $I_{I(VINT)}$

Fig 17. Typical enable time and in-rush current



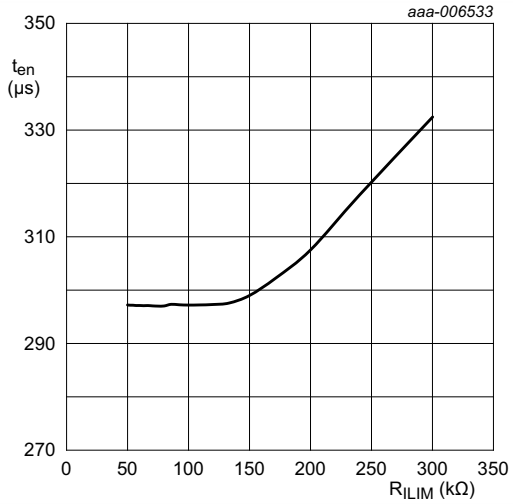
EN = 1.5 V; VINT = 5.5 V; R_L = 150 Ω; C_L =220 µF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

(1) EN

(2) V_{BUS}

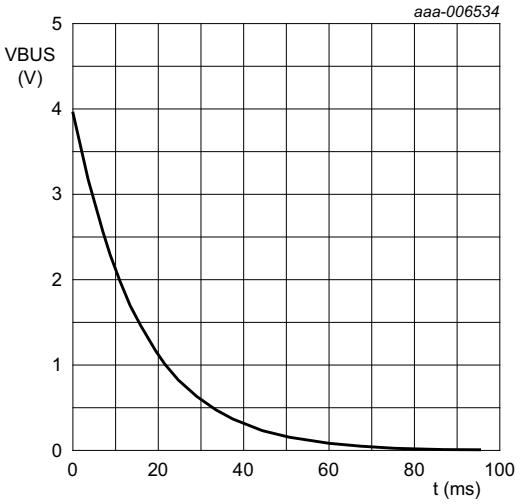
(3) $I_{I(VINT)}$

Fig 18. Typical enable time and in-rush current



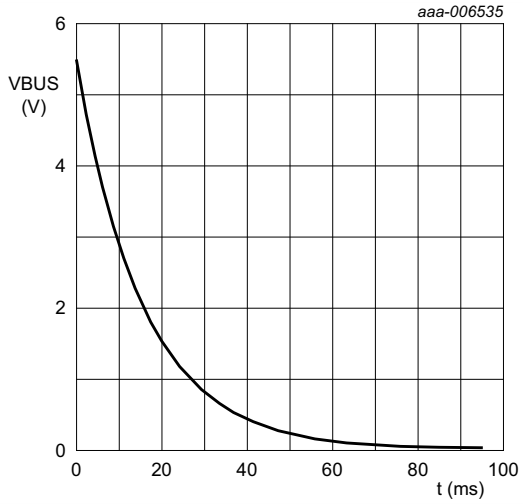
EN = 1.5 V; VINT = 4 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C.

Fig 19. Typical enable time versus current limit resistance (R_{ILIM})



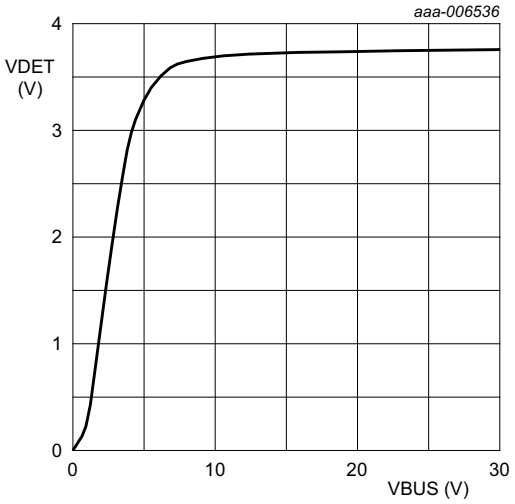
EN = 1.5 V; VINT = 4 V; R_L = 150 Ω; C_L = 100 µF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

Fig 20. Typical disable time



EN = 1.5 V; VINT = 5.5 V; R_L = 150 Ω; C_L = 100 µF; R_{ILIM} = 50 kΩ; T_{amb} = 25 °C.

Fig 21. Typical disable time



VINT = 5.5 V; T_{amb} = 25 °C.

Fig 22. Typical VDET versus VBUS

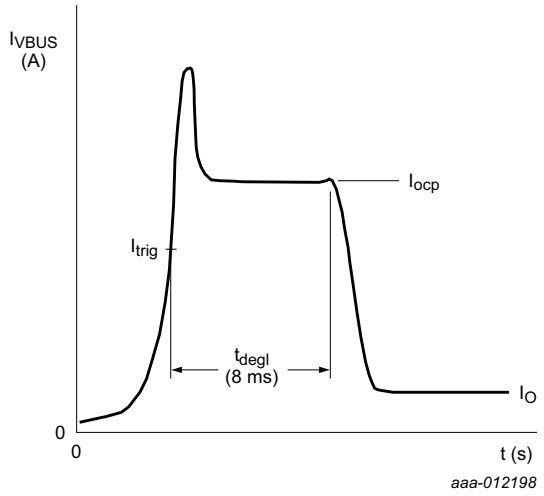
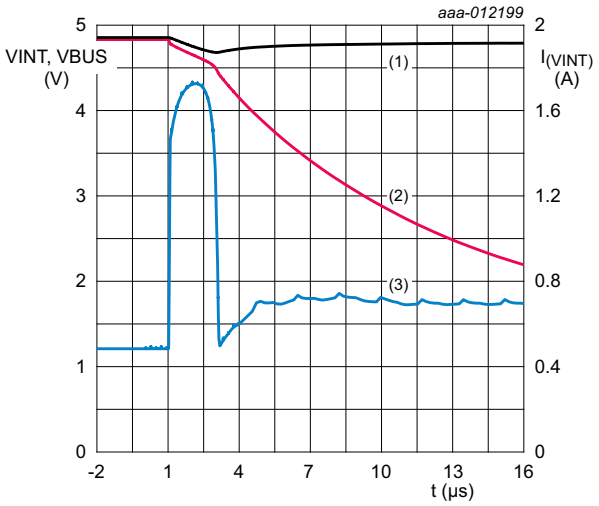


Fig 23. OCP level definitions

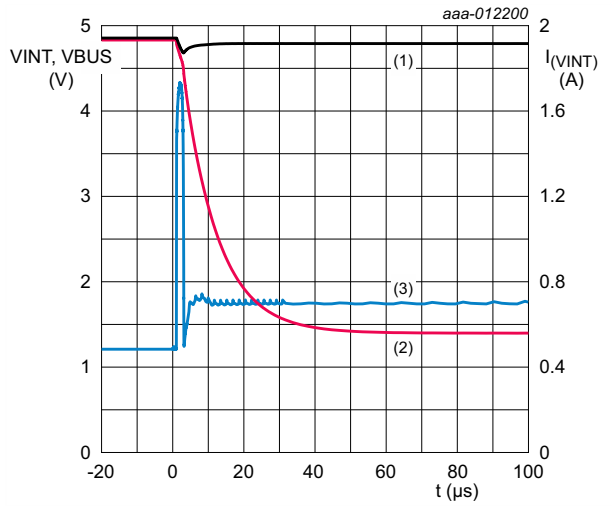


(1) VINT

(2) VBUS

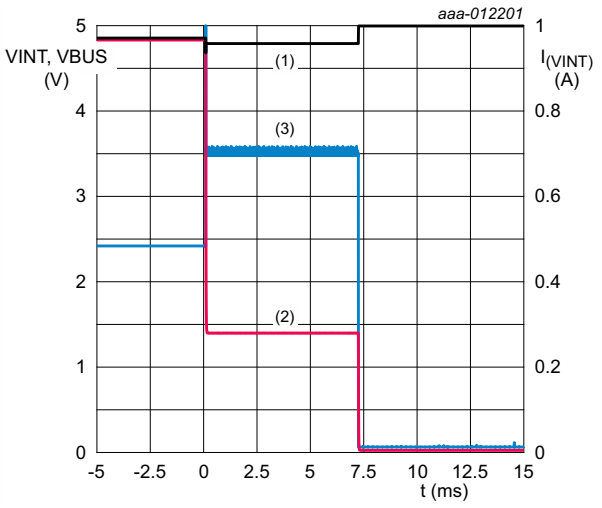
(3) $I_{I(VINT)}$

Fig 24. OCP load curve



(1) VINT
(2) VBUS
(3) $I_{I(VINT)}$

Fig 25. OCP load curve



(1) VINT
(2) VBUS
(3) $I_{I(VINT)}$

Fig 26. OCP load curve

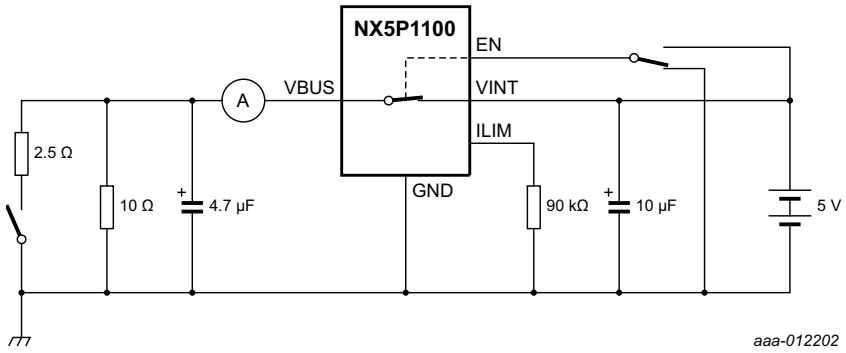
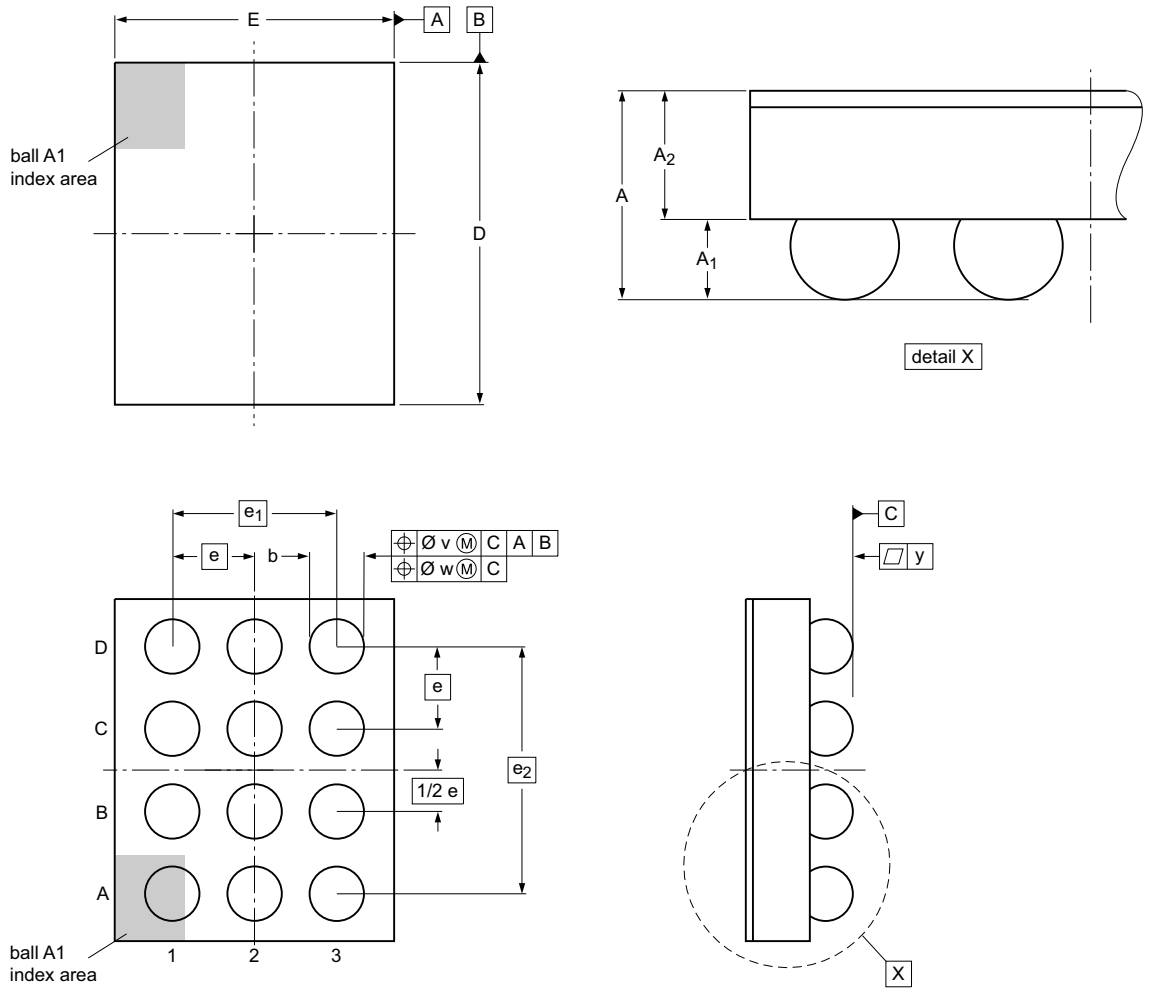


Fig 27. Test circuit for measuring OCP load curves

15. Package outline

WLCSP12: wafer level chip-scale package;
12 bumps; 1.36 x 1.66 x 0.51 mm, 0.4 mm pitch (Backside coating included) **NX5P1100**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.55	0.23	0.34	0.29	1.69	1.39						
mm	nom	0.51	0.20	0.31	0.26	1.66	1.36	0.4	0.8	1.2	0.05	0.15	0.03
	min	0.47	0.17	0.29	0.23	1.63	1.33						

wlcsp12_nx5p1100_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX5P1100						~~13-08-22~~ 13-12-20

Fig 28. Package outline NX5P1100 (WLCSP12)

16. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
OCP	OverCurrent Protection
OTP	OverTemperature Protection
RCP	Reverse Current Protection
USB OTG	Universal Serial Bus On-The-Go
UVLO	Undervoltage lockout
VBUS	USB Power Supply
OVLO	Overvoltage lockout

17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P1100 v.1	20140321	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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