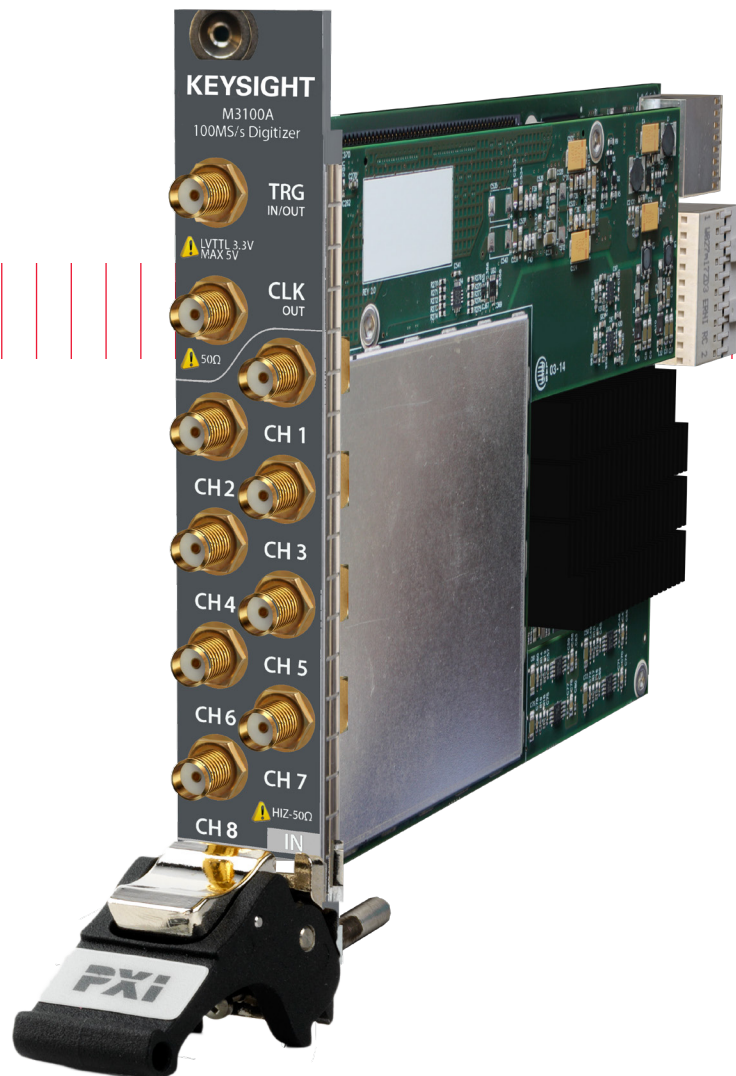


# Keysight M3100A

## PXIe Digitizers with Optional Real-Time Sequencing and FPGA Programming

100 MSa/s, 14 Bits, 4/8 Channels

Data Sheet



## Improve Your Measurement Fidelity, Signal Integrity and Measurement Throughput

The M3102A are high-performance, high-bandwidth digitizers with an advanced data acquisition system (DAQ). Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (HVI Hard Virtual Instrumentation), and graphical FPGA programming technology.

### Features

**100 MSa/s simultaneous sampling, 14 bits, 4/8 channels, 100 MHz BW<sup>1</sup>**

#### Advanced data acquisition system (DAQ)

- Flexible triggering (HW trigger, HVI trigger, SW trigger)
- Programmable cycles and data bursts to avoid PC saturation

#### Optional HW programming for high-performance applications

- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7, 325T or 410T FPGA

**Up to 2 GB of onboard RAM (~ 1 Gsamples)**

#### Mechanical/interface

- 1 slot 3U (PXIe)
- Up to 1.6 GB/s transfer BW with P2P capabilities (PCIe Gen 2)
- Independent DMA channels for fast and efficient data transfer

### Applications

**General purpose digitizer**

**Hardware-in-the-loop (HIL)/automated test equipment (ATE)**

**R&D/scientific research equipment**

**Aerospace & defense (A/D)**

1. 100 MHz refer to the Front End bandwidth. This digitizer can operate in 1st and 2nd Nyquist zones (using undersampling technique), but its real-time BW is limited by Nyquist to some 50 MHz. As an example for a band-limited signal of 70 MHz with a 10 MHz signal bandwidth the aliased component will appear between 25 to 35 MHz (30 ± 5 MHz).

## Programming Technology and Software Tools

### Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python, and more

### Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully-parallelized hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
  - Graphical M3602A FPGA design environment (-FP1 option required on HW)
  - No FPGA know-how required
  - Include high-level to low-level design elements: off-the-shelf DSP blocks, MATLAB/Simulink designs, Xilinx CORE Generator IP cores, Xilinx VIVADO/ISE projects, VHDL or Verilog code
  - Ultra-fast, one-click compiling and on-the-fly programming

### No programming

- Ready-to-use SD1 SPF (software front panels)

## PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	2/4	DC-400				
M3201A	AWG	500	16	2/4	DC-200				
M3102A	Digitizer					500	14	2/4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

## Functional Block Diagram

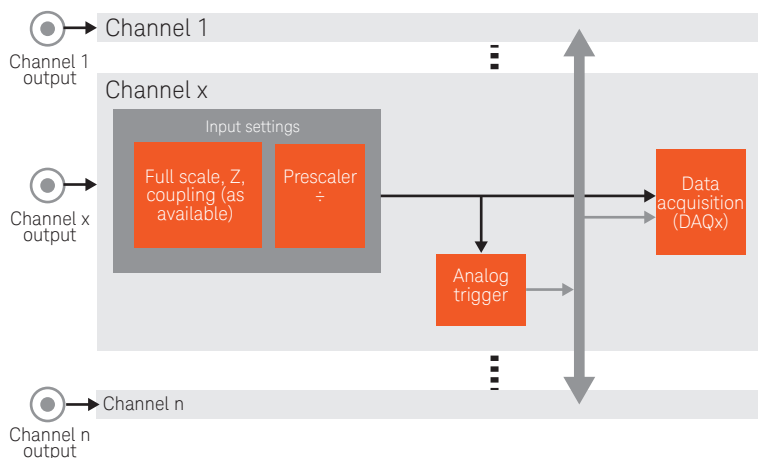


Figure 1. M3100A input functional block diagram, all channels have identical input structure

## Ordering Information <sup>1</sup>

Product	Description
M3100A	PXIe digitizer: 100 MSa/s, 14 Bits
Options	Description
M3100A-CH4 / -CH8	Four channels <sup>2</sup> / eight channels
M3100A-CLF	Fixed sampling clock, low jitter <sup>2</sup>
M3100A-M01 / -M12 / -M20	Memory 16 MB, 8 MSamples <sup>2</sup> / 128 MB, 60 MSamples / 2 GB, 1 GSamples
HW programming options	Description
M3100A-HVI	Enabled HVI programming, requires an HVI design environment license (M3601A)
M3100A-FP1	Enabled FPGA programming, requires -K32 or -K41 option and an FPGA design environment license (M3602A)
M3100A-K32 / -K41	FPGA, Xilinx 7K325T / 7K410T, required for -FP1 option only (needs memory option -M20)

Related software	Description
M3601A	HVI design environment
M3602A	FPGA design environment

1. All options must be selected at time of purchase and are not upgradable  
 2. These options represent the standard configuration

## Technical Specifications and Characteristics

### General characteristics

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>Inputs and outputs</b>								
Channels	4			8			Out	
Reference clock <sup>1</sup>	1			1			Out	
Reference clock <sup>2</sup>	1			1			In	
Triggers/markers <sup>1,3</sup>	1			1			In/out	Reconfigurable
Triggers/markers <sup>2,3</sup>	8			8			In/out	Reconfigurable
<b>Input channels overview</b>								
Sampling rate	100			100			MSa/s	
Voltage resolution	14			14			Bits	
Input frequency	DC	100		DC	100		MHz	
Real-time BW	50			50			MHz	
Time skew	<50			<50			ps	Between channels
<b>Built-in functionalities</b>								
Input conditioning blocks	4			8				1 per channel
Analog trigger processors	4			8				1 per channel
Data acquisition blocks	4			8				1 per channel
<b>Onboard memory</b>								
RAM memory	16	2048		16	2048		MBytes	

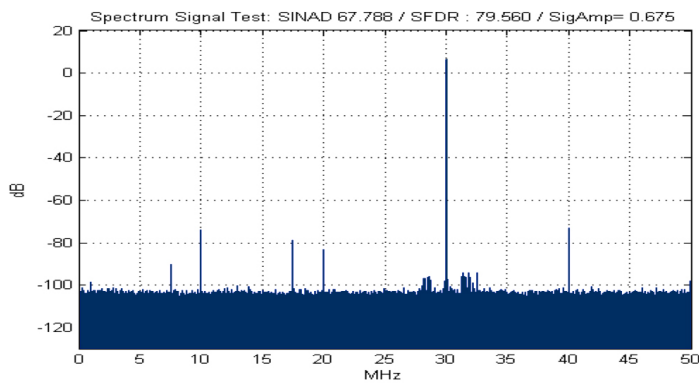
1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later

## I/O specifications

**Analog input characteristics**

Number of channels	CH4 or CH8
Sampling rate	100 MSa/s option CLF
Configurable inputs: impedance	50Ω or 1 MΩ (HiZ)
Configurable inputs: Coupling	AC or DC
Input voltage range (50Ω)	400 mVpp to 6Vpp (continue: variable attenuator at input)
Input voltage range (HiZ)	200 mVpp to 20Vpp (continue: variable attenuator at input)
Bandwidth limit filters	100 MHz
Effective number of bits (ENOB) <sup>1</sup>	10.8 bits @30MHz (typical)
Noise floor	-142 dBm/Hz @30 MHz (typical)
SINAD	67 dB @30 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distorsion	79 dBc (typical)

1. measured at -1 DBFS input signal with 1.5 Vpp 50Ω



Parameter	M3100A			Units	Comments
	Min	Typ	Max		
<b>Reference clock output</b>					
Frequency		10 or 100		MHz	Generated from the internal clock. User selectable
Voltage		800		mVpp	On a 50 Ω load
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
<b>External I/O trigger/marker</b>					
V <sub>IH</sub>	2		5	V	
V <sub>IL</sub>	0		0.8	V	
V <sub>OH</sub>	2.4		3.3	V	On a high Z load
V <sub>OL</sub>	0		0.5	V	On a high Z load
Input impedance		10		K Ω	
Source impedance		TTL		-	
Speed			500	Mbps	

## Data acquisition blocks (DAQs) specifications

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
DAQs	4			8				1 per channel
Aggregated speed	400			800			MSa/s	For all onboard DAQs combined
Acquisition burst multiple	5			5			Samples	Burst length must be a multiple of this value
Acquisition RAM capacity	15		957M	15		957M	Samples	Maximum depends on onboard RAM
Acquisition RAM capacity effic.	93.5			93.5			%	Effic. = waveform size / waveform size in RAM
Trigger	Selec.			Selec.				Hardware trigger (analog channels, input trigger, backplane triggers), software trigger
<b>DAQ specifications</b>								
Speed	100			100			MSa/s	Per DAQ
Resolution	14			14			Bits	

## Clock system specifications

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Clock frequency	100			100			MHz	

## System Specifications

### Environmental specifications (PXI Express)

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>System bus</b>								
Slots	1			1			Slot	PXI Express (CompactPCI Express compatible)
PCI Express type	Gen 1		Gen 2	Gen 1		Gen 2	-	Automatic gen negotiation, chassis dependent
PCI Express link	1		4	1		4	Lanes	Automatic lane negotiation, chassis dependent
PCI Express speed	400		1600	400		1600	MBytes/s	Depends on # of lanes, chassis, congestion, and more
Sustainable throughput	200		800	200		800	MPoints/s	Depends on # of lanes, chassis, congestion, and more
<b>Power dissipation</b>								
3.3V PXIe power supply	1.5			1.5			A	~ 5 W
12V PXIe power supply	2			2			A	~ 24 W

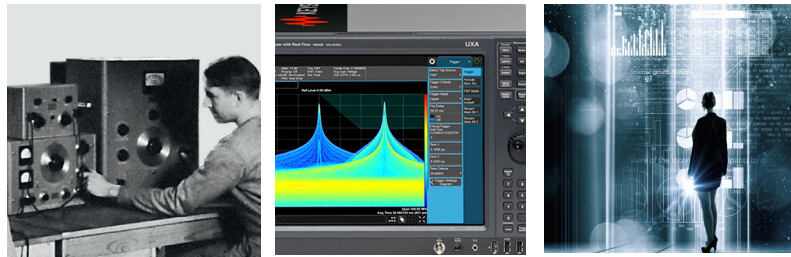
<b>Environmental <sup>1</sup></b>	
Temperature range	Operating Non-operating
	0 to +55°C (10,000 feet) -40 to +70 °C (up to 15,000 feet)
Max operative altitude	2000 m (10,000 feet)
Operating Humidity range (%RH)	10 to 95% at 40 °C
Non-operating Humidity range (%RH): 5 to 95	5 to 95%
Calibration interval	1 year
EMC	Complies with European EMC Directive - IEC/EN 61326-1 - CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada. This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.



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