RENESAS TECHNICAL UPDATE

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Title	Correction for Incorrect Description Notice RL78/I1A Descriptions in the Hardware User' Rev. 2.10 Changed	Information Category	Technical Notification			
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This document describes misstatements found in the RL78/I1A hardware user's manual Rev. 2.10 (R01UH0169EJ0210).

Corrections

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Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)	P.303	Incorrect descriptions revised
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32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	P.1100	Explanations added
33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	P.1142	Explanations added



Document Improvement

The above corrections will be made for the next revision of the hardware user's manual.

Corrections in the hardware user's manual

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15	33.7 Data Me Retention Ch	emory STOP Mode Lo naracteristics	ow Supply Voltage Data	p.1142	p.36

Incorrect: Bold with underline; Correct: Gray hatched

Issued Document History

RL78/I1A Incorrect description notice, issued document history

Document Number	Issue Date	Description
TN-RL*-A024A/E	Apr. 9, 2014	First edition issued Incorrect descriptions of No.1 to No.15 revised (This notice)



1. Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)

Incorrect descriptions of the TMRSTEN1 and TMRSTEN0 bits of Peripheral Function Switch Register 0 (PFSEL0) are revised, and Note is added.

Incorrect:

Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0) Address: F05C6H After reset: 00H R/W Symbol <6> <5> <4> 3 2 <1> <0> 7 PFSEL0 ADTRG11 ADTRG10 TMRSTEN1 TMRSTEN0 0 CMP2STEN **CMP0STEN** PNFEN CMP2STEN CMP0STEN Comparator interrupt selection See CHAPTER 14 COMPARATOR. PNFEN Use/Do not use external interrupt INTP20 noise filter Use noise filter 0 1 Do not use noise filter ADTRG11 ADTRG10 Timer trigger selection for A/D conversion 0 0 Timer KB0 trigger source 0 1 Timer KB1 trigger source 0 Timer KB2 trigger source 1 1 1 Setting prohibited TMRSTEN1 Function selection for external interrupt INTP21 0 External interrupt function (external interrupt generation enabled, timer restart disabled) Timer restart function (external interrupt generation disabled, standby release disabled) 1 TMRSTEN0 Function selection for external interrupt INTP20 0 External interrupt function (external interrupt generation enabled, timer restart disabled) 1 Timer restart function (external interrupt generation disabled, standby release disabled) Remark See Figure 14-1 Block Diagram of Comparator.



Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN
	r	1						
	CMP2STEN	CMP0STEN		C	Comparator int	errupt selectio	on	
	See CHAPT	ER 14 CON	IPARATOR.					
	PNFEN		Use/D	o not use ex	ternal interrupt	t INTP20 nois	e filter	
	0	Use noise filt	er					
	1	Do not use n	oise filter					
		8						
	ADTRG11	ADTRG10		Timer	trigger selectio	on for A/D con	version	
	0	0	Timer KB0 tri	gger source				
	0	1	Timer KB1 trig	gger source				
	1	0	Timer KB2 tri	gger source				
	1	1	Setting prohib	oited				
	TMRSTEN1			Switch of ext	ternal interrupt	INTP21 Note		
	0	External inter	rrupt function is	s selected (st	op mode relea	ase enabled, t	imer restart di	sabled).
	1	Timer restart	function is sel	ected (stop n	node release c	lisabled, timer	restart enable	ed).
	TMRSTEN0			Switch of ext	ternal interrupt	INTP20 Note		
	0	External inter	rrupt function is	s selected (st	op mode relea	ase enabled, t	imer restart di	sabled).
	1	Timer restart	function/force	d output stop	function 2 is s	selected (stop	mode release	disabled,
		timer restart	enabled).					
Note	When INTF function, se	20 or INTP2 ee 14. 5 Ca	1 is used as ution for Us	a trigger of ing Timer I	the timer KE KB Simultar	3 forced outp neous Opera	out stop func ation Functi	tion 2 or tim on .
Rema	rk See Fig	ure 14-1 B	lock Diagrar	n of Comp	arator.			



RENESAS TECHNICAL UPDATE TN-RL*-A024A/E Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) 2. Incorrect descriptions of forced output stop function control register 0p (TKBPACTL0p) are revised, and Note is added. Incorrect: Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2) Address: F0630H (TKBPACTL00), F0632H (TKBPACTL01) After reset: 0000H R/W 14 13 12 10 9 8 15 11 Symbol TKBPACTL0p TKBPAFXS0p3 TKBPAFXS0p2 TKBPAFXS0p1 TKBPAFXS0p0 0 0 0 TKBPAFCM0p 7 6 5 4 3 2 1 0 0 TKBPAHZS0p2 TKBPAHZS0p1 TKBPAHZS0p0 TKBPAHCM0p1 TKBPAHCM0p0 TKBPAMD0p1 TKBPAMD0p0 TKBPAFXS0p3 External interruption trigger selection for forced output stop function 2 0 INTP20 can not be used as a trigger. INTP20 can be used as a trigger. 1 TKBPAFXS0p2 Comparator trigger selection for forced output stop function 2 0 Comparator 2 can not be used as a trigger. 1 Comparator 2 can be used as a trigger.

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2	
0	Comparator 1 can not be used as a trigger.	
1	Comparator 1 can be used as a trigger.	

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger.

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.



Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

	TKBPAHZS0p2	Comparator trigger selection for forced output stop function 1
0 Comparator 2 can not be used as a trigger. 1 Comparator 2 can be used as a trigger.		Comparator 2 can not be used as a trigger.
		Comparator 2 can be used as a trigger.

TKBPAHZS0p1	'KBPAHZS0p1 Comparator trigger selection for forced output stop function 1	
0	Comparator 1 can not be used as a trigger.	
1	Comparator 1 can be used as a trigger.	

TKBPAHZS0p0	p0 Comparator trigger selection for forced output stop function 1	
0	Comparator 0 can not be used as a trigger.	
1	Comparator 0 can be used as a trigger.	

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when Hi-Z stop trigger (TKBPAHTT0) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "Hi-Z stop trigger (TKBPAHTTO) = 1" is invalid. Forced output stop function 1 is cleared when Hi-Z stop trigger. (TKBPAHTTO) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after Hi-Z stop trigger . (TKBPAHTT0) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing " Hi-Z stop trigger (TKBPAHTT0) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after Hi-Z stop trigger (TKBPAHTT0) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function		
		Forced output stop function 1	Forced output stop function 2	
0	0	Hi-Z output	Output fixed at low level	
0	1	Hi-Z output	Output fixed at high level	
1	0	Output fixed at low level	Output fixed at low level	
1	1	Output fixed at high level	Output fixed at high level	

Cautions 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1



Correct:

ddress: F0630	ОН (ТКВРАСТ	L00), F0632H	(TKBPACTL	01) After	reset: 0000H	R/W		
Symbol	15	14	13	12	11	10	9	8
KBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM
	7	6	5	4	3	2	1	0
	0	TKBPAHZS0p2	TKBPAHZS0p1	TKBPAHZS0p0 T	KBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0
	TKBPAFXS0p3	E	External interr	uption trigger se	election for fo	rced output st	op function 2	2
	0	INTP20 can	not be used a	as a trigger.				
	1	INTP20 can	be used as a	trigger. Note 1				
	TKBPAFXS0p2		Comparat	or trigger select	ion for forced	output stop f	unction 2	
	0	Comparator	2 can not be	used as a trigge	er.			
	1	Comparator	2 can be use	ed as a trigger. ^N	lote 2			
	TKBPAFXS0p1		Comparat	or trigger select	ion for forced	output stop f	unction 2	
	0	Comparator	1 can not be	used as a trigge	er.			
	1	Comparator	1 can be use	ed as a trigger.	lote 3			
	TKBPAFXS0p0		Comparat	or trigger select	ion for forced	output stop f	unction 2	
	0	Comparator	0 can not be	used as a trigge	er.			
	1	Comparator	0 can be use	ed as a trigger. ^N	lote 2			
	TKBPAFCM0p		Operatio	n mode selectic	on for forced o	output stop fu	nction 2	
	0	Forced outp cleared at th	ut stop functione next counter	on 2 starts with t er period. ^{Note 4}	trigger input,	and forced ou	itput stop fur	nction 2 is
	1	Forced outp cleared at th 4	ut stop functione next counte	on 2 starts with ter period following	trigger input, ng detection o	and forced ou of the reverse	itput stop fur edge of the	nction 2 is trigger. ^{Note}
		1	Composed		ion for forced	autout at an f	instice 1	
	0	Comparator				output stop i		
	1	Comparator	2 can be use		lote 2			
	I	Comparator	2 can be use					
	TKBPAHZS0p1		Comparat	tor trigger select	ion for forced	output stop f	unction 1	
	0	Comparator	1 can not be	used as a trigg	er.			
	1	Comparator	1 can be use	ed as a trigger.	lote 3			
	TKBPAHZS0n0		Comparat	or trigger select	ion for forced	output stop f	unction 1	
	0	Comparator						
	U	Comparator	U Call HOLDE	useu as a linggi	υ .			



Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1	
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.	
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written while the trigger signal is in its inactive period.	
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.	
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written when the trigger signal is in its inactive period.	

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function		
		Forced output stop function 1	Forced output stop function 2	
0	0	Hi-Z output	Output fixed at low level	
0	1	Hi-Z output	Output fixed at high level	
1	0	Output fixed at low level	Output fixed at low level	
1	1	Output fixed at high level	Output fixed at high level	

- Notes 1. When INTP20 is used as the forced output stop function 2, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - When CMP0 or CMP2 is used as the timer KB forced output stop function, set CMPnSTEN = 1. See 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - 3. When CMP1 is used as the timer KB forced output stop function, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - **4.** When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).
- Cautions 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).
 - 2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1



3. Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) Incorrect descriptions of forced output stop function control register 1p (TKBPACTL1p) are revised, and Note is added. Incorrect: Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (1/2) Address: F0670H (TKBPACTL10), F0672H (TKBPACTL11) After reset: 0000H R/W 13 10 9 8 15 14 12 11 Symbol TKBPACTL1p TKBPAFXS1p3 TKBPAFXS1p2 TKBPAFXS1p1 TKBPAFXS1p0 0 0 0 TKBPAFCM1p 7 6 5 3 2 0 4 1 0 TKBPAHZS1p2 TKBPAHZS1p1 TKBPAHZS1p0 TKBPAHCM1p1 TKBPAHCM1p0 TKBPAMD1p1 TKBPAMD1p0 **FKBPAFXS1p3** External interruption trigger selection for forced output stop function 2 0 INTP20 can not be used as a trigger. 1 INTP20 can be used as a trigger. TKBPAFXS1p2 Comparator trigger selection for forced output stop function 2 0 Comparator 3 can not be used as a trigger. 1 Comparator 3 can be used as a trigger. TKBPAFXS1p1 Comparator trigger selection for forced output stop function 2 0 Comparator 2 can not be used as a trigger. 1 Comparator 2 can be used as a trigger. TKBPAFXS1p0 Comparator trigger selection for forced output stop function 2 0 Comparator 0 can not be used as a trigger. 1 Comparator 0 can be used as a trigger. TKBPAFCM1p Operation mode selection for forced output stop function 2 0 Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. 1 Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.



Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (2/2)

TKBPAHZS1p2	Comparator trigger selection for forced output stop function 1			
0	Comparator 3 can not be used as a trigger.			
1	Comparator 3 can be used as a trigger.			

TKBPAHZS1p1	Comparator trigger selection for forced output stop function 1			
0	Comparator 2 can not be used as a trigger.			
1	Comparator 2 can be used as a trigger.			

TKBPAHZS1p0	Comparator trigger selection for forced output stop function 1			
0	Comparator 0 can not be used as a trigger.			
1	Comparator 0 can be used as a trigger.			

TKBPAHCM1p1	TKBPAHCM1p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when Hi-Z stop trigger (TKBPAHTT1) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "Hi-Z stop trigger (TKBPAHTT1) = 1" is invalid. Forced output stop function 1 is cleared when Hi-Z stop trigger. (TKBPAHTT1) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after Hi-Z stop trigger . (TKBPAHTT1) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing " Hi-Z stop trigger (TKBPAHTT1) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after Hi-Z stop trigger (TKBPAHTT1) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD1p1	TKBPAMD1p0	Output status selection when executing forced output stop function		
		Forced output stop function 1	Forced output stop function 2	
0	0	Hi-Z output	Output fixed at low level	
0	1	Hi-Z output	Output fixed at high level	
1	0	Output fixed at low level	Output fixed at low level	
1	1	Output fixed at high level	Output fixed at high level	

Cautions 1. During timer operation, setting the other bits of the TKBPACTL1p register is prohibited. However, the TKBPACTL1p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1



Correct:

dress: F0670	H (TKBPAC	ΓL10), F0672⊦	I (TKBPACTL	11) After	reset: 0000H	R/W			
Symbol	15	14	13	12	11	10	9	8	
BPACTL1p	TKBPAFXS1p3	TKBPAFXS1p2	TKBPAFXS1p1	TKBPAFXS1p0	0	0	0	TKBPAFCM'	
	7	6	5	4	3	2	1	0	
	0	TKBPAHZS1p2	TKBPAHZS1p1	TKBPAHZS1p0	KBPAHCM1p1	TKBPAHCM1p0	TKBPAMD1p1	TKBPAMD1	
	TKBPAFXS1p3	-	External interr	uption trigger s	election for fo	prced output st	op function 2	2	
	0	INTP20 can	not be used a	as a trigger.					
	1	INTP20 can	be used as a	trigger. Note 1					
	TKBPAFXS1p2		Comparat	or trigger select	ion for forced	d output stop fi	unction 2		
	0	Comparator	3 can not be	used as a trigg	er.				
	1	Comparator	3 can be use	d as a trigger.	lote 2				
	TKRP4FXS1n1		Comparat	or trigger select	ion for forcer	t output stop fi	unction 2		
	0	Comparator	2 can not be	used as a trigg	er				
	1	Comparator	2 can be use	d as a trigger.	lote 3				
			0			1 .	and the second		
	0	Comparator	Comparator 0 can not be used as a triager.						
	1	Comparator	0 can be use	d as a trigger.	lote 3				
			Operatio	n mode selectio	on for forced	outout stop fur	action 2		
		Forood outr						ation 2 io	
	U	cleared at th	ne next counte	er period. Note 4	trigger input,	and forced ou	itput stop für	ICTION 2 IS	
	1	Forced outp cleared at th 4	out stop function ne next counte	on 2 starts with er period followi	trigger input, ng detection	and forced ou of the reverse	tput stop fur edge of the	nction 2 is trigger. ^{Note}	
	TKBPAHZS1p2		Comparat	or trigger selec	tion for forced	d output stop f	unction 1		
	0	Comparator	r 3 can not be	used as a trigg	er.				
	1	Comparator	r 3 can be use	d as a trigger.	1016 2				
	TKBPAHZS1p1		Comparat	or trigger selec	tion for forced	d output stop f	unction 1		
	0	Comparato	r 2 can not be	used as a trigg	er.				
	1	Comparator	r 2 can be use	ed as a trigger.	Note 3				
		-							
l			0	and the large states and the	in a far fare	· · · · · · · · · · · · · · · · · ·			
	TKBPAHZS1p0		Comparat	or trigger selec	tion for forced	d output stop f	unction 1		



Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (2/2)

TKBPAHCM1p1	TKBPAHCM1p0	Clear condition selection for forced output stop function 1	
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT1p) = 1 is written, regardless of the trigger signal level.	
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT1p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT1p) = 1 is written while the trigger signal is in its inactive period.	
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT1p) = 1 is written, regardless of the trigger signal level.	
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT1p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT1p) = 1 is written when the trigger signal is in its inactive period.	

TKBPAMD1p1	TKBPAMD1p0	Output status selection when executing forced output stop function		
		Forced output stop function 1	Forced output stop function 2	
0	0	Hi-Z output	Output fixed at low level	
0	1	Hi-Z output	Output fixed at high level	
1	0	Output fixed at low level	Output fixed at low level	
1	1	Output fixed at high level	Output fixed at high level	

- Notes 1. When INTP20 is used as the forced output stop function 2, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - When CMP3 is used as the timer KB forced output stop function, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - When CMP0 or CMP2 is used as the timer KB forced output stop function, set CMPnSTEN = 1. For details, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - 4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).
- Cautions 1. During timer operation, setting the other bits of the TKBPACTL1p register is prohibited. However, the TKBPACTL1p register can be refreshed (the same value is written).
 - 2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1



Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) 4. Incorrect descriptions of forced output stop function control register 2p (TKBPACTL2p) are revised, and Note is added. Incorrect: Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (1/2) Address: F06B0H (TKBPACTL20), F06B2H (TKBPACTL21) After reset: 0000H R/W 13 10 9 8 15 14 12 11 gSymbol TKBPACTL2p TKBPAFXS2p3 TKBPAFXS2p2 TKBPAFXS2p1 TKBPAFXS2p0 0 0 0 TKBPAFCM2p 7 6 5 3 2 0 4 1 0 TKBPAHZS2p2 TKBPAHZS2p1 TKBPAHZS2p0 TKBPAHCM2p1 TKBPAHCM2p0 TKBPAMD2p1 TKBPAMD2p0 FKBPAFXS2p3 External interruption trigger selection for forced output stop function 2 0 INTP20 can not be used as a trigger. 1 INTP20 can be used as a trigger. TKBPAFXS2p2 Comparator trigger selection for forced output stop function 2 0 Comparator 5 can not be used as a trigger. 1 Comparator 5 can be used as a trigger. TKBPAFXS2p1 Comparator trigger selection for forced output stop function 2 0 Comparator 3 can not be used as a trigger. 1 Comparator 3 can be used as a trigger. TKBPAFXS2p0 Comparator trigger selection for forced output stop function 2 0 Comparator 0 can not be used as a trigger. 1 Comparator 0 can be used as a trigger. TKBPAFCM2p Operation mode selection for forced output stop function 2 0 Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. 1 Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.



Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (2/2)

TKBPAHZS2p2	Comparator trigger selection for forced output stop function 1
0	Comparator 5 can not be used as a trigger.
1	Comparator 5 can be used as a trigger.

TKBPAHZS2p1	Comparator trigger selection for forced output stop function 1
0	Comparator 4 can not be used as a trigger.
1	Comparator 4 can be used as a trigger.

TKBPAHZS2p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger.

TKBPAHCM2p1	TKBPAHCM2p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when Hi-Z stop trigger (TKBPAHTT2) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "Hi-Z stop trigger (TKBPAHTT2) = 1" is invalid. Forced output stop function 1 is cleared when Hi-Z stop trigger. (TKBPAHTT2) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after Hi-Z stop trigger . (TKBPAHTT2) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing " Hi-Z stop trigger (TKBPAHTT2) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after Hi-Z stop trigger (TKBPAHTT2) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD2p1	TKBPAMD2p0	Output status selection when ex	ecuting forced output stop function
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL2p register is prohibited. However, the TKBPACTL2p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1



Correct:

		1220),100021			51 Teset. 000							
Symbol	15	14	13	12	11	10	9	8				
PACTL2p	TKBPAFXS2p3	TKBPAFXS2p2	TKBPAFXS2p1	TKBPAFXS2p0	0	0	0	TKBPAFCM2				
	7	6	5	4	3	2	1	0				
	0	TKBPAHZS2p2	TKBPAHZS2p1	TKBPAHZS2p0	ТКВРАНСМ2р	1 TKBPAHCM2p0	TKBPAMD2p1	TKBPAMD2p				
	TKBPAFXS2p3	E	External interr	uption trigger s	election for	forced output s	top function 2					
	0	INTP20 can	not be used a	as a trigger.								
	1	INTP20 can	be used as a	trigger. Note 1								
	TKBPAFXS2p2		Comparate	or trigger seled	tion for force	ed output stop f	unction 2					
	0	Comparator	Comparator 5 can not be used as a trigger.									
	1	Comparator	Comparator 5 can be used as a trigger. Note 2									
	TKBPAFXS2p1	Comparator trigger selection for forced output stop function 2										
	0	Comparator	Comparator 3 can not be used as a trigger.									
	1	Comparator	3 can be use	d as a trigger.	Note 2							
	TKBPAFXS2p0		Comparate	or trigger selec	tion for force	ed output stop f	unction 2					
	0	Comparator	0 can not be	used as a trigg	jer.							
	1	Comparator	0 can be use	d as a trigger.	Note 3							
	TKBPAFCM2p		Operatio	n mode selecti	on for forced	d output stop fu	nction 2					
	0	Forced outp cleared at th	ut stop functio e next counte	on 2 starts with er period. ^{Note d}	trigger inpu 1	t, and forced or	utput stop fund	ction 2 is				
	1	Forced outp cleared at th	ut stop functio e next counte	on 2 starts with er period follow	trigger inpu ing detection	t, and forced ou n of the reverse	utput stop fund e edge of the t	ction 2 is rigger. ^{Note}				
		1										
	ТКВРАН252р2		Comparat	or trigger selec	ction for force	ed output stop i	function 1					
	0	Comparator 5 can not be used as a trigger.										
	1	Comparator	5 can be use	d as a trigger.								
	TKBPAHZS2p1		Comparat	or trigger selec	tion for force	ed output stop f	function 1					
	0	Comparator	4 can not be	used as a trio	ber.							
	1	Comparator	4 can be use	d as a trigger.	Note 2							
	TKBPAHZS2p0		Comparat	or trigger seled	ction for force	ed output stop f	function 1					
	0	Comparator	0 can not be	used as a trig	ger.							
	1	Comparator	0 can be use	d as a trigger	Note 3							



Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (2/2)

TKBPAHCM2p1	TKBPAHCM2p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT2p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT2p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT2p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT2p) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT2p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT2p) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD2p1	TKBPAMD2p0	Output status selection when executing forced output stop function			
		Forced output stop function 1	Forced output stop function 2		
0	0	Hi-Z output	Output fixed at low level		
0	1	Hi-Z output	Output fixed at high level		
1	0	Output fixed at low level	Output fixed at low level		
1	1	Output fixed at high level	Output fixed at high level		

- Notes 1. When INTP20 is used as the forced output stop function 2, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - When CMP4 or CMP5 is used as the timer KB forced output stop function, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.
 - When CMP0 is used as the timer KB forced output stop function, set CMP0STEN = 1. For details, see 14. 5
 Caution for Using Timer KB Simultaneous Operation Function.
 - 4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).
- Cautions 1. During timer operation, setting the other bits of the TKBPACTL2p register is prohibited. However, the TKBPACTL2p register can be refreshed (the same value is written).
 - 2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1



5. Figure 14-1. Block Diagram of Comparator

Incorrect names of the noise filter and the edge detection circuit in the block diagram are revised, and Note is added.







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Address: F05C6H After reset: 00H RW Symbol 7 <6> <5> <4> 3 2 <1> PFSEL0 0 CMP2STEN CMP0STEN PNFEN ADTRG11 ADTRG10 TMRSTEN1 TMRSTEN1 TMRSTEN1 0 STOP mode clear disabled 0 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) CMP0STEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) VEXPOND STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) VEXPOND Use/Do not use external interrupt INTP20 noise filter 1 Do not use noise filter 1 Do not use noise filter Vextmal interrupt INTP21 function select 0 External interrupt INTP21 function select External interrupt INTP21 function select 1 Time restart function (can not be generated external interrupt, and cannot release standby mode) 1 Time restart function (cannot be generated external interrupt, but canno		Figure 1	4-12. Format o	f Periphe	eral Funct	ion Switch I	Register 0 (PFSEL0)			
Symbol 7 <6> <5> <4> 3 2 <1> <0> PFSEL0 0 CMP2STEN CMP0STEN PNFEN ADTRG11 ADTRG10 TMRSTEN1 TMRSTEN 0 STOP mode clear disabled	Address: F	05C6H	After reset: 00H	R/W							
PFSEL0 0 CMP2STEN CMPOSTEN PNFEN ADTRG11 ADTRG10 TMRSTEN1 TMRSTEN1 0 STOP Comparator 2 detection interrupt (INTCMP2) switching 0 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) CMPOSTEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use/Do not use external interrupt INTP20 noise filter 1 Do not use noise filter 0 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select <	Symbol	7	<6> <	<5>	<4>	3	2	<1>	<0>		
CMP2STEN Comparator 2 detection interrupt (INTCMP2) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) CMPOSTEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 Timer restart function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEND External interrupt INTP20 function select 0 External interrupt function (can be generated external i	PFSEL0	0	CMP2STEN CMP	OSTEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0		
O STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) CMPOSTEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 Do not use noise filter 1 Do not use noise filter 1 TMRSTEN1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt INTP20 function select		CMP2STEN		Comparator 2 detection interrupt (INTCMP2) switching							
1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) CMPOSTEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 Do not use noise filter 1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function)		0	STOP mode clear	disabled							
(Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) CMPOSTEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer mode)		1	STOP mode clear	enabled, b	out only whe	n not using no	oise filter				
CMPOSTEN Comparator 0 detection interrupt (INTCMP0) switching 0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 Do not use noise filter 1 De not use noise filter 1 TMRSTEN1 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer			(Can be set when o	operating i	n low-powe	RTC mode (RTCLPC = 1	in the OSMC	register)		
0 STOP mode clear disabled 1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 Do not use noise filter 1 Do not use noise filter 0 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEND External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function (cannot be generated external interrupt, and cannot release standby mode)		CMP0STEN Comparator 0 detection interrupt (INTCMP0) switching									
1 STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 TMRSTEN1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer			STOP mode clear disabled								
Image: Construction of the operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction of the operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction of the operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction of the operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction of the operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction of the operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction operating in low-power RTC mode (RTCLPC = 1 in the OSMC register) Image: Construction operating interrupt INTP20 function select Image: Construction operated external interrupt, but cannot be used for timer restart function (can be generated external interrupt, but cannot be used for timer mode) Image: Construction operated external interrupt, and cannot release standby mode) Image: Construction operated external interrupt (INTP20 function select) Image: Construction operated external interrupt, but cannot be used for timer Image: Construction operated external interrupt, but cannot be used for timer		1	STOP mode clear enabled, but only when not using noise filter								
PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter 1 Do not use noise filter 0 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, and cannot release standby mode)			(Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register						register)		
PNFEN Use/Do not use external interrupt INTP20 noise filter 0 Use noise filter 1 Do not use noise filter Image: State of the st									0 /		
0 Use noise filter 1 Do not use noise filter TMRSTEN1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer		PNFEN		Use/Do	not use ext	ernal interrupt	INTP20 nois	e filter			
1 Do not use noise filter Image: TMRSTEN1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) Image: TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer		0	Use noise filter								
TMRSTEN1 External interrupt INTP21 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer		1	Do not use noise fi	lter							
0 External interrupt function (can be generated external interrupt, but cannot be used for timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer		TMRSTEN1		E	xternal inter	rupt INTP21 f	unction select	:			
1 Timer restart function) 1 Timer restart function (cannot be generated external interrupt, and cannot release standby mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer		0	External interrupt function (can be generated external interrupt, but cannot be used for timer								
mode) TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer		1	Timer restart function)	ion (canno	t be genera	ed external in	terrupt, and c	annot release	standby		
TMRSTEN0 External interrupt INTP20 function select 0 External interrupt function (can be generated external interrupt, but cannot be used for timer			mode)								
0 External interrupt function (can be generated external interrupt, but cannot be used for timer		TMRSTEN0		E	xternal inter	rupt INTP20 fi	unction select				
rostart function)		0	External interrupt f	unction (ca	an be gener	ated external i	nterrupt, but	cannot be use	d for timer		
1 Timer restart function (cannot be generated external interrupt, and cannot release standby		1	Timer restart function	ion (canno	t he genera	ed external in	terrunt and c	annot release	standby		
mode)			Timer restart function (cannot be generated external interrupt, and cannot release standby mode)						standby		
			mouc)						-		



	— ••••••••••••••••••••••••••••••••••••								
	Figure	14-12. Form	at of Peripl	neral Funct	tion Switch I	Register 0 (I	PFSEL0)		
Address [.]	F05C6H	After reset: 00	H R/W						
, laurooo.	1000011					_		_	
Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>	1
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0	
	CMP2STEN		Comparate	or 2 detection	n interrupt (INT	CMP2) switch	Note 1		1
	0	Signal via digi	tal edge deter	ct circuit is se	elected STO	P mode releas	se is disabled		-
	1	Forced output	stop request	signal is sele	ected.				-
		STOP mode r	elease is enal	bled, but only	/ when not usir	ng noise filter.			
		(Can be set w	Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)						
									-
	CMP0STEN		Comparate	or 0 detectior	n interrupt (INT	CMP0) switch	ning Note 1		
	0	Signal via digi	tal edge dete	ct circuit is se	elected. STO	P mode releas	se is disabled		_
	1	Forced output	stop request	signal is sele	ected.				
		STOP mode r	elease is ena	bled, but only	/ when not usir	ng noise filter.			
		(Can be set w	hen operating	in low-powe	er RTC mode (I	RTCLPC = 1 i	n the OSMC	register)	
	PNEEN Use/Do not use external interrupt INTP20 noise filter								1
	0	Use noise filter							-
	1 Do not use noise filter							-	
									J
			TMRSTEN1 External interrupt INTP21 function switching Note 2						
	TMRSTEN1		Exter	nal interrupt	INTP21 function	on switching ^N	ote 2		1
	TMRSTEN1	External interr	Exter upt function is	nal interrupt	INTP21 function (STOP mode r	on switching ^N release is enal	ote 2 bled, but canr	not be used]
	TMRSTEN1 0	External interr for timer resta	Exter upt function is rt function)	nal interrupt s selected.	INTP21 functio	on switching ^N elease is enal	ote 2 bled, but cann	not be used	
	TMRSTEN1 0 1	External interr for timer resta Timer restart t	Exter upt function is rt function) iunction is sele	rnal interrupt s selected. ected. (STC	INTP21 function (STOP mode r DP mode relea	on switching ^N elease is enal se is disabled	bled, but canr , but can be u	not be used	
	TMRSTEN1 0 1	External interr for timer resta Timer restart f restart functio	Exter upt function is rt function) function is sele n)	nal interrupt s selected. ected. (STC	INTP21 function (STOP mode r DP mode relea	on switching ^N elease is enal se is disabled	bled, but canr , but can be u	not be used used for timer	
	TMRSTEN1 0 1	External interr for timer resta Timer restart f restart functio	Exter upt function is rt function) function is sel n)	nal interrupt s selected. ected. (STC	INTP21 function (STOP mode r DP mode relea	on switching ^N release is enal se is disabled	bled, but canr , but can be u	not be used used for timer	
	TMRSTEN1 0 1 TMRSTEN0	External interr for timer resta Timer restart t restart functio	Exter rupt function is rt function) function is sele n) Exter	nal interrupt s selected. ected. (STC	INTP21 function (STOP mode r DP mode relean INTP20 function	on switching ^N release is enal se is disabled on switching ^N	bled, but cann , but can be u ote 2	not be used used for timer	
	TMRSTEN1 0 1 TMRSTEN0 0	External interr for timer resta Timer restart f restart functio External interr for timer resta	Exter upt function is rt function is sel n) Exter upt function is rt function)	rnal interrupt s selected. ected. (STC	INTP21 function (STOP mode relean DP mode relean INTP20 function (STOP mode r	on switching ^N release is enal se is disabled on switching ^N release is enal	ote 2 bled, but canr , but can be u lote 2 bled, but canr	not be used used for timer not be used]
	TMRSTEN1 0 1 TMRSTEN0 0 1	External interr for timer restart f restart functio External interr for timer restart	Exter upt function is rt function is sele n) Exter upt function is rt function)	rnal interrupt s selected. ected. (STC rnal interrupt s selected.	INTP21 function (STOP mode relean DP mode relean INTP20 function (STOP mode relean function 2 is s	on switching ^N elease is enal se is disabled on switching ^N elease is enal	ote 2 bled, but canr , but can be u lote 2 bled, but canr	not be used used for timer not be used ease is	



7. 14.5 Caution for Using Timer KB Simultaneous Operation Function

As respects of INTP2m and comparator, Caution for Using Timer KB Simultaneous Operation Function is added.

Incorrect:

No applicable item

Correct:

14.5 Caution for Using Timer KB Simultaneous Operation Function

In addition to their use as an external interrupt input, the INTP2m pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. The settings in peripheral function switch register 0 (PFSEL0) and the edge selection registers must be specified according to the function used. The width of the active signal required until each function starts operating differs.

When using INTP2m or the comparator output signal, refer to Tables 14-4 to 14-6 to specify the necessary register settings, and configure external circuits so that the required active signal width is assured.

Eurotien	Peripheral enable	Edge setting	Necessary activ	e signal width to operat	e each function
Function	register setting	registers	Interrupt	Forced output stop	Timer restart
External interrupt	TMRSTENm = 0	EGPn, EGNn	To 1 µs	-	-
(STOP release is					
enabled)					
Forced output stop	TMRSTENm = 1	CEGPp, CEGNp	55 to 215 ns ^{Note 3} +	55 to 215 ns	-
Note 1		Note 2	2 to 3 clocks Note 4	Note 3, 5	
Timer restart	TMRSTENm = 1	CEGPp, CEGNp	55 to 215 ns ^{Note 3} +	-	55 to 215 ns ^{Note 3} +
			2 to 3 clocks Note 4		2 to 3 clocks Note 4, 6

Table 14-4. Relationship of INTP2m function, register settings, and active signal width

Figure 14-18. Generation Timing of Forced Output Stop Signal and Timer Restart Request Signal by INTP2m



Notes 1. Only INTP20 can be used as a trigger for forced output stop function 2.

- 2. The active level of INTP20 (used for forced output stop function 2) is high. Edge selection is only applied to detection of an interrupt signal.
- 3. 5 to 15 ns when noise filtering on INTP20 is disabled (PNFEN = 1)
- **4.** For f_{CLK} or f_{PLL} (when PLLON = 1)
- **5.** An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.



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Notes 6. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

Remark m = 0, 1 n = 20, 21 p = 7, 6

Table 14-5. Relationship of comparator 0 and 2 functions, register settings, and active signal width

Function	Peripheral enable	Edge setting	Necessary activ	e signal width to operat	te each function
Function	register setting	registers	Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is enabled ^{Note 1})	CMPnSTEN = 1	Rising edge only Note 2	To 150 ns ^{Note 3}	-	-
External interrupt (STOP release is disabled)	CMPnSTEN = 0	CEGPn, CEGNn	To 150 ns ^{Note 3} + 2 to 3 clocks ^{Note 4, 5}	-	-
Forced output stop	CMPnSTEN = 1	Note 6	To 150 ns Note 3	To 150 ns ^{Note 3, 7}	-
Timer restart	CMPnSTEN = 0	CEGPn, CEGNn	To 150 ns ^{Note 3} + 2 to 3 clocks ^{Note 4, 5}	-	To 150 ns ^{Note 3} + 2 to 3 clocks ^{Note 4, 5}

Figure 14-19. Generation Timing of Forced Output Stop Request Signal by Comparator 0 and 2 (CMPnSTEN = 1)



Figure 14-20. Generation Timing of Timer Restart Request Signal by Comparator 0 and 2 (CMPnSTEN = 0)



Notes 1. When noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL)

- 2. To change the level of the edge direction, invert the comparator output signal by using the CnINV bit in the comparator n control register (CnCTL).
- **3.** This is the time required when noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL).

If a setting other than "0, 0" is specified, the specified noise elimination width is added.

4. For f_{CLK} or f_{PLL} (when PLLON = 1)



- **Notes 5.** Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.
 - 6. The active level of INTP20 (used for forced output stop function 2) is high.
 - **7.** An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

Remark n = 0, 2

Table 14-6. Relationship of comparator 1, 3, 4, and 5 functions, register settings, and active signal width

Function	Peripheral enable	Edge setting	Necessary active signal width to operate each function				
Function	register setting	registers	Interrupt	Forced output stop	Timer restart		
External interrupt	-	CEGPn, CEGNn	To 150 ns ^{Note 1} +	-	-		
(STOP release is			2 to 3 clocks Note 2, 3				
disabled)							
Forced output stop	-	Note 4	To 150 ns ^{Note 2} +	To 150 ns ^{Note 2, 5}	-		
			2 to 3 clocks Note 3, 4				
Timer restart Note 6	-	CEGPn, CEGNn	To 150 ns ^{Note 2} +	-	To 150 ns ^{Note 2} +		
			2 to 3 clocks Note 3, 4	1	2 to 3 clocks Note 3, 4		

Figure 14-21. Generation Timing of Forced Output Stop Request Signal and Timer Restart Request Signal by



Comparator 1, 3, 4, and 5

- **Notes 1.** When noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL). If a setting other than "0, 0" is specified, the specified noise elimination width is added.
 - **2.** For f_{CLK} or f_{PLL} (when PLLON = 1)
 - 3. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.
 - 4. The active level of INTP20 (used for forced output stop function 2) is high.
 - **5.** An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.
 - 6. The timer restart function can be used for comparator 1 and 3 only .
 - **7.** An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

Remark n = 1, 3 to 5



8. Timing Chart of SNOOZE Mode Operation (p.666, 667, 669)

Incorrect the clock request signal (internal signal) timing is revised.





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Incorrect the timing chart of clock request signal (internal signal) and SDR01 is revised.







Incorrect the clock request signal (internal signal) timing chart is revised.







9. Table 20-1. Interrupt Source List (2/3)

Note for the interrupt source list is added.

Incorrect:

- **Notes 1.** The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.
 - 2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 20-1.
 - 3. INTCMP1. INTCMP3. INTCMP4. and INTCMP5 cannot be used to clear the STOP mode.

Correct:

- **Notes 1.** The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.
 - 2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 20-1.
 - INTCMP1, INTCMP3, INTCMP4, and INTCMP5 cannot be used to clear the STOP mode.
 About interrupt generation timing, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.



10. Figure 20-1. Basic Configuration of Interrupt Function

Incorrect the basic configuration of interrupt function is revised.

Incorrect:

(B) External maskable interrupt (INTPn, INTCMPm)



- IF: Interrupt request flag
- IE: Interrupt enable flag
- ISP0: In-service priority flag 0
- ISP1: In-service priority flag 1
- MK: Interrupt mask flag
- PR0: Priority specification flag 0
- PR1: Priority specification flag 1
- **Remark** 20-pin: n = 0, 20, 21, 22, m = 0 to 3

30-pin: n = 0, 4, 11, 20 to 23, m = 0 to 5

38-pin: n = 0, 3, 4, 9 to 11, 20 to 23, m = 0 to 5



Correct:

(B) External maskable interrupt (INTPn, INTCMPm)





11. <u>Table 21-1. Operating Statuses in HALT Mode (2/2)</u>

Incorrect description about the comparator operation in HALT mode is revised.

Incorrect:

HALT Mode Setting		When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock				
Item		When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f _{Exs})			
System clock		Clock supply to the CPU is stopped	Clock supply to the CPU is stopped			
Main system clock fin		Operation disabled				
	fx					
	f _{EX}					
Subsystem clock	fхт	Operation continues (cannot be stopped)	Cannot operate			
	fexs	Cannot operate	Operation continues (cannot be stopped)			
fiL.		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops				
CPU		Operation stopped				
Code flash memory						
Data flash memory						
RAM						
Port (latch)		Status before HALT mode was set is retained				
Timer array unit		Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).				
Timer KB0 to KB2						
Timer KC0						
Real-time clock (RTC)		Operable				
12-bit interval timer						
Watchdog timer		See CHAPTER 11 WATCHDOG TIMER				
A/D converter		Operation disabled				
Programmable gain amplifier		Operable (However, this is not used, since the operation has been disabled for the A/D converter that is the destination for input of the PGA output signal)				
Comparator		Operable (When in the low-consumption RTC mode (RTCLPC = 1 in the OSMC register), this can be used only when the STOP mode cancel is set (CMPnSTEN = 1 in the PESEL0 register) by the comparator interrupt detection and the noise filter is not used ($n = 0, 2$))				



Correct:

HALT Mode Setting		When HALT Instruction Is Executed Wh	ile CPU Is Operating on Subsystem Clock					
Item		When CPU Is Operating on XT1 Clock (fxr)	When CPU Is Operating on External Subsystem Clock (f _{EXS})					
System clock		Clock supply to the CPU is stopped						
Main system clock fin		Operation disabled						
	fx							
	fex							
Subsystem clock	fхт	Operation continues (cannot be stopped)	Cannot operate					
	fexs	Cannot operate	Operation continues (cannot be stopped)					
fiL		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops						
CPU		Operation stopped						
Code flash memory								
Data flash memory								
RAM								
Port (latch)		Status before HALT mode was set is retained						
Timer array unit		Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).						
Timer KB0 to KB2		-						
Timer KC0								
Real-time clock (RTC)		Operable						
12-bit interval timer								
Watchdog timer		See CHAPTER 11 WATCHDOG TIMER						
A/D converter		Operation disabled						
Programmable gain amplifier		Operable (However, this is not used, since the operation has been disabled for the A/D converter that is the destination for input of the PGA output signal)						
Comparator		Only CMP0 and CMP2 are operable. (When in the low-consumption RTC mode (RTCLPC = 1 in the OSMC register), CMPn can be used only when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. ($n = 0, 2$))						



12. Table 21-2. Operating Statuses in STOP Mode

Incorrect description about the comparator operation in STOP mode is revised.

Incorrect:

STOP Mode Setting		Setting	When STOP Instruction Is Executed While CPU Is Operating on Main System Clock				
Item			When CPU Is Operating on High-speed On-chip Oscillator Clock (fH) When CPU Is Operating on X1 Clock (fx) When CPU Is Operating External Main System Clock (fEX)				
System clock			Clock supply to the CPU is stop	ped			
Main system	clock f	fін	Stopped				
fx							
	f	fex					
Subsystem clock fxT			Status before STOP mode was	set is retained			
	f	fexs					
fı∟			Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops				
CPU			Operation stopped				
Code flash memo	ory						
Data flash memo	ry						
RAM							
Port (latch)			Status before STOP mode was set is retained				
Timer array unit			Operation disabled				
Timer KB0 to KB	2						
Timer KC0							
Real-time clock (RTC)		Operable				
12-bit interval tim	ier						
Watchdog timer			See CHAPTER 11 WATCHDO	DG TIMER			
A/D converter			Wakeup operation is enabled (switching to the SNOOZE mode)				
Programmable g	ain ampli	ifier	Operable				
Comparator			Operable (Only for channels set to enable cancellation of STOP mode and when digital filter is not used)				



STOP Mode Setting		Setting	When STOP Instruction Is	When STOP Instruction Is Executed While CPU Is Operating on Main System Clock					
Item			When CPU Is Operating on High-speed On-chip Oscillator Clock (fiH) When CPU Is Operating on X1 Clock (fx) When CPU Is Operating on External Main System Clock (fEX)						
Sy	stem clock		Clock supply to the CPU is stop	Clock supply to the CPU is stopped					
Main system clock fill			Stopped						
	fx								
		f _{EX}							
	Subsystem clock	fхт	Status before STOP mode was	set is retained					
		fexs							
fiL			Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops						
CF	ال		Operation stopped						
Сс	de flash memory								
Da	ata flash memory								
R/	λM								
Po	ort (latch)		Status before STOP mode was set is retained						
Tir	mer array unit		Operation disabled						
Tir	mer KB0 to KB2								
Tir	mer KC0								
Re	eal-time clock (RTC)		Operable						
12	-bit interval timer								
Wa	atchdog timer		See CHAPTER 11 WATCHD	OG TIMER					
A/D converter			Wakeup operation is enabled (switching to the SNOOZE mode)						
Programmable gain amplifier			Operable						
Comparator			Only CMP0 and CMP2 are operable when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. ($n = 0$, 2)						



13. <u>Table 21-3.</u> Operating Statuses in SNOOZE Mode

Incorrect description about the comparator operation in SNOOZE mode is revised.

Incorrect:

STOP Mode	e Setting	When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode			
		When CPU Is Operating on High-speed On-chip Oscillator Clock (fill)			
System clock		Clock supply to the CPU is stopped			
Main system clock	fін	Operation started			
	fx	Stopped			
	fex				
Subsystem clock	fхт	Use of the status while in the STOP mode continues			
	fexs				
fı∟		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops			
CPU		Operation stopped			
Code flash memory					
Data flash memory					
RAM					
Port (latch)		Use of the status while in the STOP mode continues			
Timer array unit		Operation disabled			
Timer KB0 to KB2					
Timer KC0					
Real-time clock (RTC)		Operable			
12-bit interval timer					
Watchdog timer		See CHAPTER 11 WATCHDOG TIMER			
A/D converter		Operable			
Programmable gain am	plifier	Operable			
Comparator		Operable (Only for channels set to enable cancellation of STOP mode and when digital filter is not used)			



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STOP Mode	e Setting	When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode			
		When CPU Is Operating on High-speed On-chip Oscillator Clock (fin)			
System clock		Clock supply to the CPU is stopped			
Main system clock	fін	Operation started			
	fx	Stopped			
	f _{EX}				
Subsystem clock	fхт	Use of the status while in the STOP mode continues			
	f _{EXS}				
fiL		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops			
CPU		Operation stopped			
Code flash memory					
Data flash memory					
RAM					
Port (latch)		Use of the status while in the STOP mode continues			
Timer array unit		Operation disabled			
Timer KB0 to KB2					
Timer KC0					
Real-time clock (RTC)		Operable			
12-bit interval timer					
Watchdog timer		See CHAPTER 11 WATCHDOG TIMER			
A/D converter		Operable			
Programmable gain am	plifier	Operable			
Comparator		Only CMP0 and CMP2 are operable when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0 2)			



32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics 14.

Descriptions of the data memory STOP mode low supply voltage data retention characteristics are added.

Incorrect:

32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, \text{ Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.44 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



Correct:

32.7 RAM Data Retention Characteristics

 $(T_A = -40 \text{ to } +105^{\circ}\text{C}, \text{ Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.44 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained.

Therefore, set STOP mode before the supplied voltage is below the operation voltage range.





33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics 15.

Descriptions of the data memory STOP mode low supply voltage data retention characteristics are added.

Incorrect:

33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

$(T_A = -40 \text{ to } +125^{\circ}\text{C}, \text{ Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.47 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



Correct:

33.7 RAM Data Retention Characteristics

 $(T_A = -40 \text{ to } +125^{\circ}\text{C}, \text{ Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.47 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained.

Therefore, set STOP mode before the supplied voltage is below the operation voltage range.



