# RENESAS

# ISL9005A

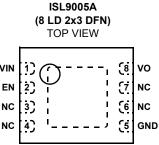
LDO with Low ISUPPLY, High PSRR

ISL9005A is a high performance Low Dropout linear regulator capable of sourcing 300mA current. It has a low standby current and high-PSRR and is stable with output capacitance of  $1\mu$ F to  $10\mu$ F with ESR of up to  $200m\Omega$ .

The ISL9005A has a high PSRR of 75dB and an output noise of less than  $45\mu V_{RMS}$ . When coupled with a no load quiescent current of 50µA, (typical) and 0.1µA shutdown current, the ISL9005A is an ideal choice for portable wireless equipment.

Several different fixed voltage outputs are standard. Output voltage options for each LDO range are from 1.5V to 3.3V. Other output voltage options may be available upon request.

## Pinout



# Features

- 300mA high performance LDO
- · Excellent transient response to large current steps
- Excellent load regulation: <0.1% voltage change across full range of load current
- High PSRR: 75dB @ 1kHz
- Wide input voltage capability: 2.3V to 6.5V
- Very low guiescent current: 50µA
- Low dropout voltage: typically 200mV @ 300mA
- Low output noise: typically 45µV<sub>RMS</sub> @ 100µA (1.5V)
- Stable with 1µF to 10µF ceramic capacitors
- Soft-start to limit input current surge during enable
- · Current limit and overheat protection
- ±1.8% accuracy over all operating conditions
- Tiny 2mmx3mm 8 Ld DFN package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

#### Applications

- · PDAs, cell phones and smart phones
- · Portable instruments, MP3 players
- · Handheld devices, including medical handhelds

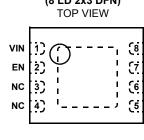
PART NUMBER (Notes 1, 2)	PART MARKING	VO VOLTAGE (V) (Note 3)	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-Free)	PKG. DWG. #
ISL9005AIRNZ-T	EBV	3.3	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9005AIRKZ-T	EBR	2.85	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9005AIRJZ-T	EBP	2.8	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9005AIRFZ-T	EBN	2.5	-40 to +85	8 Ld 2x3 DFN	L8.2x3
SL9005AIRCZ-T	EBM	1.8	-40 to +85	8 Ld 2x3 DFN	L8.2x3
SL9005AIRBZ-T	EBL	1.5	-40 to +85	8 Ld 2x3 DFN	L8.2x3

## Ordering Information

NOTES:

- 1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- 2. Please refer to TB347 for details on reel specifications.
- 3. For other output voltages, contact Intersil Marketing.







FN6452 Rev 2.00 November 20, 2015

#### **Absolute Maximum Ratings**

Supply Voltage (VIN) +7.1	V
VO Pin	V
All Other Pins	V

#### **Recommended Operating Conditions**

Ambient Temperature Range (T <sub>A</sub> )	40°C to +85°C
Supply Voltage (VIN)	2.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 4, 5)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)
8 Ld 2x3 DFN Package	69	10
Junction Temperature Range	40°	°C to +125°C
Operating Temperature Range	4(	0°C to +85°C
Storage Temperature Range	65°	°C to +150°C
Pb-free reflow profile		ee link below
http://www.intersil.com/pbfree/Pb-FreeR	eflow.asp	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

#### NOTES:

- 4. θ<sub>JA</sub> is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- 5. For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications	Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature
-	range of the device as follows: $T_A = -40^{\circ}$ C to +85°C; $V_{IN} = (V_O + 0.5V)$ to 5.5V with a minimum $V_{IN}$ of 2.3V;
	$C_{IN} = 1\mu F; C_O = 1\mu F.$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	ТҮР	MAX (Note 8)	UNITS
DC CHARACTERISTICS	<u> </u>		1	1		1
Supply Voltage	V <sub>IN</sub>		2.3		6.5	V
Ground Current		Quiescent condition: $I_O = 0\mu A$				
	I <sub>DD</sub>	LDO active		50	75	μA
Shutdown Current	IDDS	LDO disabled @ +25°C		0.1	1.0	μA
UVLO Threshold	V <sub>UV+</sub>		1.9	2.1	2.3	V
	V <sub>UV-</sub>		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Initial accuracy at $V_{IN}$ = $V_O$ + 0.5V, $I_O$ = 10mA, $T_J$ = +25°C	-0.7		+0.7	%
		$V_{IN} = V_O + 0.5V$ to 5.5V, $I_O = 10\mu A$ to 300mA, $T_J = +25^{\circ}C$	-0.8		+0.8	%
		$V_{IN} = V_O + 0.5V$ to 5.5V, $I_O = 10\mu A$ to 300mA, T <sub>J</sub> = -40°C to +125°C	-1.8		+1.8	%
Maximum Output Current	I <sub>MAX</sub>	Continuous	300			mA
Internal Current Limit	I <sub>LIM</sub>		350	475	600	mA
Dropout Voltage (Note 7)	V <sub>DO1</sub>	I <sub>O</sub> = 300mA; V <sub>O</sub> < 2.5V		300	500	mV
	V <sub>DO2</sub>	$I_O$ = 300mA; 2.5V $\leq V_O \leq$ 2.8V		250	400	mV
	V <sub>DO3</sub>	I <sub>O</sub> = 300mA; V <sub>O</sub> > 2.8V		200	325	mV
Thermal Shutdown Temperature	T <sub>SD+</sub>			145		°C
	T <sub>SD-</sub>			110		°C
AC CHARACTERISTICS	-					
Ripple Rejection (Note 6)		I <sub>O</sub> = 10mA, V <sub>IN</sub> = 2.8V (min), V <sub>O</sub> = 1.8V				
		@ 1kHz		75		dB
		@ 10kHz		60		dB
		@ 100kHz		40		dB
Output Noise Voltage (Note 6)		I <sub>O</sub> = 100μA, V <sub>O</sub> = 1.5V, T <sub>A</sub> = +25°C BW = 10Hz to 100kHz		45		μV <sub>RMS</sub>

### **Electrical Specifications**

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ;  $V_{IN} = (V_O + 0.5V)$  to 5.5V with a minimum  $V_{IN}$  of 2.3V;  $C_{IN} = 1\mu$ F;  $C_O = 1\mu$ F. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	түр	MAX (Note 8)	UNITS
DEVICE START-UP CHARACTE	RISTICS					
Device Enable Time	t <sub>EN</sub>	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO (nom)		250	500	μs
LDO Soft-start Ramp Rate	t <sub>SSR</sub>	Slope of linear portion of LDO output voltage ramp during start-up		30	60	µs/V
EN PIN CHARACTERISTICS						
Input Low Voltage	VIL		-0.3		0.5	V
Input High Voltage	V <sub>IH</sub>		1.4		V <sub>IN</sub> + 0.3	V
Input Leakage Current	I <sub>IL</sub> , I <sub>IH</sub>				0.1	μA
Pin Capacitance	C <sub>PIN</sub>	Informative		5		pF

NOTES:

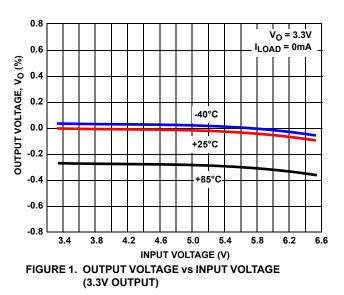
6. Limits established by characterization and are not production tested.

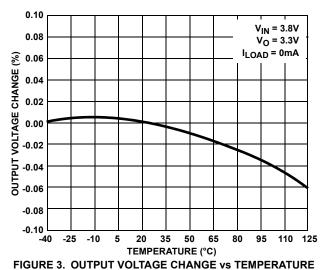
7. VOx = 0.98\*VOx(NOM); Valid for VOx greater than 1.85V.

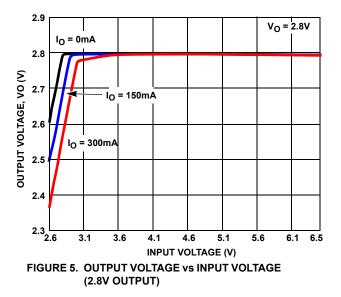
8. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

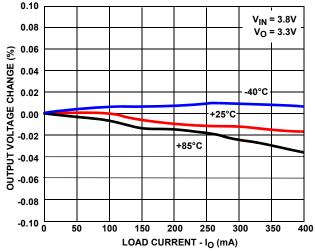


## Typical Performance Curves

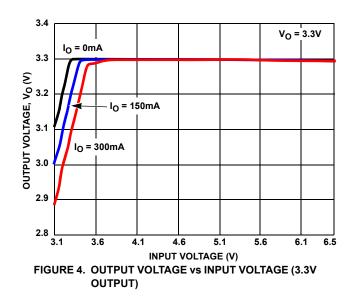


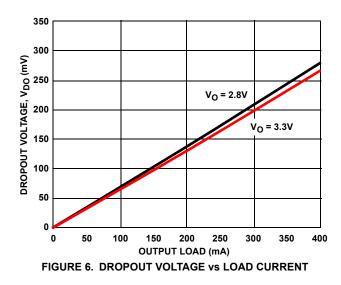








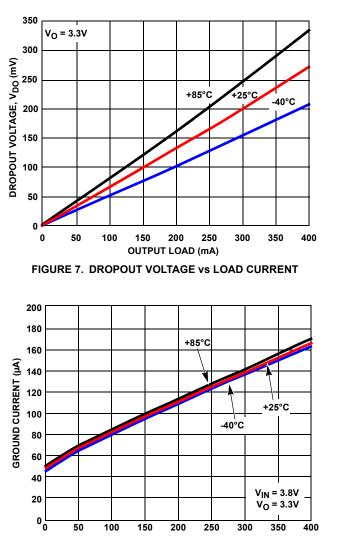




FN6452 Rev 2.00 November 20, 2015

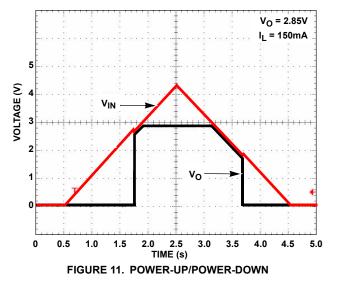


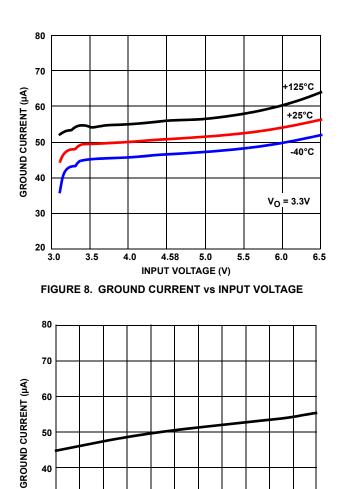
## Typical Performance Curves (Continued)





LOAD CURRENT (mA)







35

**TEMPERATURE (°C)** 

50

65 80 95

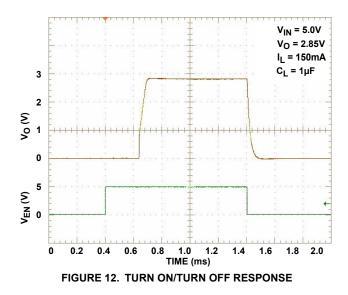
50

40

30

20

, -40 -25 -10 5 20



FN6452 Rev 2.00 November 20, 2015 V<sub>IN</sub> = 3.8V

V<sub>O</sub> = 3.3V

110 125

I<sub>LOAD</sub> = 0μA

## Typical Performance Curves (Continued)

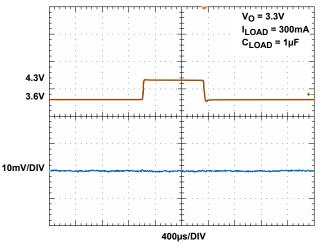
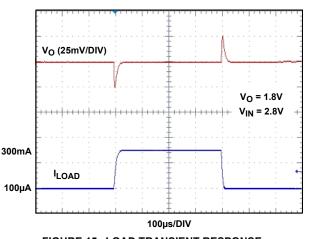


FIGURE 13. LINE TRANSIENT RESPONSE, 3.3V OUTPUT





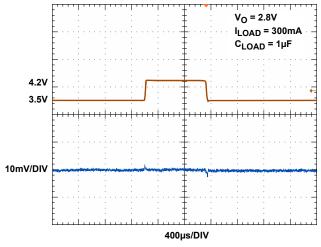
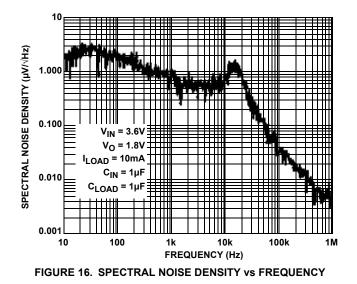
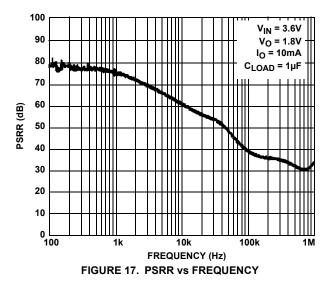


FIGURE 14. LINE TRANSIENT RESPONSE, 2.8V OUTPUT





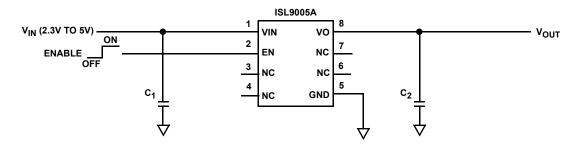
FN6452 Rev 2.00 November 20, 2015



# **Pin Description**

PIN NUMBER	PIN NAME	DESCRIPTION
1	VIN	Supply Voltage/LDO Input: Connect a 1µF capacitor to GND.
2	EN	LDO Enable.
3	NC	Do not connect.
4	NC	Do not connect.
5	GND	GND is the connection to system ground. Connect to PCB Ground plane.
6	NC	Do not connect.
7	NC	Do not connect.
8	VO	LDO Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended).

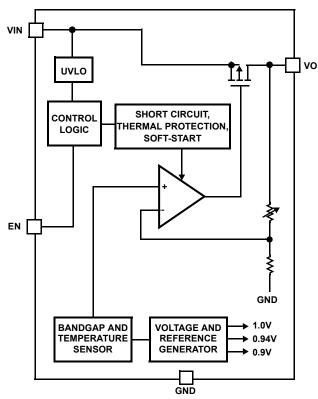
## **Typical Application**



C1, C2: 1µF X5R CERAMIC CAPACITOR



### Block Diagram



## Functional Description

The ISL9005A contains all circuitry required to implement a high performance LDO. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9005A adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, and soft-start. Smart thermal shutdown protects the device against overheating.

#### **Power Control**

The ISL9005A has an enable pin (EN) to control power to the LDO output. When EN is low, the device is in shutdown mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than  $0.1\mu$ A. When the enable pin is asserted, the device first monitors the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power-up. Once the references are stable, a fast-start circuit powers up the LDO. During operation, whenever the VIN voltage drops below about 1.84V, the ISL9005A immediately disables the LDO output. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

#### **Reference Generation**

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference and other voltage references required for current generation and over-temperature detection.

The current generator outputs references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

#### LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9005A provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and ESR less than 200m $\Omega$ , and the design is performance-optimized for a 1µF output capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not recommended as LDO performance improvement is minimal.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge. The ISL9005A provides short-circuit protection by limiting the output current to about 425mA.

The LDO uses an independently trimmed 1V reference as its input. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory.

#### **Overheat Detection**

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +140°C, if the LDO is sourcing more than 50mA it shuts down until the die cools sufficiently. Once the die temperature falls back below about +110°C, the disabled LDO is re-enabled and soft-start automatically takes place.

## **Revision History**

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
November 20, 2015	FN6452.2	<ul> <li>Updated Ordering Information Table on page 1.</li> <li>Added Revision History.</li> <li>Added About Intersil Verbiage.</li> <li>Updated POD L8.2X3 to latest revision changes are as follow: Bottom View:</li> <li>Changed exposed pad height from 1.80 +/-0.10 to 1.80 +0.10/-0.15</li> <li>Changed exposed pad width from 1.65 +/-0.10 to 1.65 +0.10/-0.15</li> <li>Side View:</li> <li>Changed 0.05 to 0.05 MAX</li> <li>Converted to new POD standards by adding land pattern and moving dimensions from table onto drawing. Tiebar Note 5 updated</li> <li>From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).</li> </ul>

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at <u>www.intersil.com</u>.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

© Copyright Intersil Americas LLC 2007-2015. All Rights Reserved. All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at <u>www.intersil.com/en/support/qualandreliability.html</u>

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

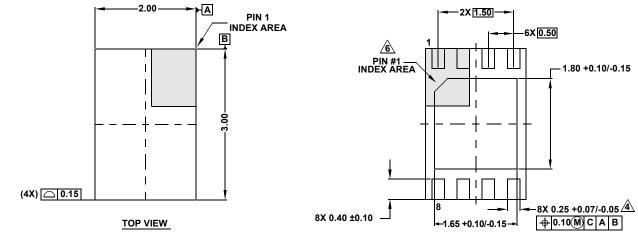
FN6452 Rev 2.00 November 20, 2015



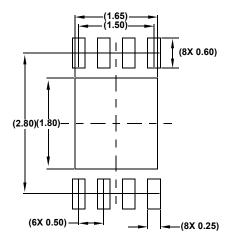
# Package Outline Drawing

## L8.2x3

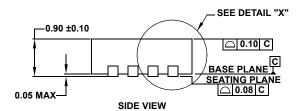
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE Rev 2, 3/15

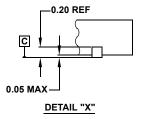


#### BOTTOM VIEW



#### TYPICAL RECOMMENDED LAND PATTERN





#### NOTES:

- 1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
- 2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
- 3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
- A Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
- 5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
- A The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
- 7. Compies to JEDEC MO-229 VCED-2.

