TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7SP300WBG

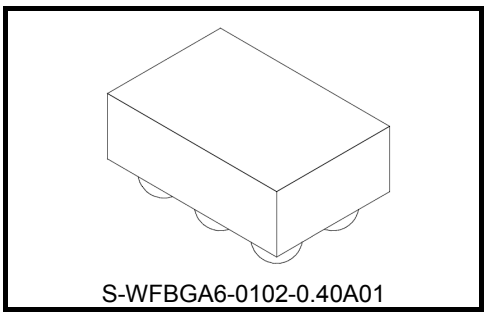
Dual supply 2-Input NAND Gate with Level Translator

The TC7SP300 is a dual supply, advanced high-speed CMOS 2-input dual supply voltage interface NAND gate fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 1.2-V, 1.5-V, 1.8-V, or 2.5-V bus and a 1.8-V, 2.5-V or 3.3-V bus in mixed 1.2-V, 1.5-V, 1.8-V or 2.5-V/1.8-V, 2.5-V or 3.3-V supply systems.

All inputs are equipped with protection circuits against static discharge.



S-WFBGA6-0102-0.40A01

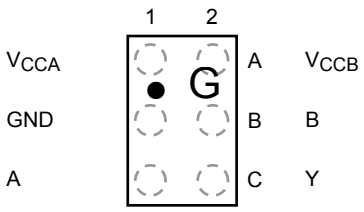
Weight: 1 mg (typ.)

Features

- Level converter for interfacing 1.2-V to 1.8-V, 1.2-V to 2.5-V, 1.2-V to 3.3-V, 1.5-V to 2.5-V, 1.5-V to 3.3-V, 1.8-V to 2.5-V, 1.8-V to 3.3-V or 2.5 V to 3.3-V system.
- High-speed operation : t_{pd} = 6.8 ns (max) (V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 7.8 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 9.0 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 31 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
  t_{pd} = 9.5 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)
  t_{pd} = 10.5 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V)
  t_{pd} = 32 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V)
  t_{pd} = 37 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V)
- Output current : I_{OH}/I_{OL} = ±12 mA (min) (V_{CCB} = 3.0 V)
  I_{OH}/I_{OL} = ±9mA (min) (V_{CCB} = 2.3 V)
  I_{OH}/I_{OL} = ±3 mA (min) (V_{CCB} = 1.65 V)
- Latch-up performance: −300 mA
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Ultra-small package: WCSP6
- Power-down protection is provided on all inputs and outputs

Start of commercial production
2009-04

Pin Assignment (top view)



Truth Table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Block Diagram

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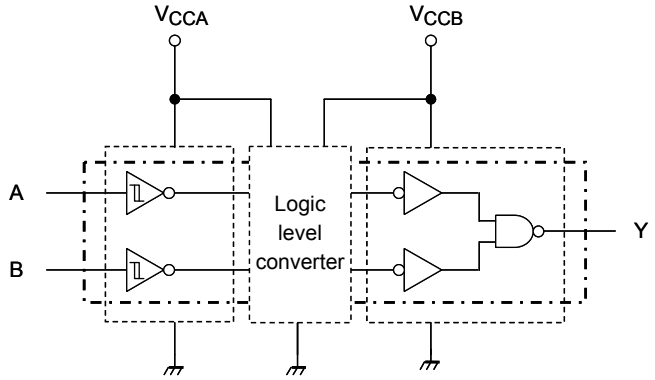


Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCA}	−0.5 to 4.6	V
	V_{CCB}	−0.5 to 4.6	
DC input voltage (A, B)	V_{IN}	−0.5 to 4.6	V
DC output voltage (Y)	V_{OUTB}	−0.5 to 4.6 (Note 3)	V
		−0.5 to V_{CCB} + 0.5 (Note 4)	
Input diode current	I_{IK}	−25	mA
Output diode current	I_{OK}	±50 (Note 5)	mA
DC output current	I_{OUTB}	±25	mA
DC V_{CC} / ground current per supply pin	I_{CCA}	±25	mA
	I_{CCB}	±50	
Power dissipation	P_D	100	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Don’t supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.

Note 3: Output in OFF state

Note 4: High or Low state. I_{OUT} absolute maximum rating must be observed.

Note 5: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 6)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CCA}	1.1 to 2.7	V
	V_{CCB}	1.65 to 3.6	
Input voltage (A, B)	V_{IN}	0 to 3.6	V
Output voltage (Y)	V_{OUTB}	0 to 3.6 (Note 7)	V
		0 to V_{CCB} (Note 8)	
Output current (Y)	I_{OUTB}	±12 (Note 9)	mA
		±9 (Note 10)	
		±3 (Note 11)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 12)	ns/V

Note 6: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 7: Output in OFF state

Note 8: High or Low state

Note 9: V_{CCB} = 3.0 to 3.6 V

Note 10: V_{CCB} = 2.3 to 2.7 V

Note 11: V_{CCB} = 1.65 to 1.95 V

Note 12: V_{IN} = 0.8 to 2.0 V, V_{CCA} = 2.5 V, V_{CCB} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Ta = –40 to 85°C		Unit
							Min	Max	
Input voltage	H-level	V_P	—		1.2	1.65 to 3.6	—	1.10	V
					1.4	1.65 to 3.6	—	1.20	
					1.65	1.65 to 3.6	—	1.35	
					2.3	1.65 to 3.6	—	1.70	
					2.7	1.65 to 3.6	—	2.00	
	L-level	V_N	—		1.2	1.65 to 3.6	0.10	—	V
					1.4	1.65 to 3.6	0.20	—	
					1.65	1.65 to 3.6	0.30	—	
					2.3	1.65 to 3.6	0.50	—	
					2.7	1.65 to 3.6	0.70	—	
Hysteresis voltage		V_H	—		1.2	1.65 to 3.6	0.20	0.90	V
					1.4	1.65 to 3.6	0.20	0.90	
					1.65	1.65 to 3.6	0.20	0.95	
					2.3	1.65 to 3.6	0.30	1.00	
					2.7	1.65 to 3.6	0.30	1.20	
Output voltage	H-level	V_{OHB}	V_{IN} = V_{IH} or V_{IL}	I_{OHB} = –100 μA	1.1 to 2.7	1.65 to 3.6	V_{CCB} – 0.2	—	V
				I_{OHB} = –3 mA	1.1 to 2.7	1.65	1.25	—	
				I_{OHB} = –9 mA	1.1 to 2.7	2.3	1.7	—	
				I_{OHB} = –12 mA	1.1 to 2.7	3.0	2.2	—	
	L-level	V_{OLB}	V_{IN} = V_{IH} or V_{IL}	I_{OLB} = 100 μA	1.1 to 2.7	1.65 to 3.6	—	0.2	V
				I_{OLB} = 3 mA	1.1 to 2.7	1.65	—	0.3	
				I_{OLB} = 9 mA	1.1 to 2.7	2.3	—	0.6	
				I_{OLB} = 12 mA	1.1 to 2.7	3.0	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±1.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	2.0	μA
Quiescent supply current		I_{CCA}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	2.0	μA
		I_{CCB}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	2.0	
		I_{CCA}	V_{CCA} < V_{IN} ≤ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	
		I_{CCB}	V_{IN} = V_{CCA} V_{CCB} ≤ Y ≤ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	

AC Characteristics (Ta = −40 to 85°C, Input: $t_r = t_f = 2.0$ ns)

V_{CCA} = 2.5 ± 0.2 V, V_{CCB}= 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	6.8	ns

V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	7.8	ns

V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	9.0	ns

V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	31	ns

V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	9.5	ns

V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	10.5	ns

V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	32	ns

V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V

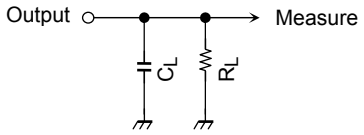
Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	37	ns

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Circuit	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Input capacitance	C_{IN}	A, B	2.5	3.3	5	pF
Power dissipation capacitance (Note)	C_{PDA}	f_{IN} = 10 MHz	2.5	3.3	5	pF
	C_{PDB}	f_{IN} = 10 MHz	2.5	3.3	10	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2$ (per bit)

AC Test Circuit



Symbol	V_{CC} (output)	
	3.3 ± 0.3 V 2.5 ± 0.2 V	1.8 ± 0.15 V
R_L	500 Ω	1 kΩ
C_L	30 pF	30 pF

Figure 1

AC Waveform

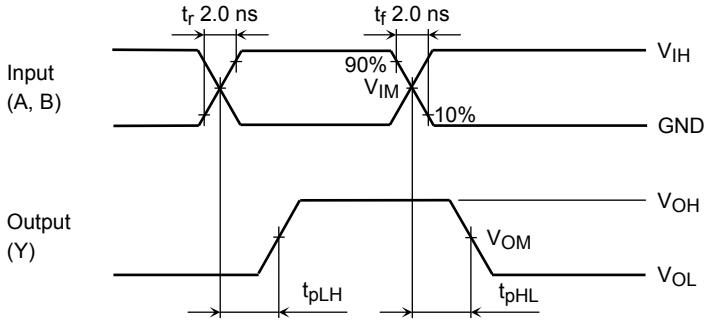
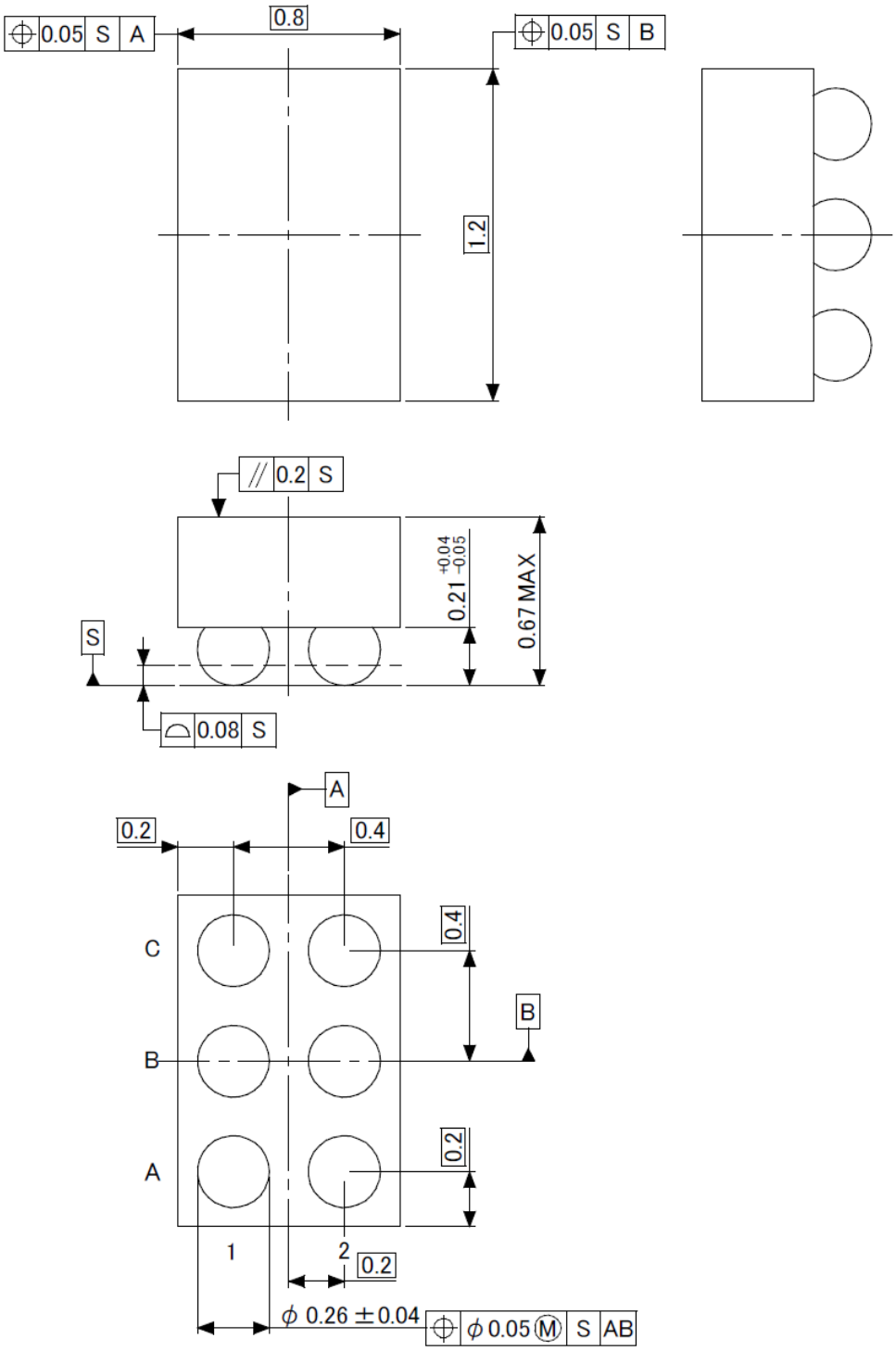


Figure 2 t_{pLH}, t_{pHL}

Package Dimensions

S-WFBGA6-0102-0.40A01 Unit: mm



Weight: 1 mg (typ.)

The resins used in this product include no flame retardants.

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