IS2062/64

Bluetooth® 4.2 Stereo Audio SoC

Features

- Qualified for Bluetooth v4.2 specifications
- Supports HFP 1.6, HSP 1.2, A2DP 1.3, SPP 1.2 and AVRCP 1.6
- Supports Bluetooth Low Energy (BLE) (FW dependent):
  - Generic access service
  - Device information service
  - Proprietary services for data communication
  - Apple Notification Center Service (ANCS)
- Supports high resolution up to 24-bit, 96 kHz audio data format
- I^2S digital audio (IS2064 only), MIC, analog audio, AUX-In
- Supports microphone inputs: 2 (IS2062) and 1 (IS2064)
- UART, GPIOs, and LEDs
- Supports firmware field upgrade
- Battery charging

Baseband Features

- 16 MHz main clock input
- Flash memory (8 Mbit)
- EEPROM (128 Kbit)
- Connects two hosts with HFP or A2DP profiles simultaneously, and SPP/BLE connection to one host
- Adaptive Frequency Hopping (AFH)

RF Features

- Class 2 output power (+2 dBm typical)
- Receive sensitivity: -90 dBm (2 Mbps EDR)
- Supports Bluetooth (BDR/EDR/BLE) specifications (FW dependent)
- Combined Tx/Rx RF terminal simplifies external matching and reduces external antenna switches
- Tx/Rx RF switch for Class 2 or Class 3 applications
- Integrated synthesizer requires no external voltage-controlled oscillator (VCO), varactor diode, resonator, loop filter
- Crystal oscillator with built-in digital trimming compensates for temperature or process variations

DSP Audio Processing

- 32-bit DSP core
- Supports 64 kbps A-Law, μ-Law PCM format, Continuous Variable Slope Delta (CVSD) Modulation for Synchronous Connection-Oriented (SCO) channel operation
- Supports 8/16 kHz noise suppression
- Supports 8/16 kHz echo cancellation
- Packet loss concealment (PLC)
- Supports Serial Copy Management System (SCMS-T) content protection

Audio Codec

- Sub-band Coding (SBC) and optional Advanced Audio Coding (AAC) decoding
- 20-bit digital-to-analog (DAC) with 98 dB SNR
- 16-bit analog-to-digital (ADC) with 92 dB SNR
- Supports up to 24-bit, 96 kHz on I^2S digital audio

Peripherals

- High-speed Host Controller Interface (HCI)-UART (supports up to 921,600 bps)
- USB2.0 compatible interface for FW/EEPROM upgrade (IS2064)
- Built-in lithium-ion and lithium-polymer battery charger (up to 350 mA)
- Integrated 1.8V and 3V configurable switching regulator and low-dropout (LDO) regulator
- Built-in ADC for battery monitoring and voltage sensor and charger thermal protection
- Built-in undervoltage protection (UVP)
- LED drivers: 2 (IS2062) and 3 (IS2064)

Operating Condition

- Operating voltage: 3.2V to 4.2V
- Temperature range: -20°C to +70°C

Package

- IS2062: 7 mm x 7 mm, LGA-56 package
- IS2064: 8 mm x 8 mm, LGA-68 package
- 0.4 mm pitch

Applications

- Soundbars and subwoofers
- Speaker phones
- Headsets and headphones

Description

The IS2062/64 is a Stereo Audio SoC qualified for Bluetooth 4.2 with Enhanced Data Rate (EDR). It integrates a 32-bit DSP co-processor and a codec which is dedicated for voice and audio applications. For voice applications, Continuously Variable Slope Delta (CVSD) encoding/decoding, 8K/16K noise reduction, and echo cancellation are implemented. For audio applications, Sub-band coding (SBC) and AAC Low-Complexity (AAC-LC) decoding functions are used.

The IS2062/64 SoC features a 20-bit audio DAC in addition to an I^2S digital audio interface that supports up to 24-bit, 96 kHz data formats. System optimizations include an integrated battery voltage sensor, battery charger, switching regulator, and LDO.

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NOTES:

1.0 DEVICE OVERVIEW

The IS2062/64 SoC integrates a Bluetooth 4.2 dual-mode radio transceiver, a Power Management Unit (PMU), a Microcontroller (MCU), an audio codec, a crystal and a 32-bit DSP. The IS2062/64 SoC can be configured using a UI tool.

Note:	The UI tool is a Windows®-based configuration utility tool, which is available for download from the Microchip web site at: www.microchip.com/IS2062 and www.microchip.com/IS2064.

Figure 1-1 illustrates a typical block diagram of the IS2062/64 SoC.

FIGURE 1-1: IS2062/64 STEREO AUDIO SOC BLOCK DIAGRAM

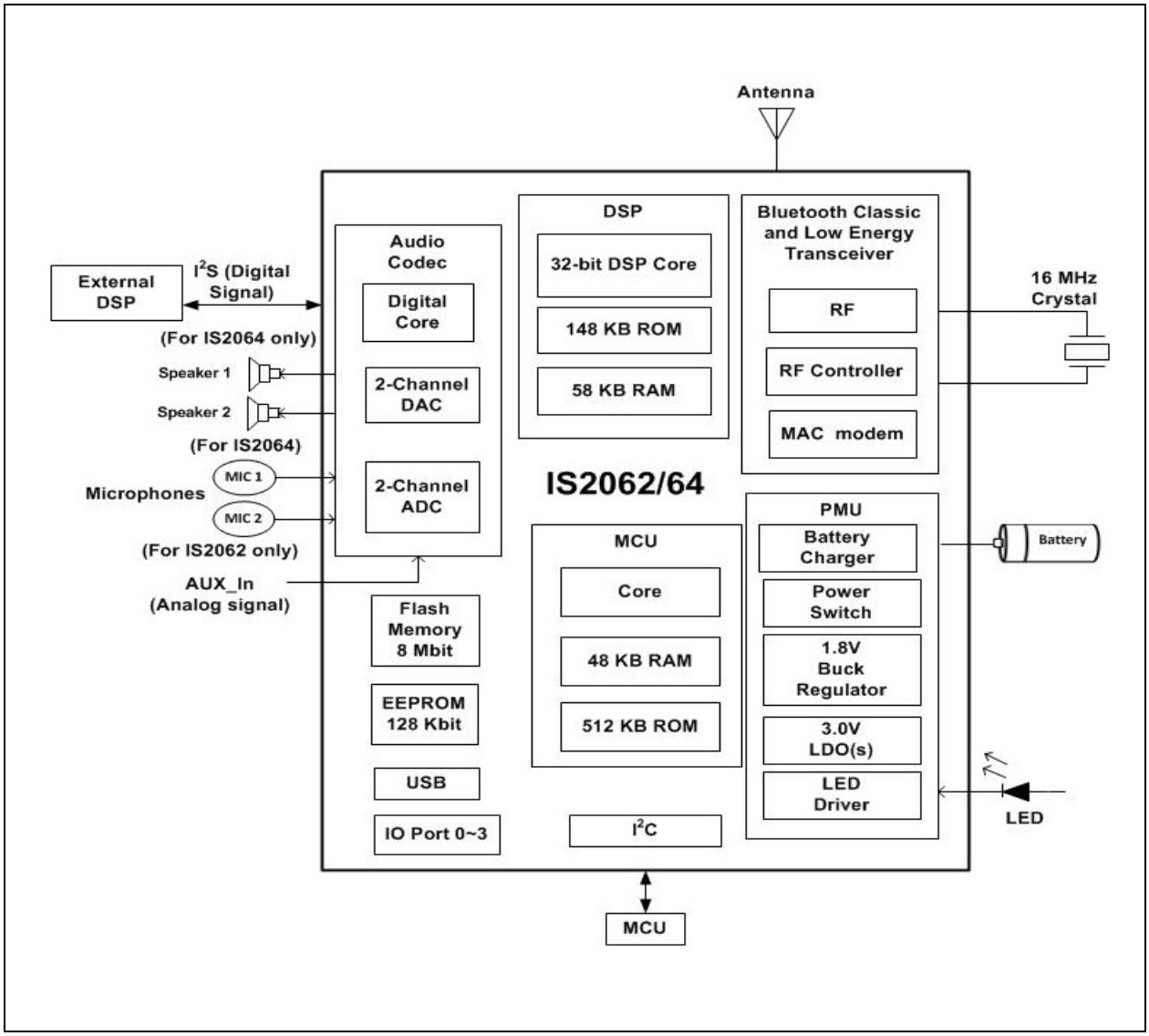


Table 1-2 provides the key features of the IS2062/64 SoC.

TABLE 1-1: IS2062/64 KEY FEATURES

Feature	IS2062	IS2064
Application	Headset/Speaker	Speaker
Stereo/mono	Stereo	Stereo
Pin count	56	68
Dimensions (mm^2)	7 x 7	8 x 8
Audio DAC output	2 Channel	2 Channel
DAC (single-ended) SNR at 2.8V (dB)	-98	-98
DAC (capless) SNR at 2.8V (dB)	-96	-96
ADC SNR at 2.8V (dB)	-92	-92
I^2S digital interface	No	Yes
Analog AUX-In	Yes	Yes
Mono microphones	2	1
External audio amplifier interface	Yes	Yes
UART	Yes	Yes
LED driver	2	3
Internal DC-DC step-down regulator	Yes	Yes
DC 5V adaptor input	Yes	Yes
Battery charger (350 mA max)	Yes	Yes
ADC for thermal charger protection	Yes	Yes
Undervoltage protection	Yes	Yes
GPIO	10	15
Button support	6	6
NFC (triggered by external NFC)	Yes	Yes
EEPROM	128 K	128 K
Customized voice prompt	Store in EEPROM	
Multi-tone	Yes	Yes
DSP sound effect	Yes	Yes
BLE	Yes	Yes
Bluetooth profiles		
HFP	1.6	1.6
AVRCP	1.6	1.6
A2DP	1.3	1.3
HSP	1.2	1.2
SPP	1.2	1.2

Figure 1-2 illustrates the IS2062 SoC pin diagram. Table 1-2 provides the pin descriptions of the IS2062 SoC and these pins can be configured using the UI tool.

FIGURE 1-2: IS2062 SOC PIN DIAGRAM

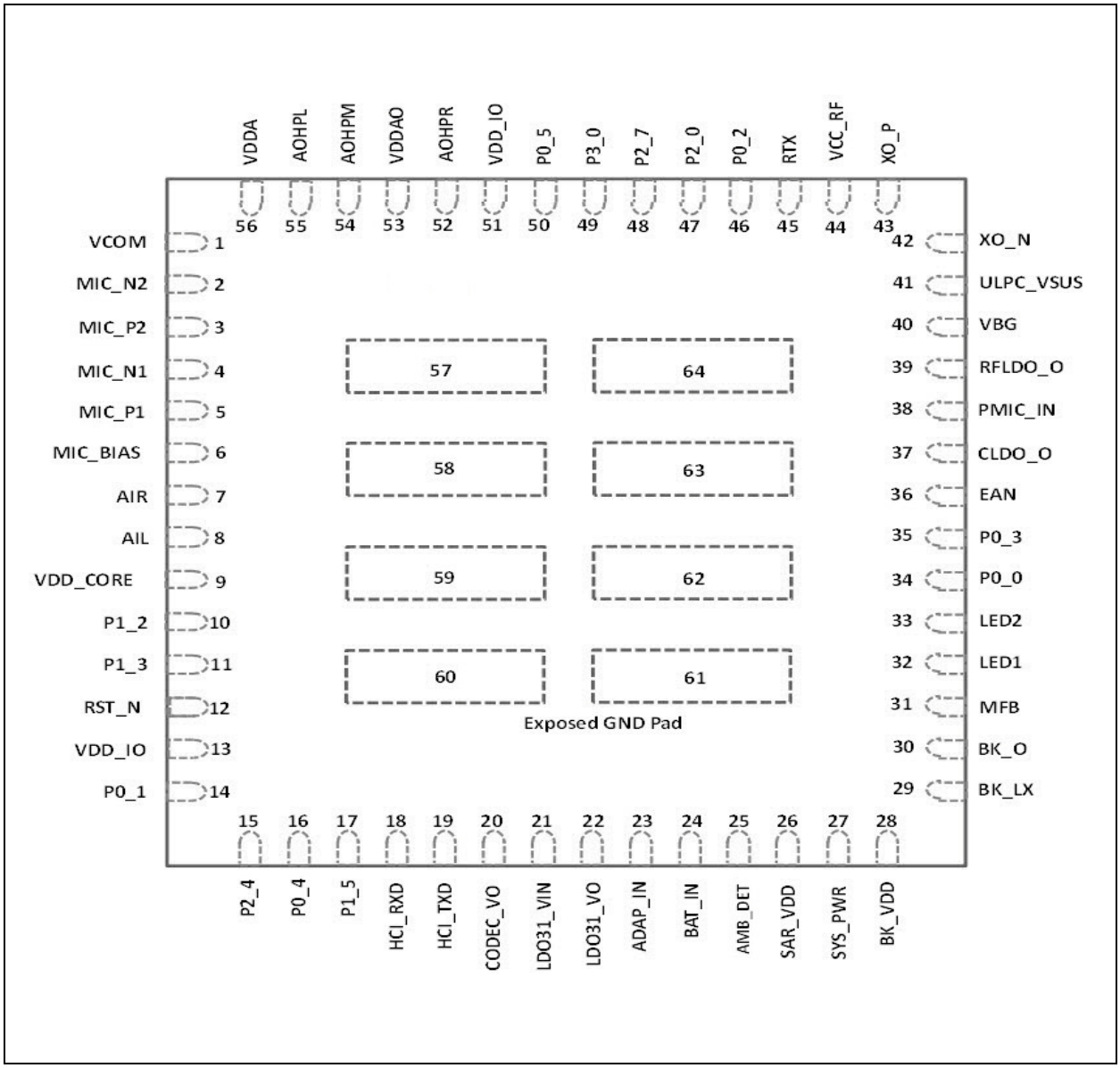


TABLE 1-2: IS2062 SOC PIN DESCRIPTIONS

Pin No	Pin Type	Name	Description
1	P	VCOM	Internal biasing voltage for codec; connect to GND through a 1 µF (X5R/X7R) capacitor
2	I	MIC_N2	Mic 2 mono differential analog negative input
3	I	MIC_P2	Mic 2 mono differential analog positive input
4	I	MIC_N1	Mic 1 mono differential analog negative input
5	I	MIC_P1	Mic 1 mono differential analog positive input
6	P	MIC_BIAS	Electric mic biasing voltage
7	I	AIR	R-channel, single-ended analog input
8	I	AIL	L-channel, single-ended analog input
9	P	VDD_CORE	Core 1.2V power input; connect to the CLDO_O pin; connect to GND through a 1 µF (X5R/X7R) capacitor
10	O	P1_2	I^2C SCL (EEPROM)
11	I/O	P1_3	I^2C SDA (EEPROM), requires external pull-up resistor
12	I	RST_N	System Reset (active-low)
13	P	VDD_IO	I/O power supply input (3.0V~3.6V); connect to LDO31_VO (pin # 22); connect to GND through a 1 µF (X5R/X7R) capacitor
14	I/O	P0_1	Configurable control or indication pin (Internally pulled up if configured as an input) • FWD key when class 2 RF (default), active-low • Class1 Tx control signal for external RF T/R switch, active-high
15	I	P2_4	System configuration pin along with P2_0 and EAN pins can be used to set the SoC in any one of the following modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
16	I/O	P0_4	Configurable control or indication pin (Internally pulled up if configured as an input) • NFC detection pin, active-low • Out_Ind_1
17	I/O	P1_5	Configurable control or indication pin (Internally pulled up if configured as an input) • NFC detection pin, active-low • Out_Ind_1 • Slide Switch Detector
18	I	HCI_RXD	HCI UART data input
19	O	HCI_TXD	HCI UART data output
20	P	CODEC_VO	LDO output for codec power
21	P	LDO31_VIN	LDO input, connect to SYS_PWR (pin # 27)
22	P	LDO31_VO	3V LDO output for VDD_IO power, do not calibrate
23	P	ADAP_IN	5V power adaptor input
24	P	BAT_IN	Battery input. voltage range: 3.2V to 4.2V

TABLE 1-2: IS2062 SOC PIN DESCRIPTIONS (CONTINUED)

Pin No	Pin Type	Name	Description
25	I	AMB_DET	Analog input for ambient temperature detection
26	P	SAR_VDD	SAR 1.8V input; connect to BK_O pin
27	P	SYS_PWR	Power output from BAT_IN or ADAP_IN for IS2062 only
28	P	BK_VDD	1.8V buck VDD power Input; connect to SYS_PWR pin
29	P	BK_LX	1.8V buck PWM/PFM output
30	P	BK_O	1.8V buck feedback input
31	I	MFB	• Multi-function button and power-on key • UART RX IND, active-high
32	I	LED1	LED driver 1
33	I	LED2	LED driver 2
34	I/O	P0_0	Configurable control or indication pin (Internally pulled up if configured as an input) • Slide Switch Detector, active-low • UART TX_IND, active-low
35	I/O	P0_3	Configurable control or indication pin (Internally pulled up if configured as an input) • REV key (default), active-low • Buzzer signal output • Out_Ind_2 • Class1 Rx Control signal of external RF T/R switch, active-high
36	I	EAN	System configuration pin along with the P2_4 and P2_0 pins can be used to set the SoC in any one of the following modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
37	P	CLDO_O	1.2V core LDO output
38	P	PMIC_IN	1.8V power input for internal blocks; connect to BK_O (pin # 30)
39	P	RFLDO_O	1.28V RF LDO output
40	P	VBG	Bandgap output reference for decoupling interference
41	P	ULPC_VSUS	ULPC 1.2V output power
42	I	XO_N	16 MHz crystal input negative
43	I	XO_P	16 MHz crystal input positive
44	P	VCC_RF	RF power input (1.28V) for both synthesizer and Tx/Rx block
45	I/O	RTX	RF path (transmit/receive)
46	I	P0_2	Configurable control or indication pin (Internally pulled up if configured as an input) Play/Pause key (default), active-low

TABLE 1-2: IS2062 SOC PIN DESCRIPTIONS (CONTINUED)

Pin No	Pin Type	Name	Description
47	I	P2_0	System configuration pin along with P2_4 and EAN pins can be used to set the SoC in any one of the following modes: • Application mode (for normal operation), • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
48	I	P2_7	Configurable control or indication pin (Internally pulled up if configured as an input) Volume-up key (default)
49	I	P3_0	Configurable control or indication pin (Internally pulled up if configured as an input) AUX-In detector
50	I	P0_5	Configurable control or indication pin (Internally pulled up if configured as an input) Volume-up key (default)
51	P	VDD_IO	I/O power supply input (3.0V~3.6V); Connect to LDO31_VO pin
52	O	AOHPR	R-channel analog headphone output,
53	P	VDDAO	Power supply dedicated to codec output amplifiers; connect to CODEC_VO pin
54	O	AOHPM	Headphone common mode output/sense input
55	O	AOHPL	L-channel analog headphone output
56	P	VDDA	Power supply or reference voltage for external codec; connect to CODEC_VO pin
57-64	P	EP	Exposed pads. Used as ground (GND) pins

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin

Note: The IS2062 SoC pins can be configured using the UI tool.

Figure 1-3 illustrates the pin diagram of the IS2064 SoC.

FIGURE 1-3: IS2064 SOC PIN DIAGRAM

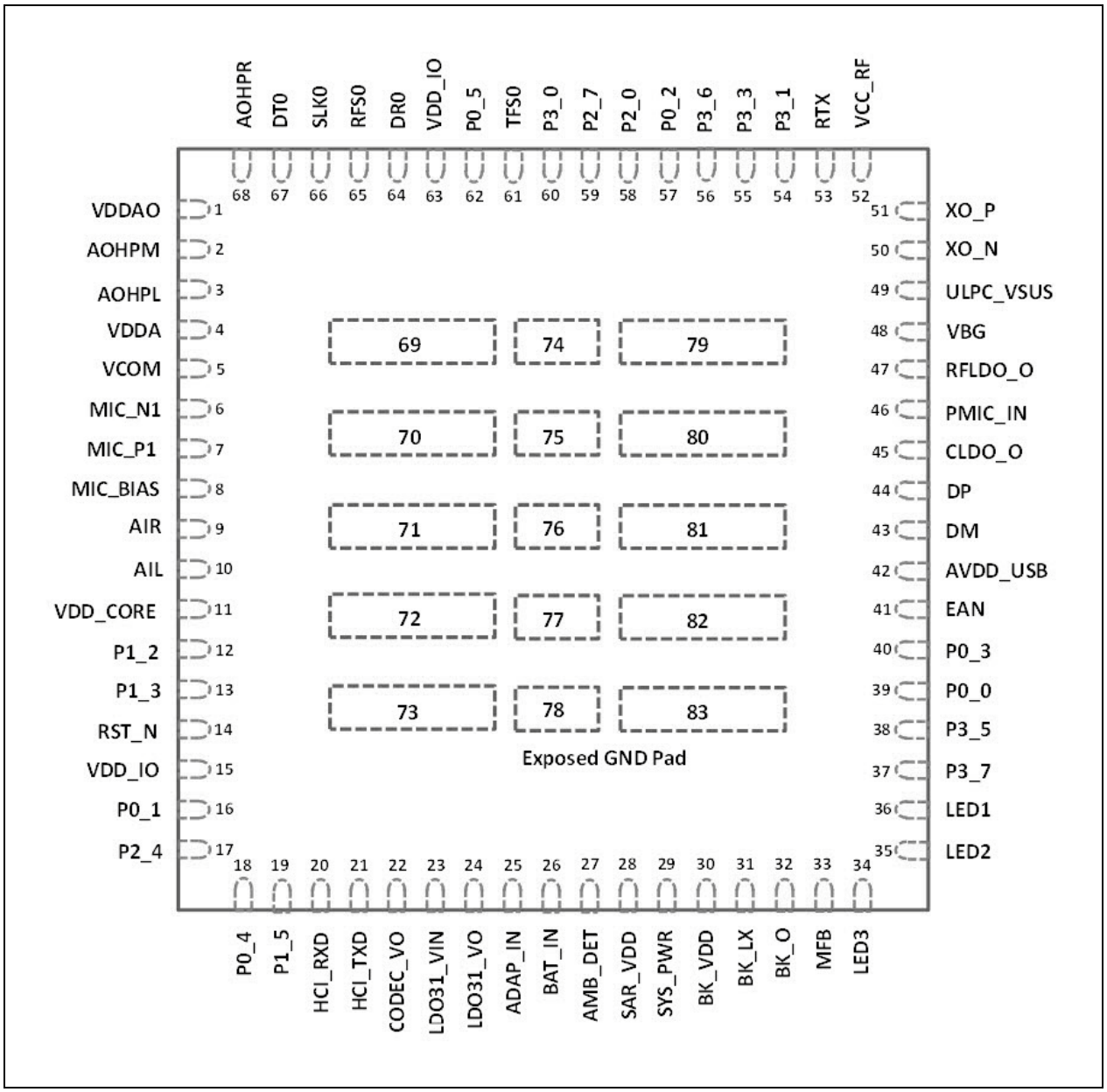


Table 1-3 provides the pin descriptions of the IS2064 SoC.

TABLE 1-3: IS2064 SOC PIN DESCRIPTIONS

Pin No	Pin Type	Name	Description
1	P	VDDAO	Power supply dedicated to codec output amplifiers; connect to the CODEC_VO pin
2	O	AOHPM	Headphone common mode output or sense input
3	O	AOHPL	Headphone output, left channel
4	P	VDDA	Power supply or reference voltage for external codec; connect to the CODEC_VO pin
5	P	VCOM	Internal biasing voltage for codec
6	I	MIC_N1	Mic 1 mono differential analog negative input
7	I	MIC_P1	Mic 1 mono differential analog positive input
8	P	MIC_BIAS	Electric microphone biasing voltage
9	I	AIR	R-channel single-ended analog input
10	I	AIL	L-channel single-ended analog input
11	P	VDD_CORE	Core 1.2V power input; connect to the CLDO_O pin
12	O	P1_2	I^2C SCL (EEPROM)
13	I/O	P1_3	I^2C SDA (EEPROM), requires external pull-up resistor
14	I	RST_N	System Reset (active-low)
15	P	VDD_IO	I/O power supply input (3.0V~3.6V); connect to LDO31_VO (pin # 24); connect to GND through a 1 µF (X5R/X7R) capacitor
16	I/O	P0_1	Configurable control or indication pin (Internally pulled up if configured as an input) • FWD key when Class 2 RF (default), active-low • Class1 Tx control signal for external RF Tx/Rx switch, active-high
17	I	P2_4	System configuration pin along with the P2_0 and EAN pins, used to set the SoC in any one of the following modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
18	I/O	P0_4	Configurable control or indication pin (Internally pulled up if configured as an input) • NFC detection pin, active-low • Out_Ind_1
19	I/O	P1_5	Configurable control or indication pin (Internally pulled up if configured as an input) • NFC detection pin • Slide switch detector, active-high • Out_Ind_1 • Multi-speaker Master/Slave mode control (FW dependent)
20	I	HCI_RXD	HCI UART data input
21	O	HCI_TXD	HCI UART data output
22	P	CODEC_VO	LDO output for codec power
23	P	LDO31_VIN	LDO input; connect to SYS_PWR (pin # 29)

TABLE 1-3: IS2064 SOC PIN DESCRIPTIONS (CONTINUED)

Pin No	Pin Type	Name	Description
24	P	LDO31_VO	3V LDO output, for VDD_IO power, do not calibrate
25	P	ADAP_IN	5V power adaptor input
26	P	BAT_IN	Battery input. Voltage range: 3.2V to 4.2V
27	I	AMB_DET	Analog input for ambient temperature detection
28	P	SAR_VDD	SAR 1.8V input; connect to BK_O pin
29	P	SYS_PWR	Power output which come from BAT_IN or ADAP_IN
30	P	BK_VDD	1.8V buck VDD Power Input; connect to SYS_PWR pin
31	P	BK_LX	1.8V buck PWM/PFM output
32	P	BK_O	1.8V buck feedback input
33	I	MFB	1. Multi-function button and power-on key 2. UART RX_IND, active-high
34	I	LED3	LED driver 3
35	I	LED2	LED driver 2
36	I	LED1	LED driver 1
37	I/O	P3_7	Configurable control or indication pin (Internally pulled up if configured as an input) UART TX_IND, active-low
38	I/O	P3_5	Configurable control or indication pin (Internally pulled up if configured as an input)
39	I/O	P0_0	Configurable control or indication pin (Internally pulled up if configured as an input) Slide switch detector, active-high
40	I/O	P0_3	Configurable control or indication pin (Internally pulled up if configured as an input) • REV key, active-low. • Buzzer signal output • Out_Ind_2 • Class 1 Rx Control signal of external RF T/R switch, active-high
41	I	EAN	System configuration pin along with the P2_0 and P2_4 pins, used to set the IS2062/64 SoC in any one of the following modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
42	P	AVDD_USB	USB power input; connect to LDO31_VO pin
43	I/O	DM	Differential data-minus USB
44	I/O	DP	Differential data-positive USB
45	P	CLDO_O	1.2V core LDO output
46	P	PMIC_IN	1.8V power input for internal blocks; connect to BK_O (pin # 32)
47	P	RFLDO_O	1.28V RF LDO output
48	P	VBG	Bandgap output reference for decoupling interference
49	P	ULPC_VSUS	ULPC 1.2V output power, maximum loading 1 mA
50	I	XO_N	16 MHz crystal input negative
51	I	XO_P	16 MHz crystal input positive

TABLE 1-3: IS2064 SOC PIN DESCRIPTIONS (CONTINUED)

Pin No	Pin Type	Name	Description
52	P	VCC_RF	RF power input for both synthesizer and Tx/Rx block
53	I/O	RTX	RF path (transmit/receive)
54	I/O	P3_1	Configurable control or indication pin (Internally pulled up if configured as an input) REV key when Class 1 RF (default), active-low
55	I/O	P3_3	Configurable control or indication pin (Internally pulled up if configured as an input) FWD key when class 1 RF (default), active-low
56	I/O	P3_6	Configurable control or indication pin (Internally pulled up if configured as an input) Multi-SPK Master/Slave mode control (FW dependent)
57	I/O	P0_2	Configurable control or indication pin (Internally pulled up if configured as an input) Play/Pause key as the default setting
58	I/O	P2_0	System configuration pin along with the EAN and P2_4 pins can be used to set the SoC in any one of the following modes: • Application mode (for normal operation), • Test mode (to change EEPROM values), and • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
59	I/O	P2_7	Configurable control or indication pin (Internally pulled up if configured as an input) Volume-up key (default)
60	I/O	P3_0	Configurable control or indication pin (Internally pulled up if configured as an input) AUX-In detector
61	I/O	TFS0	I^2S interface: left/right clock
62	I/O	P0_5	Configurable control or indication pin (Internally pulled up if configured as an input) Volume down key (default)
63	P	VDD_IO	I/O power supply input (3.0V~3.6V); connect to LDO31_VO pin
64	I/O	DR0	I^2S interface: digital left/right data
65	I/O	RFS0	I^2S interface: left/right clock
66	I/O	SCLK0	I^2S interface: bit clock
67	I/O	DT0	I^2S interface: digital left/right data
68	O	AOHPR	Headphone output, right channel
69-83	P	EP	Exposed pads, Used as ground (GND) pins

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin

Note: These pins can be configured using the UI tool.

2.0 AUDIO

The input and output audios have different stages and each stage can be programmed to vary the gain response characteristics. For microphone, both single-end inputs and differential inputs are supported. To maintain a high quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors can be used at both positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

2.1 Digital Signal Processor

A Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction are in-built. To reduce nonlinear distortion and help echo cancellation, an outgoing signal level to the speaker will exceed the threshold (and therefore likely to create echo). This may result in suppression of the signal. Adaptive filtering is also applied to track the echo path impulse in response to provide echo free and full-duplex user experience. The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by microphones and improves mutual understanding in communication. Advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are in-built. The audio effect algorithms are to improve the user's audio listening experience in terms of better quality audio after audio signal processing.

Figure 2-1 and Figure 2-2 illustrate the processing flow of speaker phone applications for speech and audio signal processing.

FIGURE 2-1: SPEECH PROCESSING

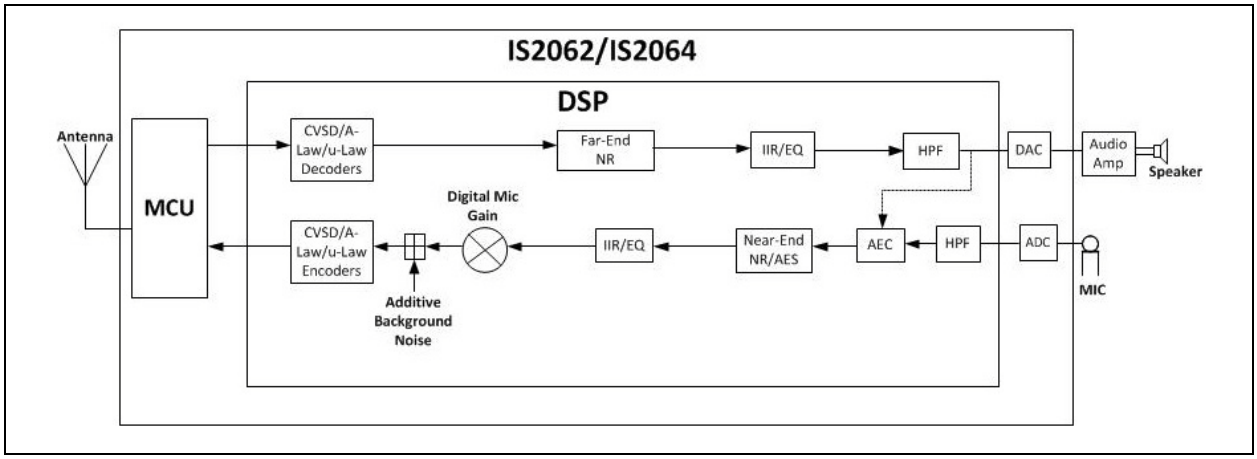
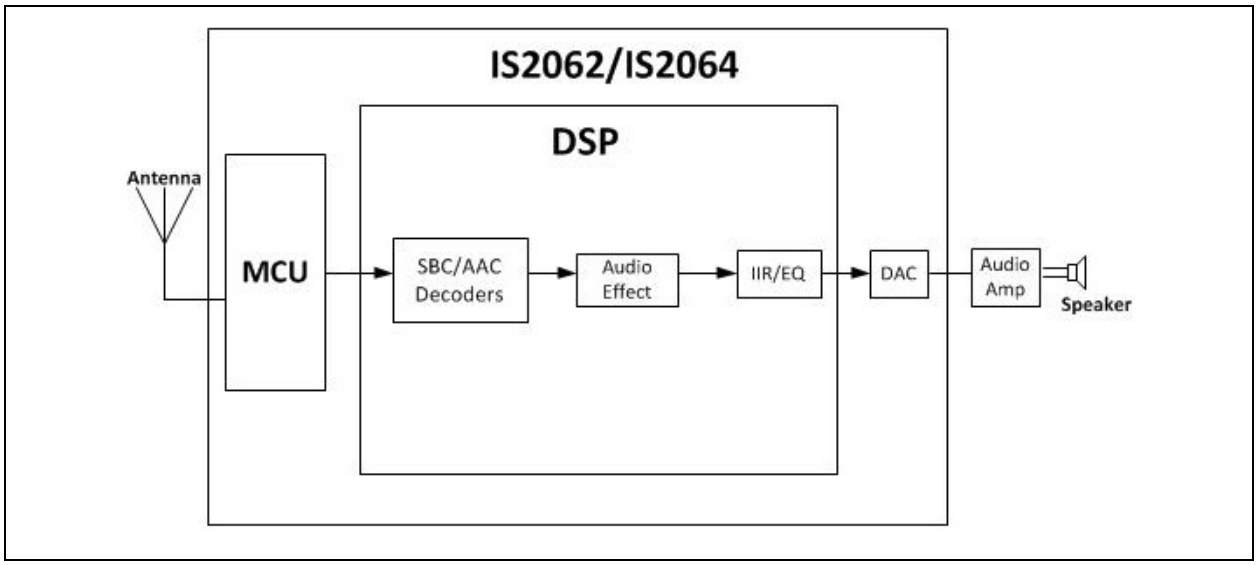


FIGURE 2-2: AUDIO PROCESSING



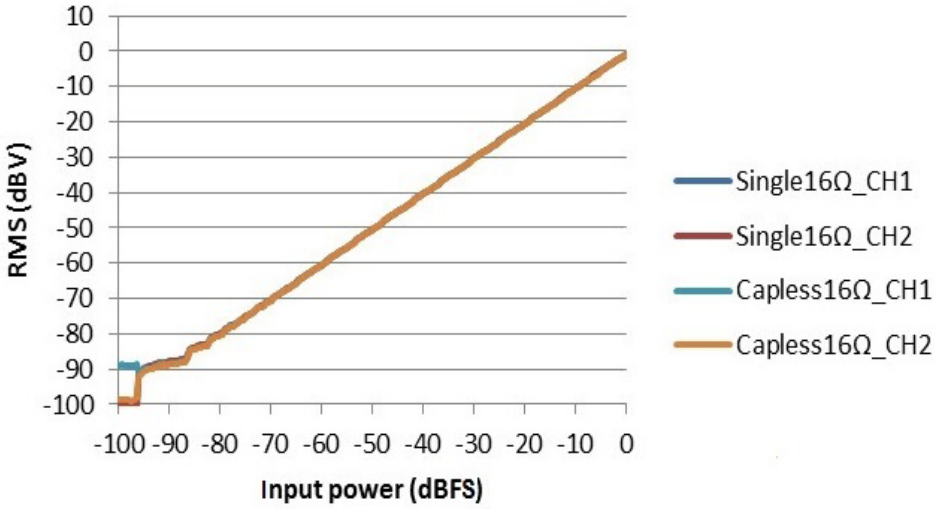
The DSP parameters can be configured using the DSP tool. For additional information on the DSP tool, refer to the *"IS206X DSP Application Note"*.

Note:	The DSP tool and IS206X DSP Application Note are available for download from the Microchip web site at: www.microchip.com/IS2062 and www.microchip.com/IS2064.

2.2 Codec

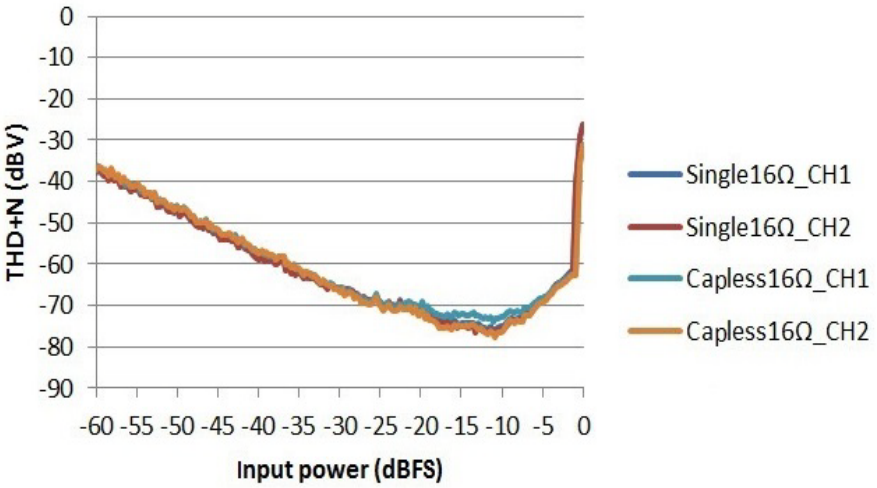
The built-in codec has a high signal-to-noise ratio (SNR) performance and it consist of an analog-to-digital converter (ADC), a digital-to-analog converter (DAC) and additional analog circuitry. Figure 2-3 through Figure 2-6 illustrate dynamic range and frequency response of the codec.

FIGURE 2-3: CODEC DAC DYNAMIC RANGE



Note: The data corresponds to 16 Ohm load with 2.8V operating voltage and 25ºC operating temperature.

FIGURE 2-4: CODEC DAC THD+N VERSUS INPUT POWER



Note: The data corresponds to 16 Ohm load with 2.8V operating voltage and 25ºC operating temperature.

FIGURE 2-5: CODEC DAC FREQUENCY RESPONSE (CAPLESS MODE)

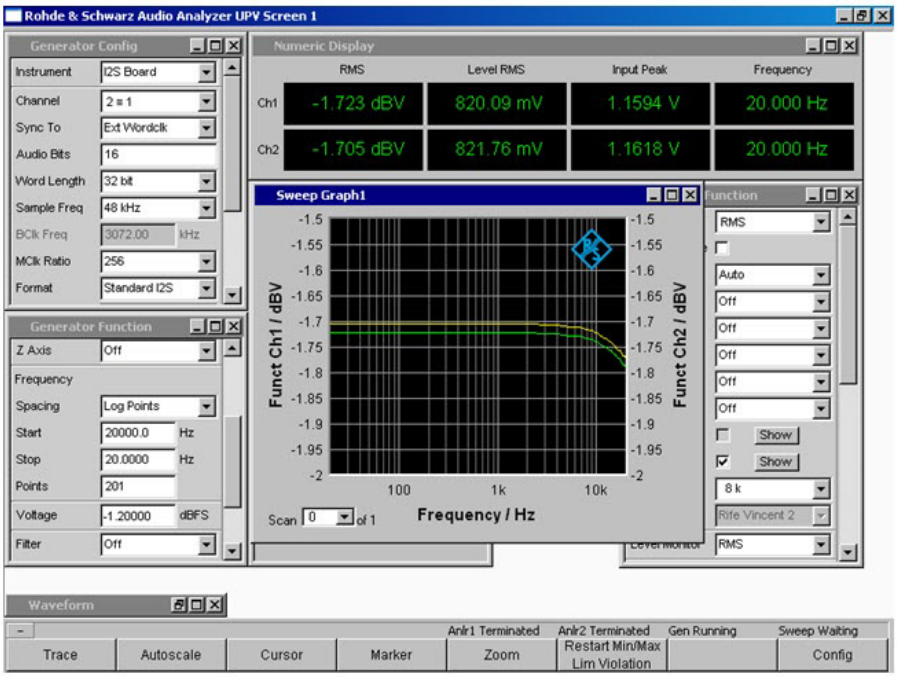
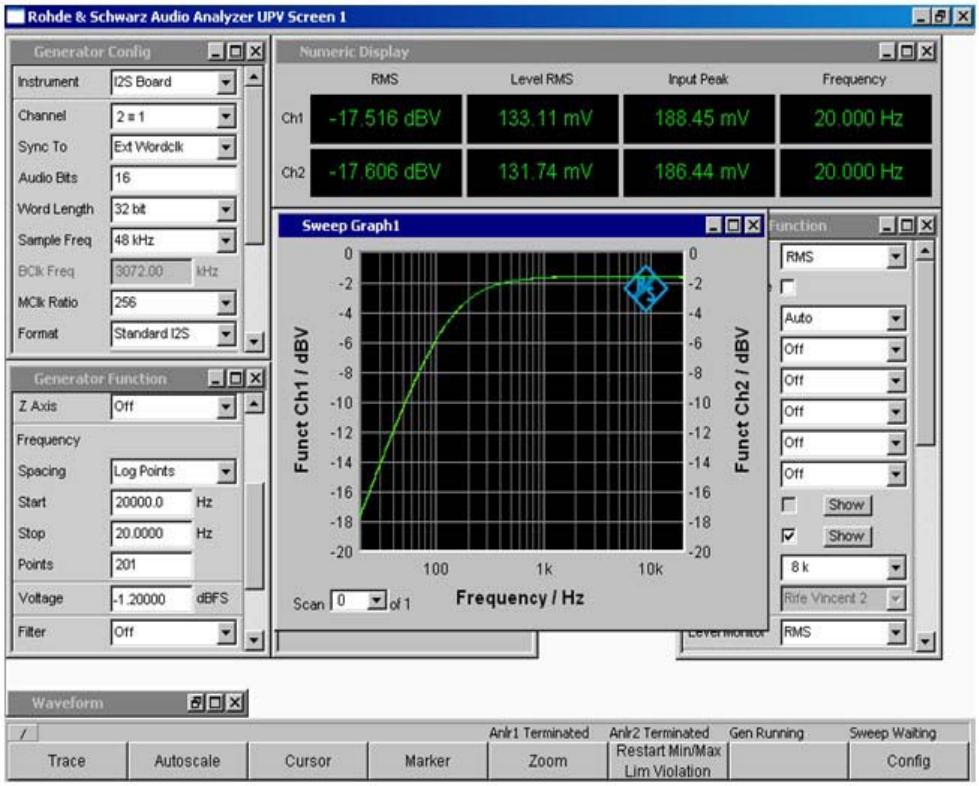


FIGURE 2-6: CODEC DAC FREQUENCY RESPONSE (SINGLE-ENDED MODE)



Note: The frequency response corresponds to single-ended mode with a 47 µF DC block capacitor.

2.3 Auxiliary Port

The IS2062/64 SoC supports one analog (line-in) signal from external audio source. The analog (line-in) signal can be processed by the DSP to generate different sound effects, multi-band dynamic range compression and audio widening, which can be setup by using the DSP tool.

2.4 Analog Speaker Output

The IS2062/64 SoC supports the following speaker output modes:

- Capless mode — Recommended for headphone applications in which capless output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. Figure 2-7 illustrates the analog speaker output Capless mode.
- Single-ended mode — Used for driving an external audio amplifier where a DC blocking capacitor is required. Figure 2-8 illustrates the analog speaker output Single-Ended mode.

FIGURE 2-7: ANALOG SPEAKER OUTPUT CAPLESS MODE

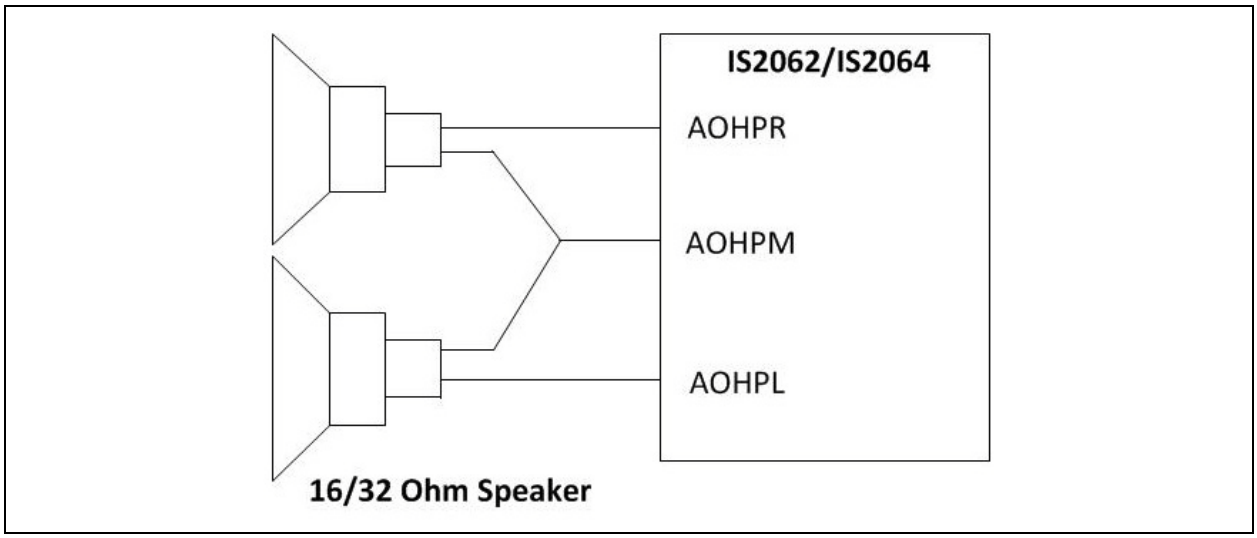
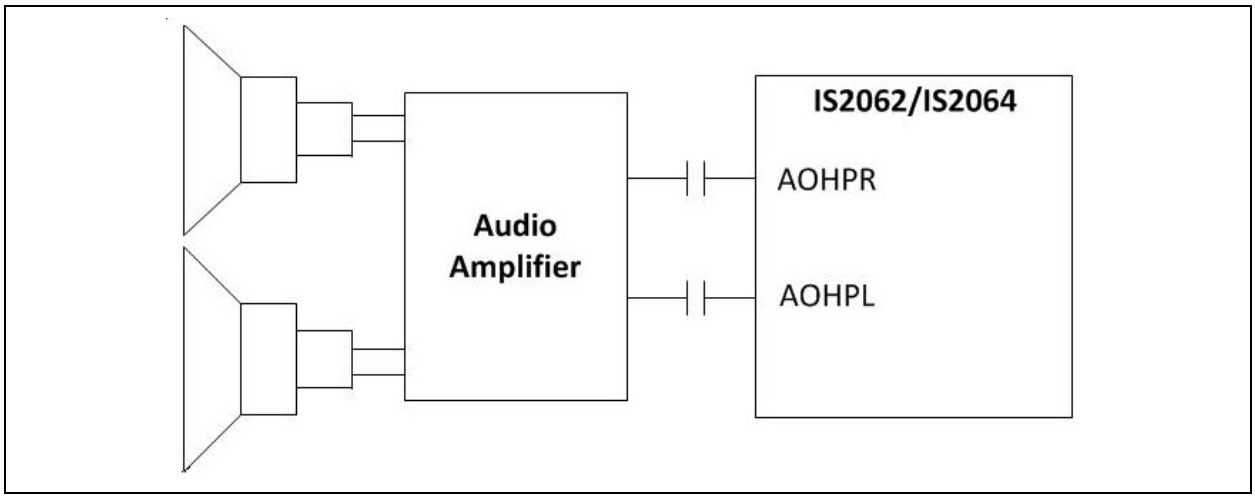


FIGURE 2-8: ANALOG SPEAKER OUTPUT SINGLE-ENDED MODE



3.0 TRANSCEIVER

The IS2062/64 SoC is designed and optimized for Bluetooth 2.4 GHz systems. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock to synchronize with another device.

3.1 Transmitter

The internal power amplifier (PA) has a maximum output power of +4 dBm. This is applied for Class 2 or Class 3 radios without an external RF PA.

The transmitter directly performs IQ conversion to minimize the frequency drift.

3.2 Receiver

The low-noise amplifier (LNA) operates with TR-combined mode for single port application. It can save a pin on package without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into digital signal for de-modulator analysis. A channel filter has been integrated into receiver channel before the ADC, which is used to reduce the external component count and increase the anti-interference capability. The image rejection filter is used to reject image frequency for low-IF architecture. This filter for low-IF architecture is intended to reduce external Band Pass Filter (BPF) component for super heterodyne architecture.

Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

3.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside, with a tunable internal LC tank that can reduce variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for synthesizer.

3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with Enhanced Data Rate (EDR) specification.

For Bluetooth 2.0 and above specifications, EDR has been introduced to provide data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packets represents 2-bit or 3-bit. This is achieved by using two different modulations, $\pi/4$ DQPSK and 8 DPSK.

3.5 Adaptive Frequency Hopping (AFH)

The IS2062/64 SoC has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose the clear channel for transceiver Bluetooth signal.

NOTES:

4.0 MICROCONTROLLER

A microcontroller is built into an SoC to execute the Bluetooth protocols. It operates from 16 MHz to higher frequencies where the firmware can dynamically adjust the trade-off between the computing power and the power consumption. In ROM version, the MCU firmware is hard-wired to minimize power consumption and to save the external Flash cost.

4.1 Memory

There are sufficient ROM and RAM to fulfill the requirement of processor, in which a synchronous single port RAM interface is used. The register bank, dedicated single port memory and Flash memory are connected to the processor bus. The processor coordinates all the link control procedures and data movement using a set of pointer registers.

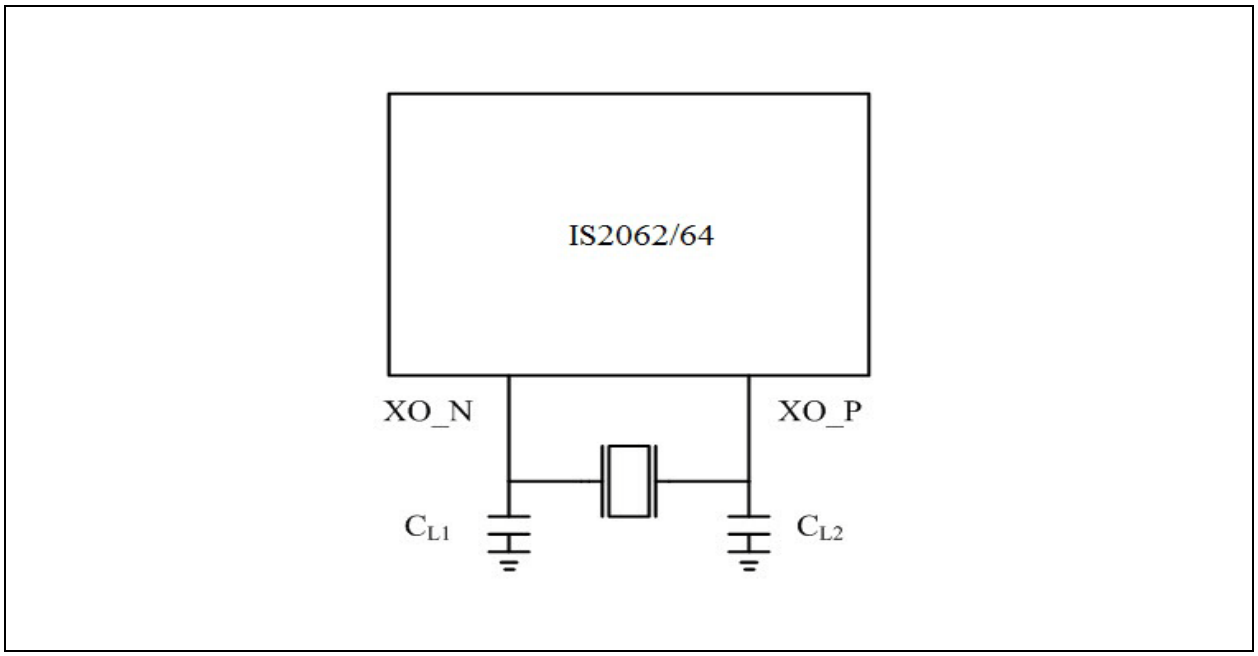
4.2 External Reset

The IS2062/64 SoC provides a watchdog timer (WDT) to Reset the SoC. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action can also be driven by an external Reset signal which is used to control the device externally by forcing it into a POR state. The RST_N signal input is active-low and no connection is required in most of the applications.

4.3 Reference Clock

The IS2062/64 SoC is composed of an integrated crystal oscillation function that uses a 16 MHz, ±10 ppm external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent loading capacitance in mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors (C_{trim}).
The value of trimming capacitance is 200 fF ($200x10^{-15}$ F) per LSb at 5-bit word and the overall adjustable clock frequency is ±50 kHz (based on crystal with load capacitance, C_L spec = 9 pF). Figure 4-1 illustrates the crystal connection of the IS2062/64 SoC with two capacitors.

FIGURE 4-1: CRYSTAL CONNECTION



NOTES:

5.0 POWER MANAGEMENT UNIT

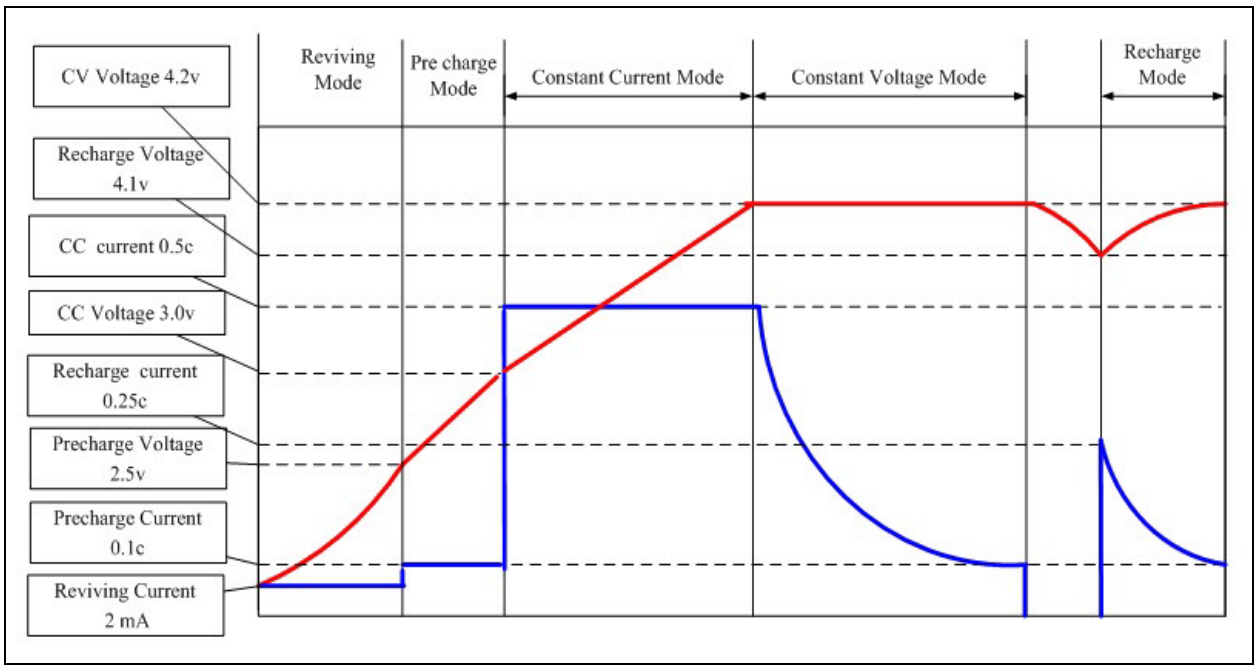
The IS2062/64 SoC has an integrated Power Management Unit (PMU). The main features of the PMU are a lithium-ion and lithium-polymer battery charger and voltage regulation. A power switch is used to switch over the power source between a battery and an adaptor. The PMU also provides current for driving LEDs.

5.1 Charging a Battery

The IS2062/64 SoC has a built-in battery charger which is optimized for lithium-ion and lithium-polymer batteries. The charger includes a current sensor for charging control, user programmable current regulator and high accuracy voltage regulator.

The charging current parameters are configured by using the UI tool. Whenever an adaptor is plugged-in, the charging circuit become activated. Reviving, pre-charging, constant current and constant voltage modes and re-charging functions are included. The maximum charging current is 350 mA. Figure 5-1 illustrates the charging curve of a battery.

FIGURE 5-1: BATTERY CHARGING CURVE



5.2 Voltage Monitoring

A 10-bit, successive approximation ADC (SAR ADC) provides a dedicated channel for voltage level detection. The warning level can be programmed by using the UI tool. The ADC provides a granular resolution to enable the MCU to take control over the charging process.

5.3 LDO

A built-in Low-Dropout Regulator (LDO) is used to convert the battery or adaptor power for power supply. It also integrates hardware architecture to control the power on/off procedure. The built-in programmable LDOs provide power for codec and digital I/O pads. Also, it is used to buffer the high input voltage from battery or adapter. This LDO requires 1 µF bypass capacitor.

5.4 Switching Regulator

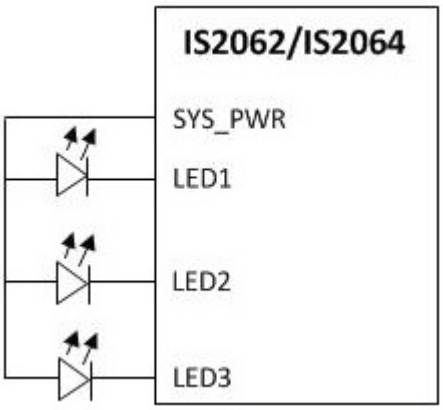
The built-in programmable output voltage regulator can convert the battery voltage to RF and baseband core power supply. This converter has a high conversion efficiency and a fast transient response.

5.5 LED Driver

The IS2062 SoC has two LED drivers and the IS2064 SoC has three LED drivers. The LED drivers provide enough sink current (16-step control and 0.35 mA for each step) and the LED can be connected directly to the IS2062/64 SoC. The LED settings can be configured using the UI tool.

Figure 5-2 illustrates the LED driver details.

FIGURE 5-2: LED DRIVER



Note: LED3 is only applicable for the IS2064 SoC.

5.6 Under Voltage Protection

When the SYS_PWR pin voltage drops below 2.9V, the system will shut-down automatically.

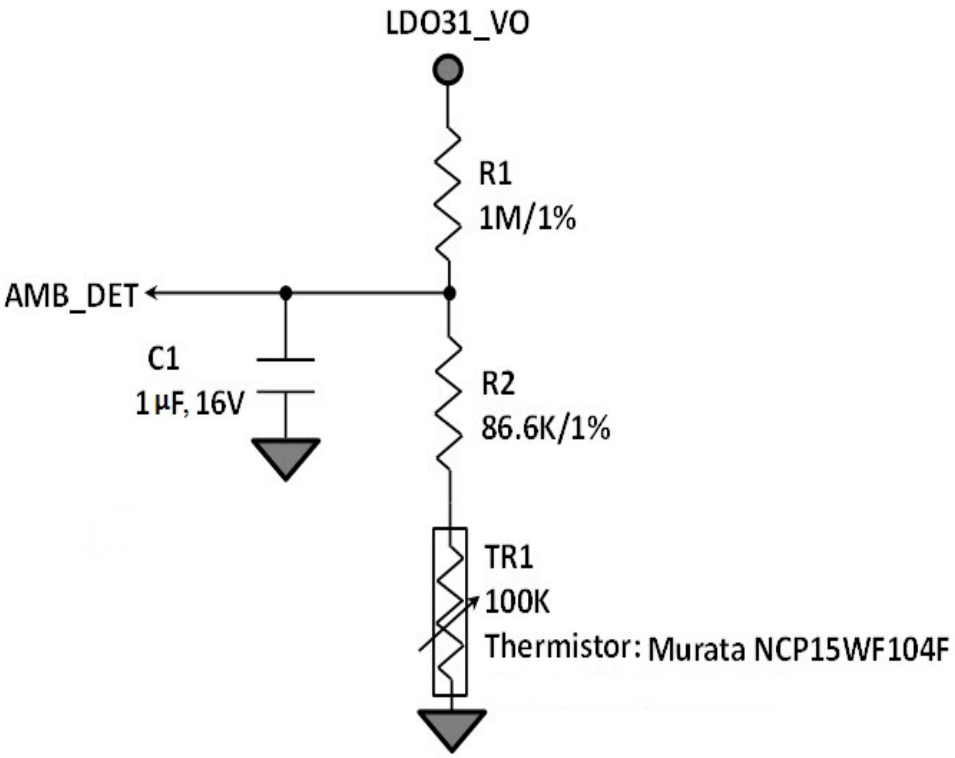
5.7 Ambient Detection

The IS2062/64 SoC has a built-in ADC for charger thermal protection.

Figure 5-3 illustrates the suggested circuit and thermistor, Murata NCP15WF104F. The charger thermal protection can avoid battery charge in restricted temperature range. The upper and lower limits for temperature values are configured by using the UI tool.

Note: Thermistor should be placed close to the battery in the user application for accurate temperature measurements and to enable thermal shutdown feature.

FIGURE 5-3: AMBIENT DETECTION



6.0 APPLICATION INFORMATION

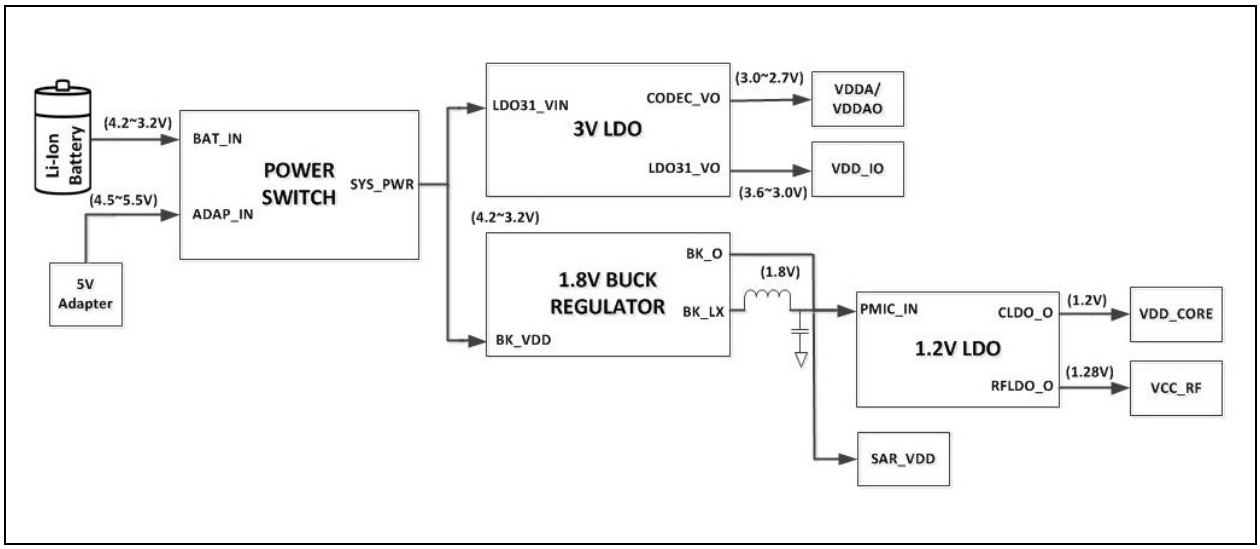
6.1 Power Supply

Figure 6-1 illustrates the connection from the BAT_IN pin to any other voltage supply pins of the IS2062/64 SoC.

The IS20/62/64 SoC is powered through the BAT_IN input pin. If battery is not connected, an external power supply must be provided as an input to the ADAP_IN pin.

Note:	When external power supply is connected to the ADAP_IN pin of the IS2062/64 SoC, the BAT_IN pin can be left open if battery is not connected.

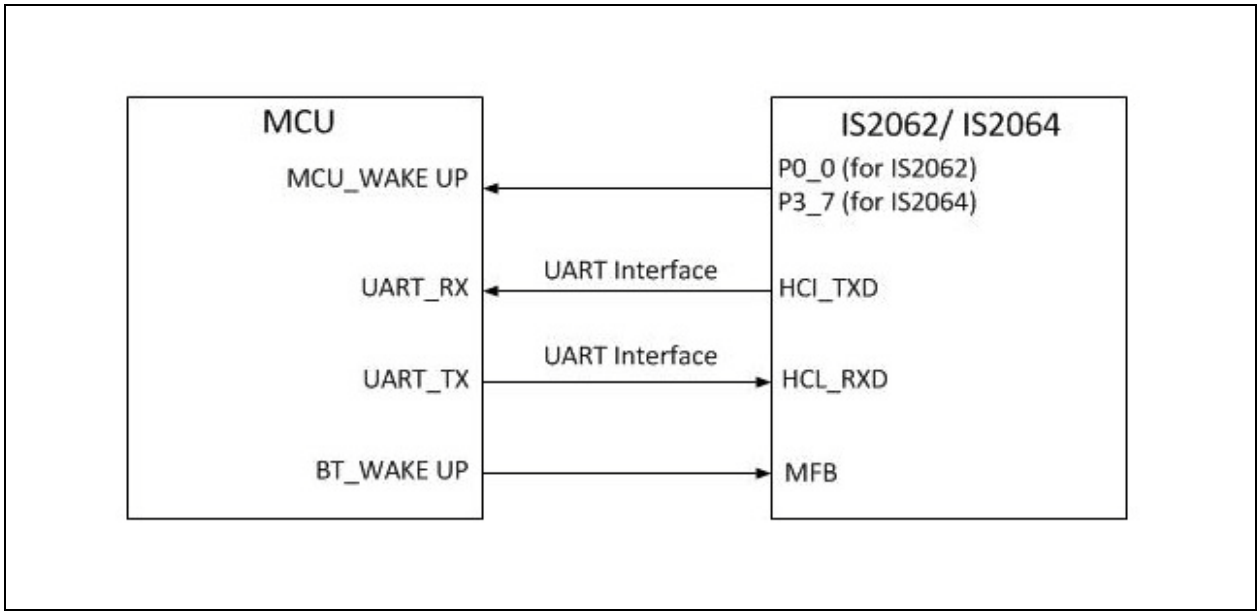
FIGURE 6-1: POWER TREE DIAGRAM



6.2 Host MCU Interface

Figure 6-2 illustrates the UART interface between the IS2062/64 SoC and MCU.

FIGURE 6-2: HOST MCU INTERFACE OVER UART



The MCU can control the IS2062/64 SoC over the UART interface and wakeup the SoC using the MFB pins, P0_0 (IS2062) and P3_7 (IS2064).

Refer to the "*UART_CommandSet*" document for a list of functions the IS2062/64 SoC supports and how to use the UI tool to set up the system using the UART command, which is available for download from the Microchip web site at: www.microchip.com/IS2062 and www.microchip.com/IS2064.

Figure 6-3 through Figure 6-8 illustrate the various UART control signal timing sequences.

FIGURE 6-3: POWER ON/OFF SEQUENCE

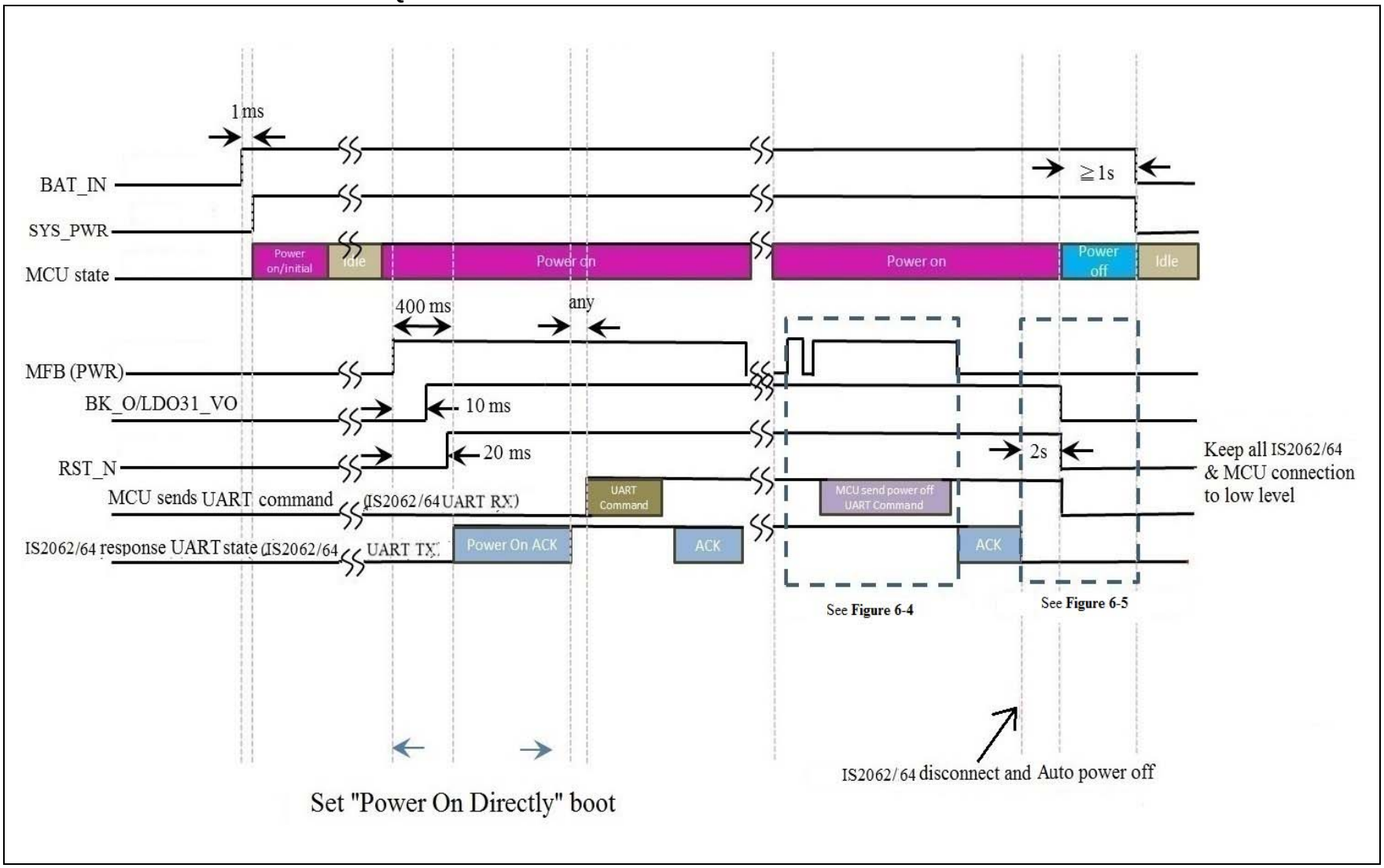


FIGURE 6-4: TIMING SEQUENCE OF RX INDICATION AFTER POWER ON

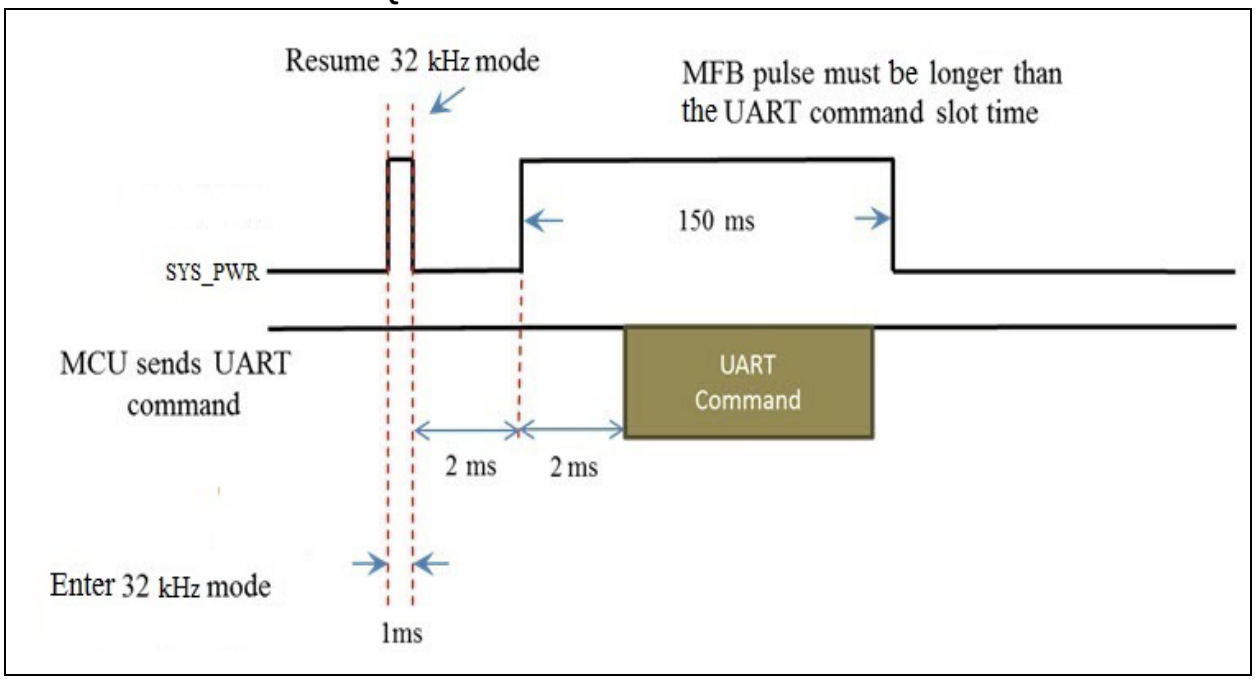
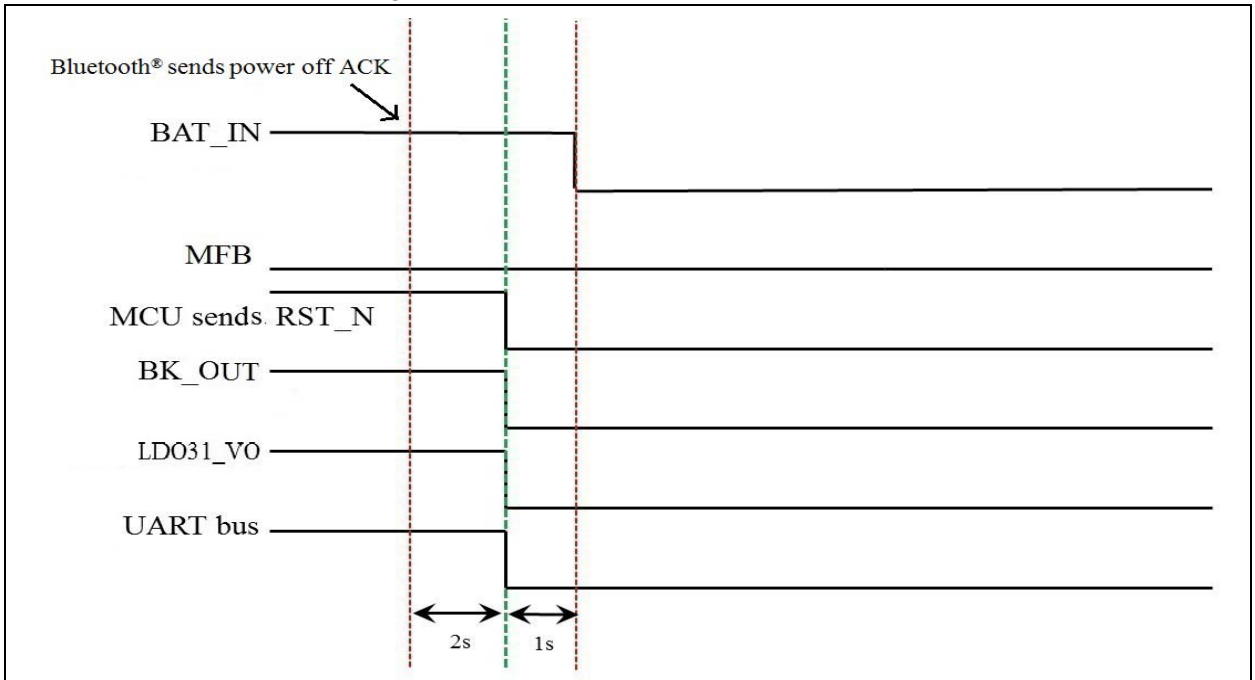


FIGURE 6-5: TIMING SEQUENCE OF POWER OFF



Note 1: EEPROM clock = 100 kHz.

2: For a byte write, 0.01 ms x 32 clock x 2 = 640 µs.

3: It is recommended to have ramp-down time more than 640 µs during power-off sequence to ensure safe operation of the device.

FIGURE 6-6: TIMING SEQUENCE OF POWER ON (NACK)

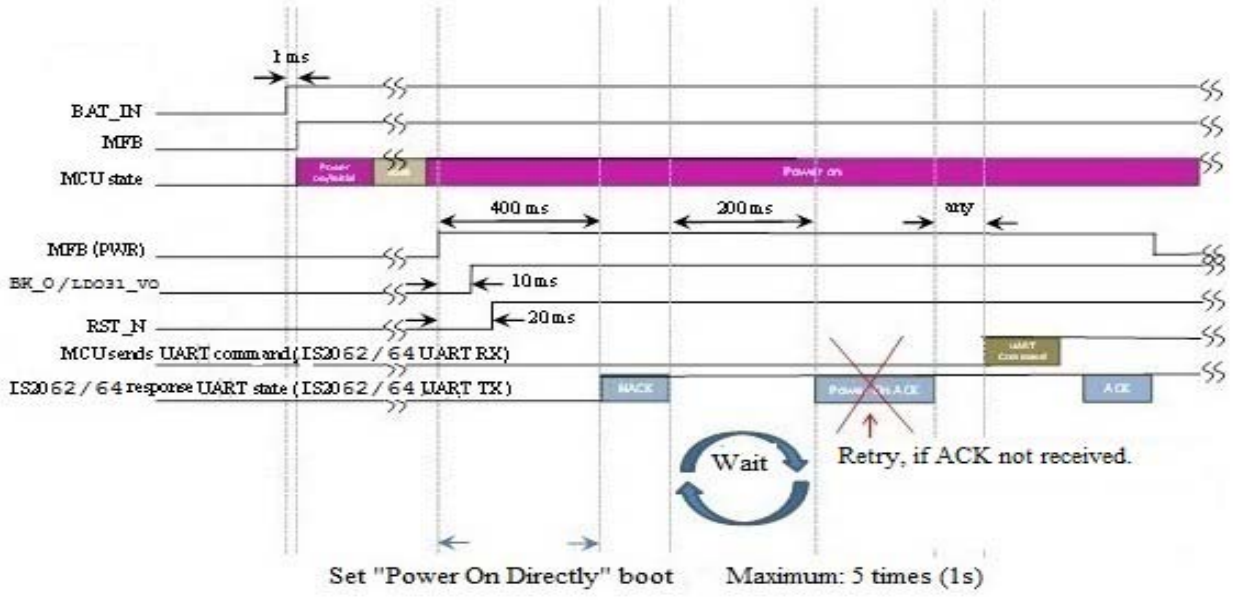
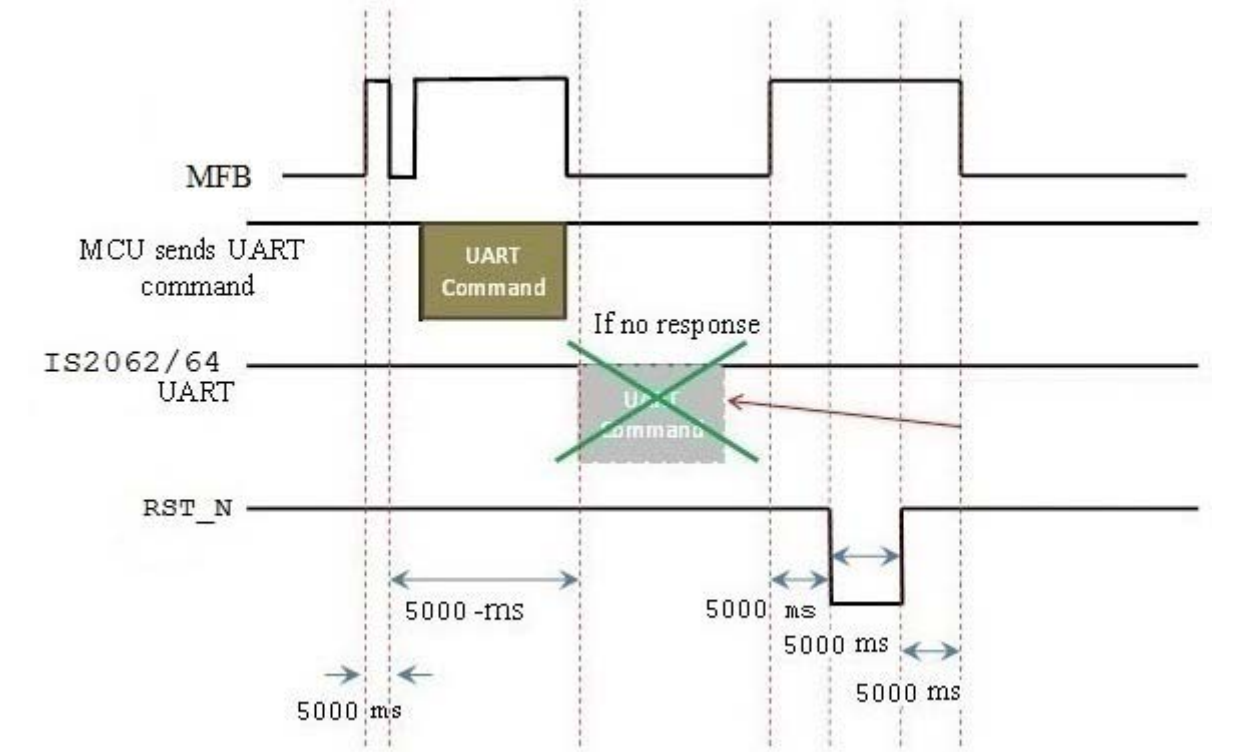
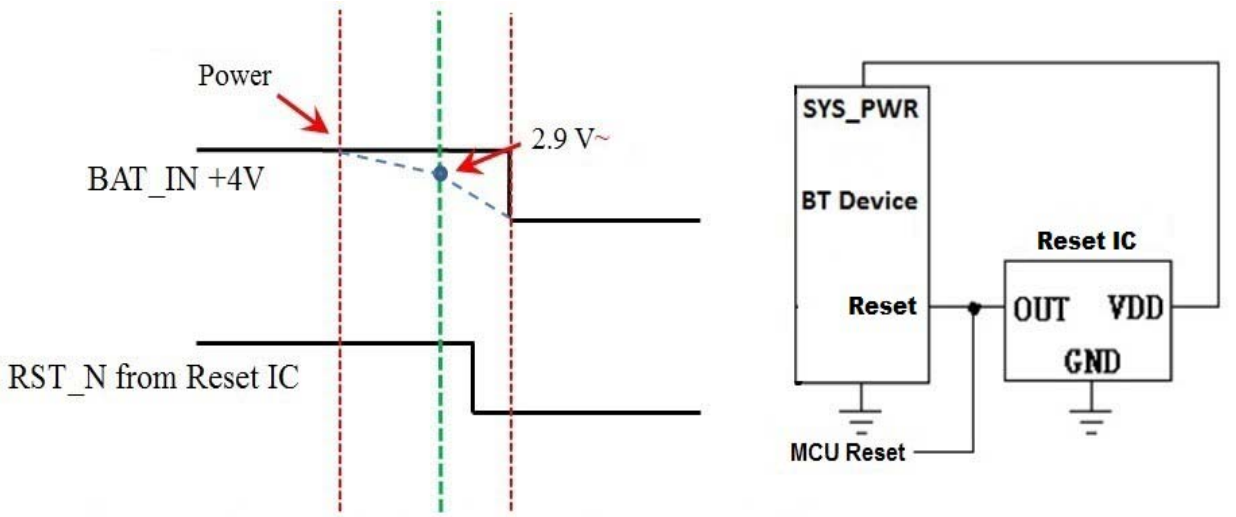


FIGURE 6-7: RESET TIMING SEQUENCE IN CASE OF NO RESPONSE FROM SOC TO HOST MCU



Note: If host MCU sends a UART command and the SoC does not respond, the MCU resends the UART command. If the SoC does not respond within 5 secs, the MCU will force the system to Reset.

FIGURE 6-8: TIMING SEQUENCE OF POWER DROP PROTECTION



Note 1: It is recommended to use the battery to provide the power supply at BAT_IN to the SoC.

2: If an external power source or a power adapter is utilized to provide power to the SoC (ADAP_IN), use a voltage supervisor IC.

3: The Reset IC output pin must be “Open drain” with delay time ≦ 10 ms, and the recommended part is G691L293T73.

6.3 Configuring and Programming

Configuration and firmware programming modes are entered according to the system configuration I/O pins. Table 6-1 provides the system configuration settings. The P2_0, P2_4 and EAN pins have internal pull ups.

TABLE 6-1: SYSTEM CONFIGURATION SETTINGS

P2_0	P2_4	EAN	Operating Mode
High	High	Flash code: Low; ROM code: High	APP mode (Normal operation)
Low	High	Flash code: Low; ROM code: High	Test mode (Write EEPROM)
Low	Low	High	Write Flash

6.4 General Purpose I/O Pins

The IS2062 SoC provides 10 GPIOs and the IS2064 SoC provides 15 GPIOs, and these GPIOs can be configured using the UI tool. Table 6-2 through Table 6-5 provide the GPIO configuration details of the IS2062/64 SoC.

The MFB pin must be configured as the power on/off key and the remaining pins can be configured for any one of the default functions as provided in Table 6-2 and Table 6-3.

TABLE 6-2: IS2062 I/O PIN CONFIGURATION

I/O Pin Name	Default Functions
MFB	Power on/off
P0_2	Play/Pause
P2_7	Volume Up
P0_5	Volume Down
P0_1	FWD
P0_3	REV

TABLE 6-3: IS2064 I/O PIN CONFIGURATION

I/O Pin Name	Default Functions
MFB	Power on/off
P0_2	Play/Pause
P2_7	Volume Up
P0_5	Volume Down
P3_3	FWD
P3_1	REV

Some pins can be configured to indicate or control the external devices. The most popular applications are NFC for easy pairing and Buzzer for indication and external audio amplifier for loud speaker.

TABLE 6-4: IS2062 I/O PIN (FOR ADDITIONAL FUNCTIONS)

I/O Configurable Features	Functions
P1_5	Slide switch
P0_4	NFC detect
P0_4 / P1_5	External AMP enable

TABLE 6-5: IS2064 I/O PIN FOR ADDED FUNCTIONS

I/O Configurable Features	Functions
P1_5	Slide switch
P0_4	NFC detect
P0_4 / P1_5	External AMP enable

6.5 I²S Mode Application

The IS2064 SoC provides an I²S digital audio output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2 and 96 kHz sampling rates for 16-bit and 24-bit data formats. The I²S setting can be configured by using the UI and DSP tools. The external codec or DSP interfaces with these pins: SCLK0, RFS0, DR0, and DT0 (pin no. 3, 2, 1, and 4).

Figure 6-9 and Figure 6-10 illustrate the I²S signal connection between the IS2064 SoC and an external DSP. Use the DSP tool to configure the IS2064 SoC as Master/Slave.

For additional information on timing specifications, refer to **8.1 "Timing specifications "**.

FIGURE 6-9: IS2064 IN I²S MASTER MODE

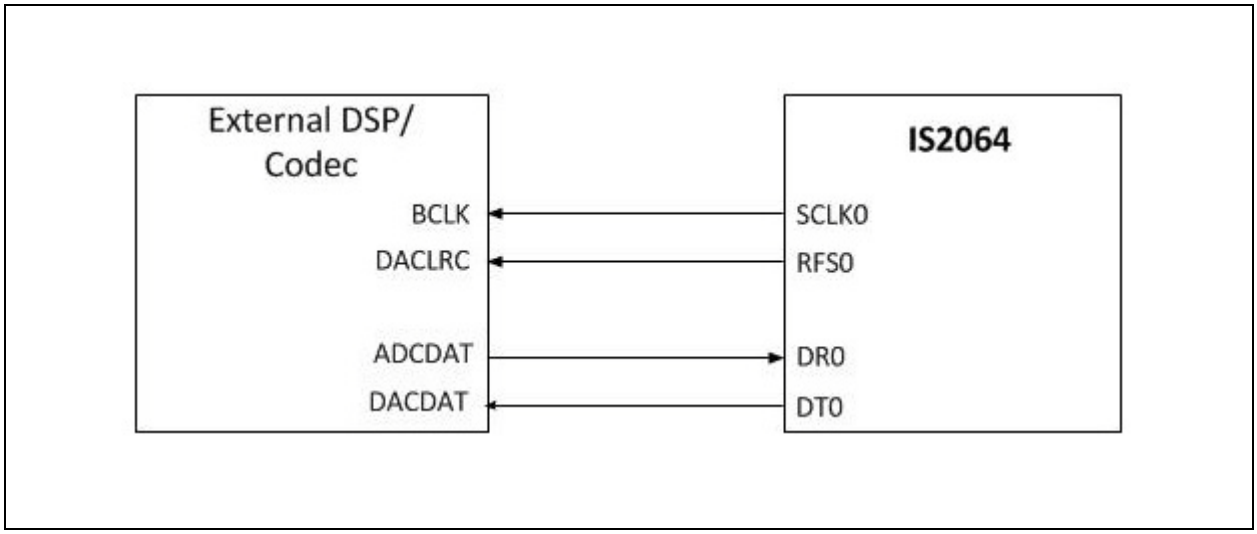
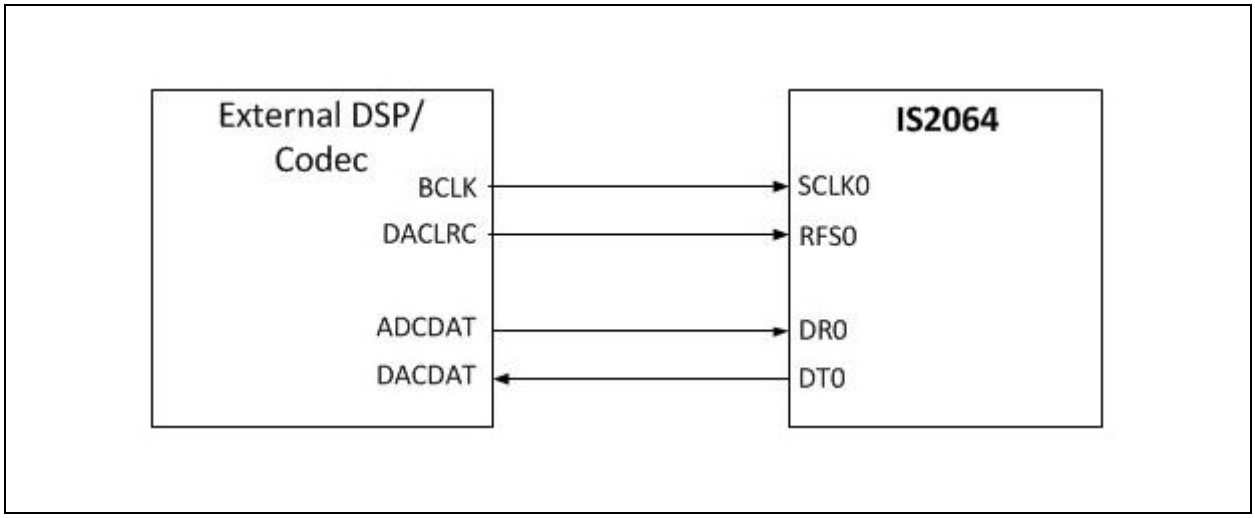


FIGURE 6-10: IS2064 SLAVE MODE



NOTES:

7.0 ANTENNA PLACEMENT RULE

Antenna placement affects the whole system performance of the Bluetooth integrated product. Antenna requires free space to radiate RF signals and it should not be surrounded by the GND plane.

Figure 7-1 illustrates a typical example of the antenna placement on the main application board with the GND plane.

FIGURE 7-1: ANTENNA PLACEMENT EXAMPLES

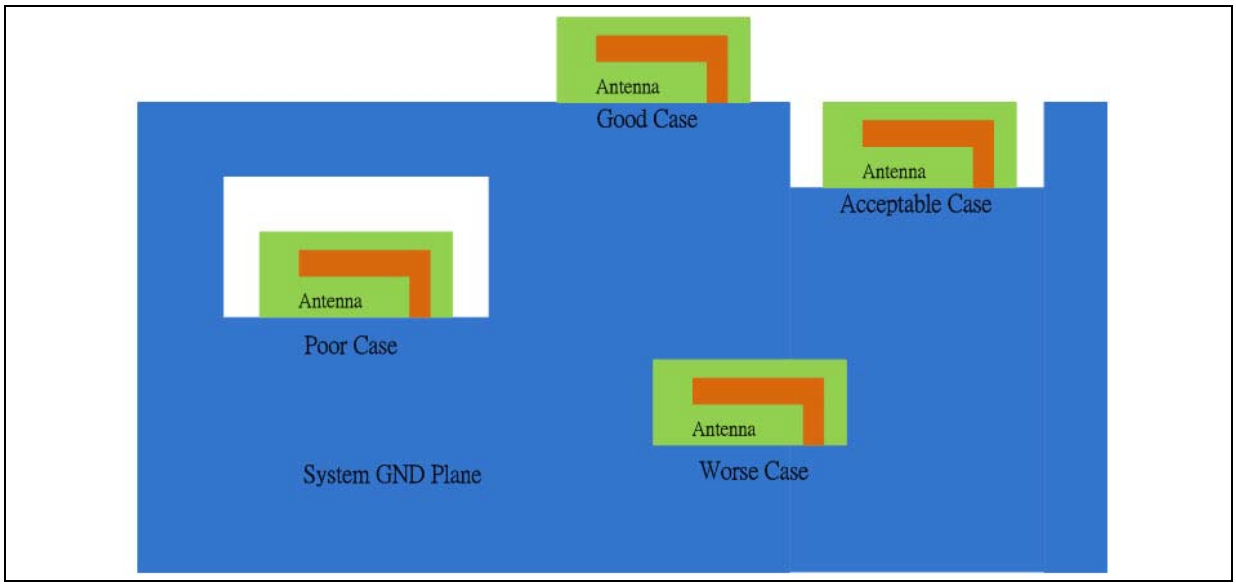
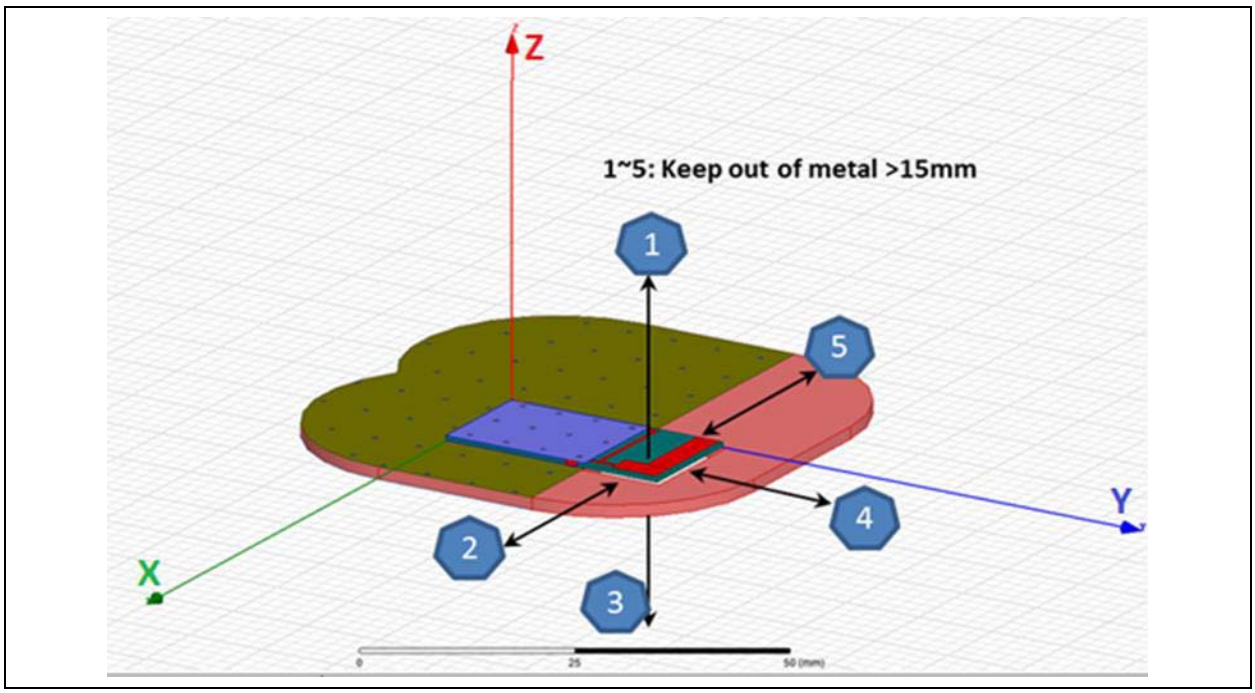


Figure 7-2 illustrates the keep-out area recommended for the antenna.

FIGURE 7-2: KEEP OUT AREA RECOMMENDATION FOR ANTENNA



For additional information on the antenna placement, refer to the specific antenna data sheet of the antenna manufacturer.

NOTES:

8.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the IS2062/64 stereo audio SoC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the IS2062/64 devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

Ambient temperature under bias ..... -20°C to +70°C
Storage temperature ..... -65°C to +150°C
Digital core supply voltage VDD_CORE ..... 0V to +1.35V
RF supply voltage VCC_RF ..... 0V to +1.35V
SAR ADC supply voltage SAR_VDD ..... 0V to +2.1V
Codec supply voltage VDDA/VDDAO ..... 0V to +3.3V
I/O supply voltage VDD_IO ..... 0V to +3.6V
Buck supply voltage BK_VDD ..... 0V to +4.3V
Supply voltage LDO31_VIN ..... 0V to +4.3V
Battery input voltage BAT_IN ..... 0V to +4.3V
Adapter input voltage ADAP_IN ..... 0V to +7V

Note: Stresses listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8-1 through Table 8-10 provide the recommended operating conditions and the electrical specifications of the IS2062/64 SoC.

TABLE 8-1: RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typical	Max.	Unit
VDD_CORE	Digital core supply voltage	1.14	1.2	1.26	V
VCC_RF	RF supply voltage	1.22	1.28	1.34	V
SAR_VDD	SAR ADC supply voltage	1.62	1.8	1.98	V
VDDA/VDDAO	Codec supply voltage	1.8	2.8	3.0	V
VDD_IO	I/O supply voltage	3.0	3.3	—	V
BK_VDD	Buck supply voltage	3	3.8	4.25	V
LDO31_VIN	Supply voltage	3	3.8	4.25	V
BAT_IN	Input voltage for battery	3.2	3.8	4.25	V
ADAP_IN	Input voltage for adaptor	4.5	5	5.5	V
$T_{OPERATION}$	Operation temperature	-20	+25	+70	ºC

Note: The PMU output powers, BK_O, CODEC_VO, RFLDO_O and CLDO_O, can be programmed through the EEPROM parameters.

TABLE 8-2: BUCK SWITCHING REGULATOR(2)

Parameter	Min.	Typical	Max.	Unit
Input Voltage	3.0	3.8	4.25	V
Output Voltage (I_{load} = 70 mA, V_{in} = 4V)	1.7	1.8	2.05	V
Output Voltage Accuracy	—	±5	—	%
Output Voltage Adjustable Step	—	50	—	mV/Step
Output Adjustment Range	-0.1	—	+0.25	V
Average Load Current (I_{LOAD})	120	—	—	mA
Conversion efficiency (BAT = 3.8V, I_{load} = 50 mA) (**Note 2**)	—	88	—	%
Quiescent Current (PFM)	—	—	40	µA
Output Current (peak)	200	—	—	mA
Shutdown Current	—	—	<1	µA

Note 1: Test condition: Temperature +25 ºC and wired inductor 10 µH.

2: These parameters are characterized, but not tested in manufacturing.

TABLE 8-3: LOW DROP REGULATOR(1,2)

Parameter		Min.	Typical	Max.	Unit
Input Voltage		3.0	3.8	4.25	V
Output Voltage	CODEC_VO	—	2.8	—	V
	LDO31_VO	—	3.3	—	
Output Accuracy (V_{IN} = 3.7V, I_{LOAD} = 100 mA, +27 ºC)		—	±5	—	%
Output current (average)		—	—	100	mA
Drop-out voltage (I_{load} = maximum output current)		—	—	300	mV
Quiescent Current (excluding load, I_{load} < 1 mA)		—	45	—	µA
Shutdown Current		—	—	<1	µA

Note 1: Test condition: Temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-4: BATTERY CHARGER(1, 3)

Parameter		Min.	Typical	Max.	Unit
Input Voltage (ADAP_IN)		4.5	5.0	5.5	V
Supply current to charger only		—	3	4.5	mA
Maximum Battery Fast Charge Current	Headroom > 0.7V (ADAP_IN = 5V)	—	350	—	mA
	Headroom = 0.3V~0.7V (ADAP_IN = 4.5V) (**Note 2**)	—	175	—	mA
Trickle Charge Voltage Threshold		—	3	—	V
Battery Charge Termination Current, (% of Fast Charge Current)		—	10	—	%

Note 1: Headroom = V_{ADAP_IN} - V_{BAT}.

2: When V_{ADAP_IN} - V_{BAT} > 2V, the maximum fast charge current is 175 mA for thermal protection.

3: These parameters are characterized but not tested in manufacturing.

TABLE 8-5: LED DRIVER(1, 2)

Parameter	Min.	Typical	Max.	Unit
Open-drain Voltage	—	—	3.6	V
Programmable Current Range	0	—	5.25	mA
Intensity Control	—	16	—	step
Current Step	—	0.35	—	mA
Power Down Open-drain Current	—	—	1	µA
Shutdown Current	—	—	1	µA

Note 1: Test condition: BK_O = 1.8V with temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-6: AUDIO CODEC DIGITAL TO ANALOG CONVERTER(4)

T = +25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz					
Parameter (Condition)		**Min.**	**Typical**	**Max.**	**Unit**
Output Sampling Rate		—	128	—	f_s
Resolution		16	—	20	Bit
Output Sample Rate		8	—	48	kHz
Signal to Noise Ratio (**Note 1**) (SNR @cap-less mode) for 48 kHz		—	96	—	dB
Signal to Noise Ratio (**Note 1**) (SNR @single-end mode) for 48 kHz		—	98	—	dB
Digital Gain		-54	—	4.85	dB
Digital Gain Resolution		—	2~6	—	dB
Analog Gain		-28	—	3	dB
Analog Gain Resolution		—	1	—	dB
Output Voltage Full-scale Swing (AVDD = 2.8V)		495	742.5	—	mV/rms
Maximum Output Power (16 Ohm load)		—	34.5	—	mW
Maximum Output Power (32 Ohm load)		—	17.2	—	mW
Allowed Load	Resistive	—	16	O.C.	Ohm
	Capacitive	—	—	500	pF
THD+N (16 Ohm load) (**Note 2**)		—	0.05	—	%
Signal to Noise Ratio (SNR @ 16 Ohm load) (**Note 3**)	—	—	98	—	dB

Note 1: f_{in}=1 kHz, B/W=20~20 kHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load = 100 kOhm.

2: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, -1dBFS signal, Load=16 Ohm.

3: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, THD+N < 0.05%, 0dBFS signal, Load = 16 Ohm.

4: These parameters are characterized but not tested in manufacturing.

TABLE 8-7: AUDIO CODEC ANALOG TO DIGITAL CONVERTER(2)

T = +25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz				
Parameter (Condition)	**Min.**	**Typical**	**Max.**	**Unit**
Resolution	—	—	16	Bit
Output Sample Rate	8	—	48	kHz
Signal to Noise Ratio (**Note 1**) (SNR @MIC or Line-in mode)	—	92	—	dB
Digital Gain	-54	—	4.85	dB
Digital Gain Resolution	—	2~6	—	dB
MIC Boost Gain	—	20	—	dB
Analog Gain	—	—	60	dB
Analog Gain Resolution	—	2.0	—	dB
Input full-scale at maximum gain (differential)	—	4	—	mV/rms
Input full-scale at minimum gain (differential)	—	800	—	mV/rms
3 dB bandwidth	—	20	—	kHz
Microphone mode (input impedance)	—	24	—	kOhm
THD+N (microphone input) at 30mVrms input	—	0.02	—	%

Note 1: f_{in}=1 kHz, B/W=20~20 kHz, A-weighted, THD+N < 1%, 150 mVpp input.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-8: TRANSMITTER SECTION FOR BDR AND EDR(1, 2)

Parameter	**Min.**	**Typical**	**Max.**	**Bluetooth specification**	**Unit**
Transmit power	—	2(3)	4	-6 to 4	dBm
Relative transmit power	-4	-1.8	1	-4 to 1	dB

Note 1: The RF TX power is modulation value.

2: The RF Transmit power is calibrated during production using MP tool software and MT8852 Bluetooth Test equipment.

3: Test condition: VCC_RF = 1.28V, temperature +25 ºC.

TABLE 8-9: RECEIVER SECTION FOR BDR AND EDR(1, 2)

	Modulation	**Min.**	**Typical**	**Max.**	**Bluetooth specification**	**Unit**
Sensitivity at 0.1% BER	GFSK	—	-89	—	≤-70	dBm
Sensitivity at 0.01% BER	π/4 DQPSK	—	-90	—	≤-70	dBm
	8 DPSK	—	-83	—	≤-70	dBm

Note 1: Test condition: VCC_RF = 1.28V, temperature +25 ºC.

2: These parameters are characterized, but not tested in manufacturing.

TABLE 8-10: SYSTEM CURRENT CONSUMPTION OF IS2062(1, 2)

System Status	Typical	Max.	Unit
System Off Mode	—	10	µA
Stop Advertising (Samsung S5 (SM-G900I)/Android™ 4.4.2)			
Standby Mode	0.57	—	mA
Link Mode	0.5	—	mA
ESCO Link	15.1	—	mA
A2DP Link	14.3	—	mA
Stop Advertising (iPhone® 6 / iOS 8.4)			
Standby Mode	0.6	—	mA
Link Mode	0.6	—	mA
SCO Link	15.3	—	mA
A2DP Link	15.4	—	mA

Note 1: Standby Mode: Power-on without Bluetooth link; Link Mode: With Bluetooth link in low-power mode.

2: Current consumption values are taken with the BM62 EVB as a test platform, BAT_IN = 3.8V. Distance between smart phone and EVB is 30 cm. Speaker is without loading.

8.1 Timing specifications

Figure 8-1 and Figure 8-2 illustrate the clock and data timing specifications.

FIGURE 8-1: TIMING FOR I²S MODES (MASTER/SLAVE)

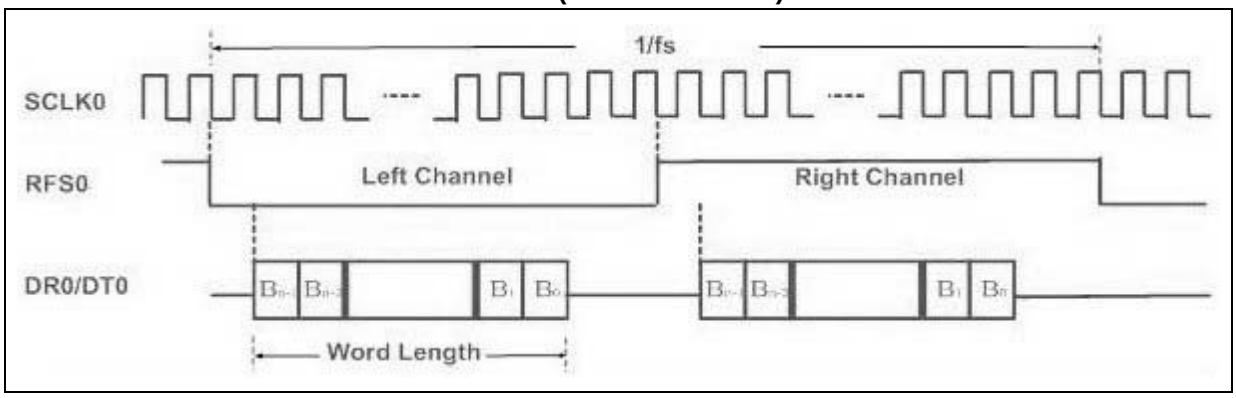
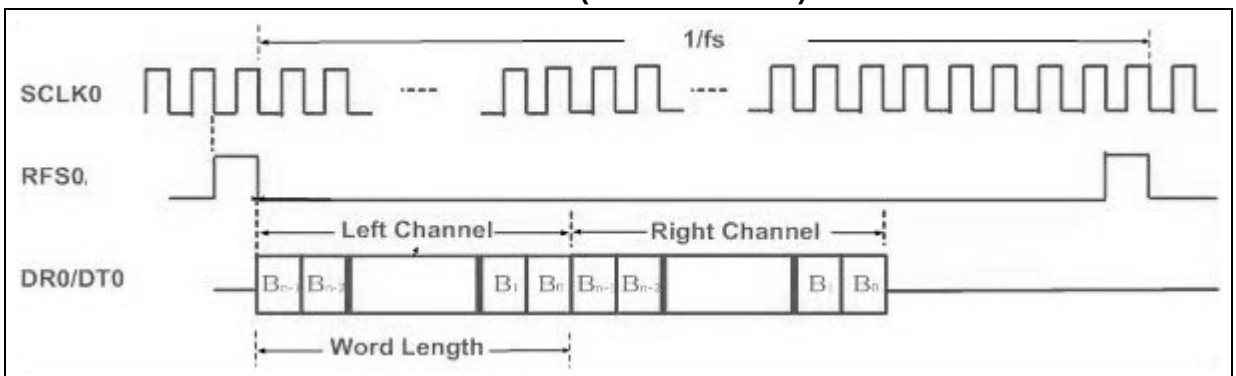


FIGURE 8-2: TIMING FOR PCM MODES (MASTER/SLAVE)



Note 1: f_S: 8,16, 32, 44.1, 48, 88.2 and 96 kHz.

2: SCLK0: 64 x f_S / 256 x f_S.

3: Word length: 16-bit and 24-bit.

Figure 8-3 illustrates the audio interface timing and Table 8-11 provides the audio interface timing specifications.

FIGURE 8-3: AUDIO INTERFACE TIMING

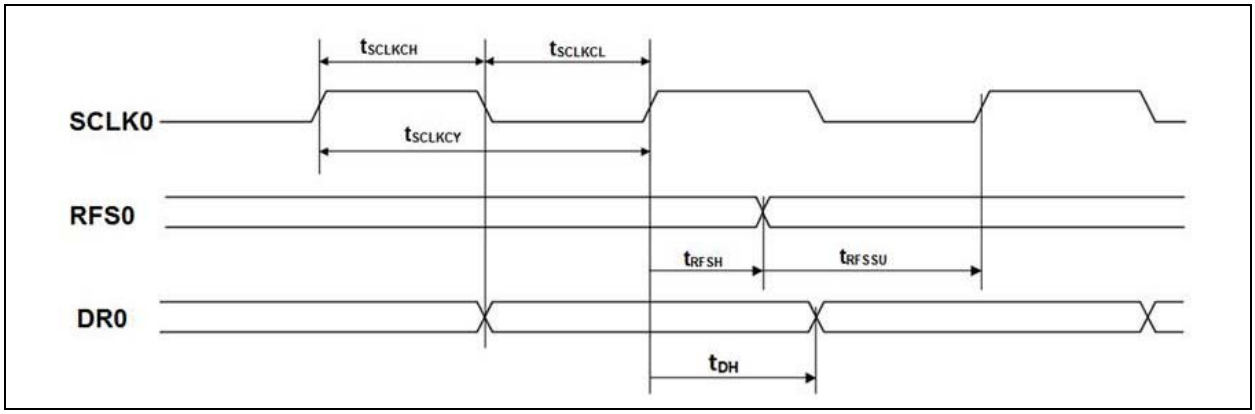


TABLE 8-11: AUDIO INTERFACE TIMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK0 Duty Ratio	d_{SCLK}	—	50	—	%
SCLK0 cycle time	t_{SCLKCY}	50	—	—	ns
SCLK0 pulse width high	t_{SCLKCH}	20	—	—	ns
SCLK0 pulse width low	t_{SCLKCL}	20	—	—	ns
RFS0 set-up time to SCLK0 rising edge	t_{RFSSU}	10	—	—	ns
RFS0 hold time from SCLK0 rising edge	t_{RFSH}	10	—	—	ns
DR0 hold time from SCLK0 rising edge	t_{DH}	10	—	—	ns

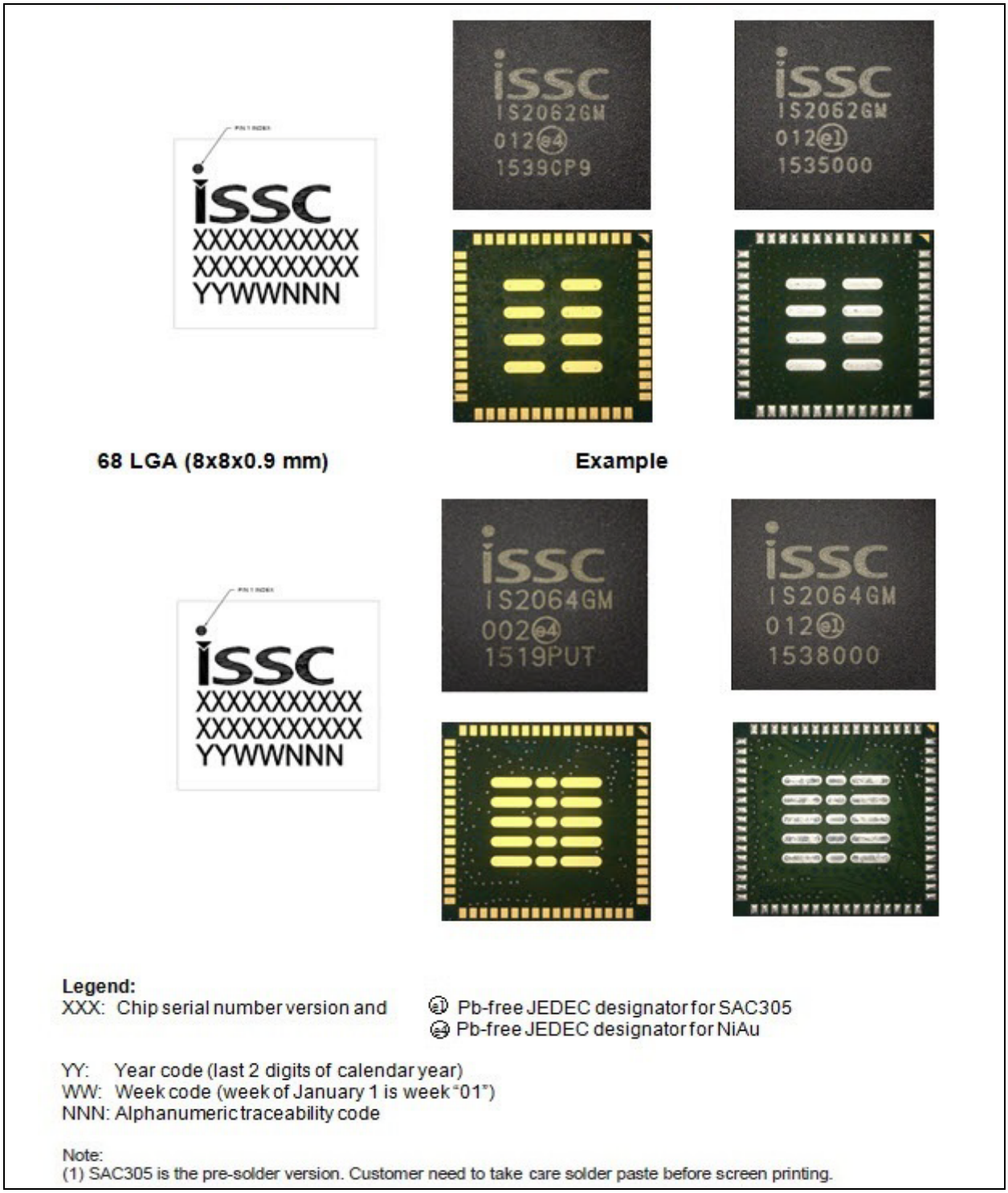
Note: Test Conditions: Slave Mode, f_s = 48 kHz, 24-bit data and SLK0 period = 256 f_s.

9.0 PACKAGING INFORMATION

9.1 Package Marking Information

Figure 9-1 illustrates the package marking information of the IS2062/64 SoC.

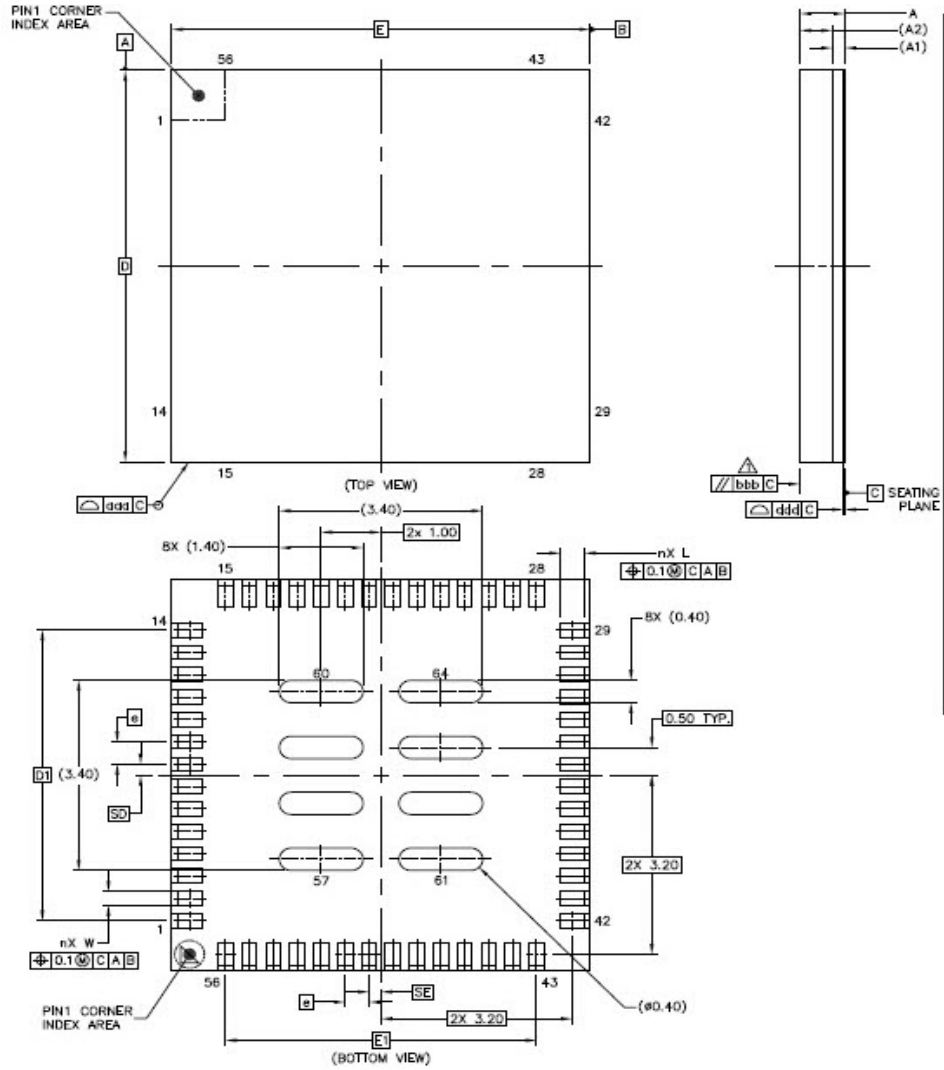
FIGURE 9-1: PACKAGE MARKING INFORMATION



9.2 Package Details

Figure 9-2 and Figure 9-3 illustrate the package details of the IS2062 SoC.

FIGURE 9-2: IS2062 - NIAU PACKAGE DETAILS

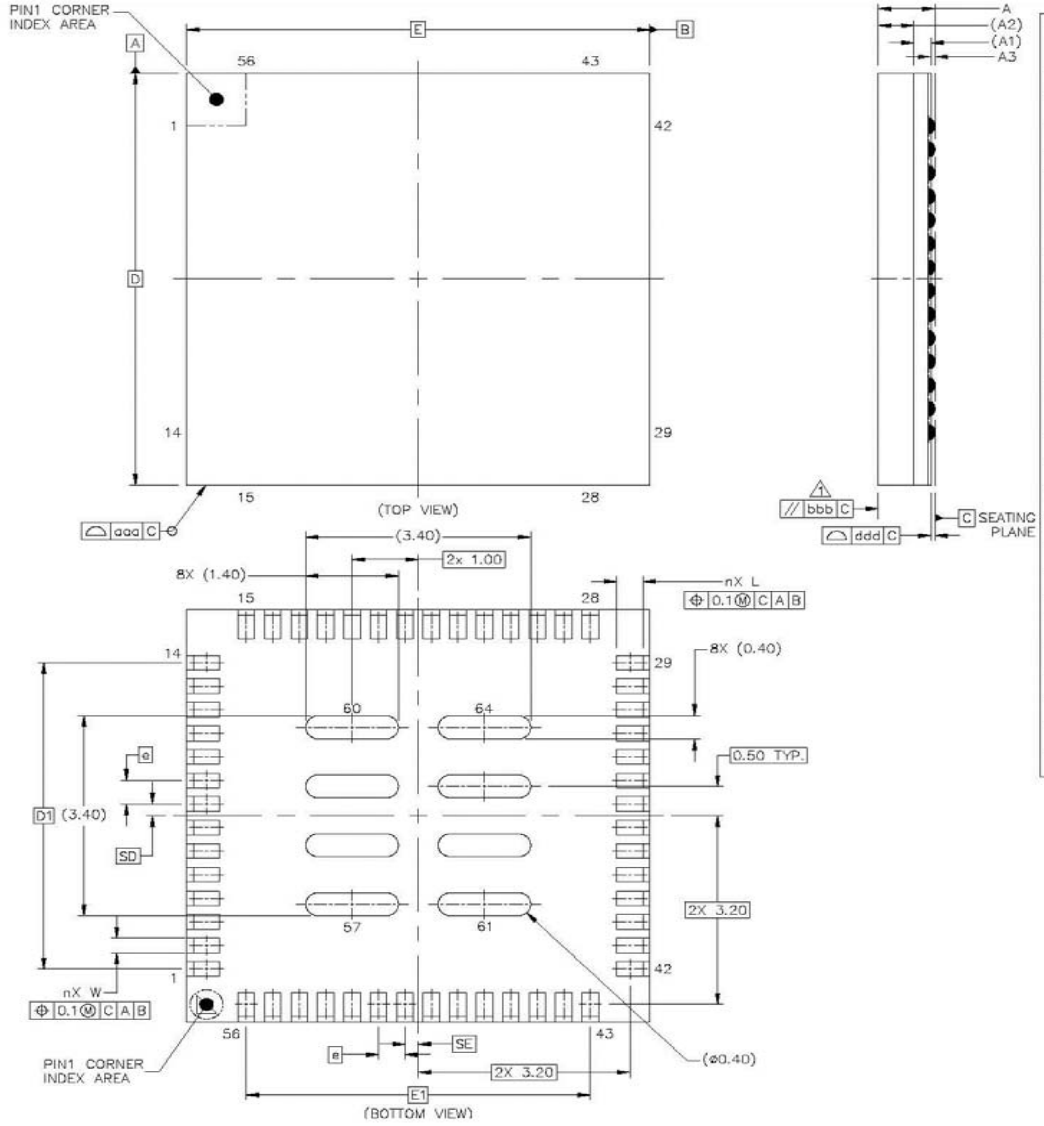


	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.9
SUBSTRATE THICKNESS	A1		0.21	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		7	BSC
	E		7	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		56	
EDGE BALL CENTER TO CENTER	D1		5.2	BSC
	E1		5.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

NOTES:

⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

FIGURE 9-3: IS2062 - SAC305 PACKAGE DETAILS



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.26	REF
MOLD THICKNESS	A2		0.54	REF
PRE-SOLDER	A3	0.02	---	1
BODY SIZE	D		7	BSC
	E		7	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		56	
EDGE BALL CENTER TO CENTER	D1		5.2	BSC
	E1		5.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

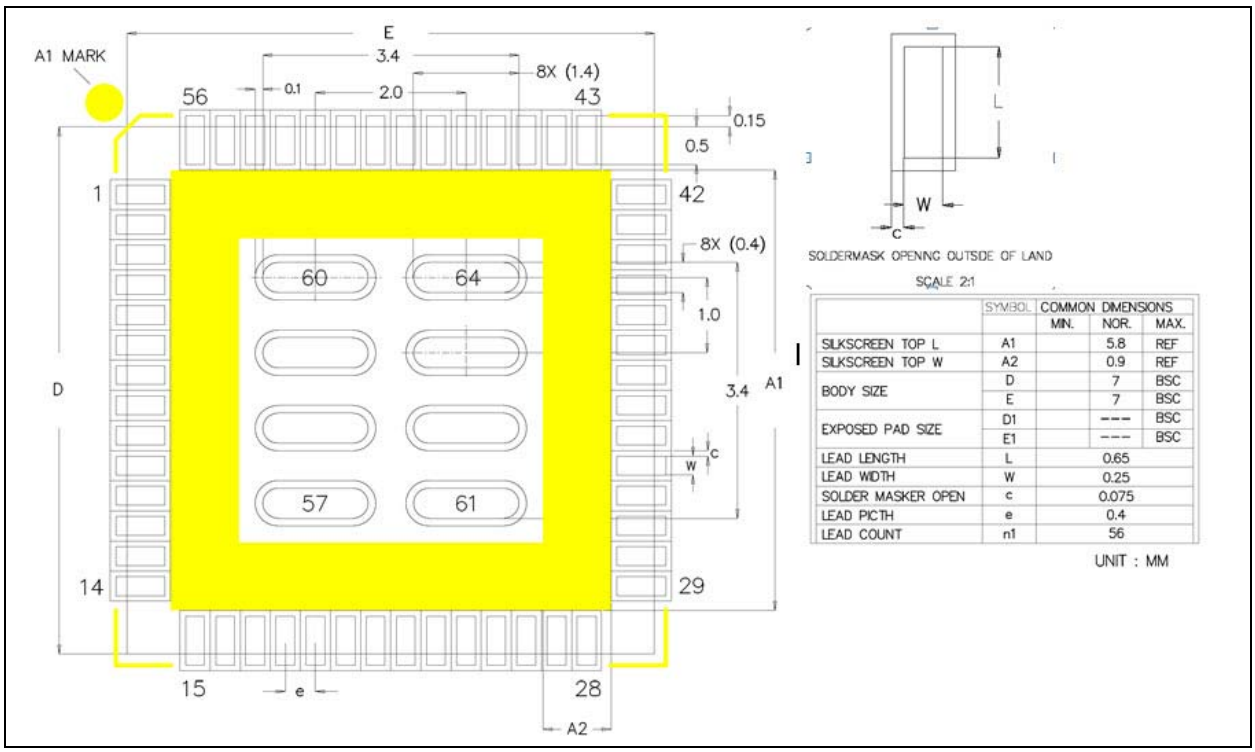
NOTES:

1. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.3 Footprint Dimensions

Figure 9-4 illustrates the footprint dimensions of the IS2062 SoC.

FIGURE 9-4: IS2062 FOOTPRINT DIMENSIONS



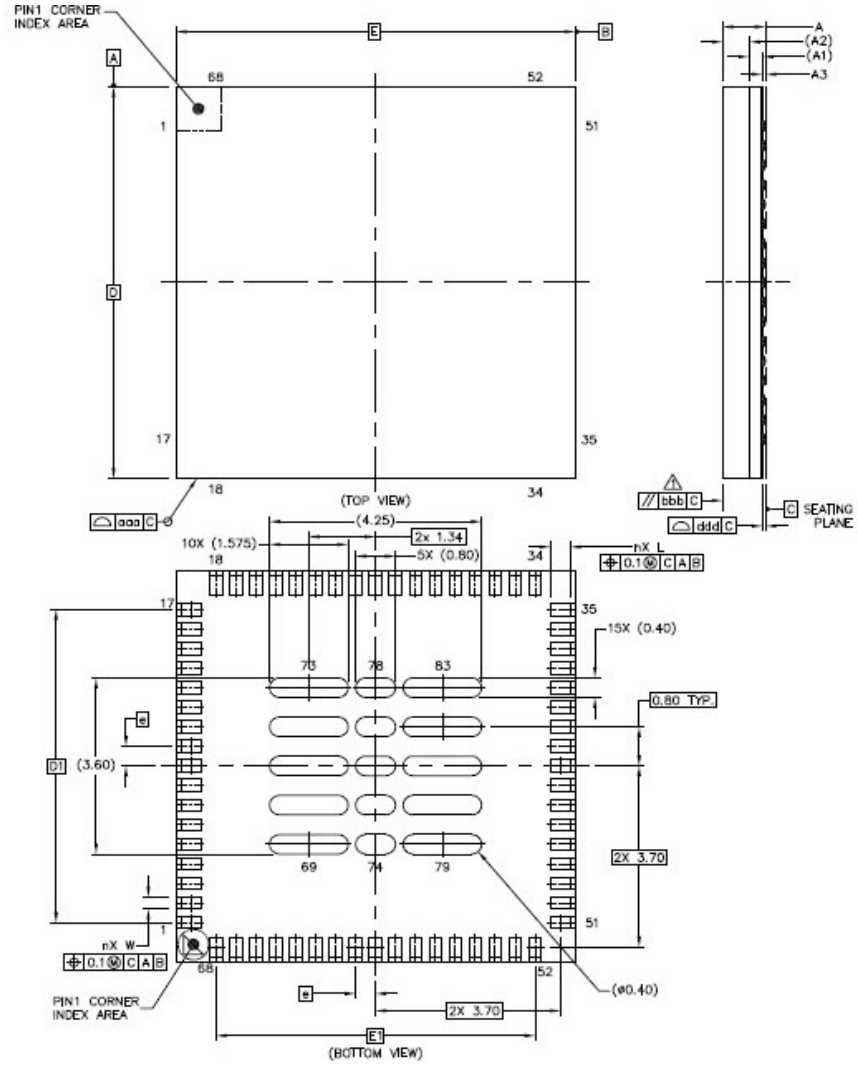
	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		5.8	REF
SILKSCREEN TOP W	A2		0.9	REF
BODY SIZE	D		7	BSC
	E		7	BSC
EXPOSED PAD SIZE	D1		---	BSC
	E1		---	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.25	
SOLDER MASKER OPEN	c		0.075	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		56	

UNIT : MM

9.4 Package Details

Figure 9-5 and Figure 9-6 illustrate the package details of the IS2064 SoC.

FIGURE 9-5: IS2064 -NIAU PACKAGE DETAILS

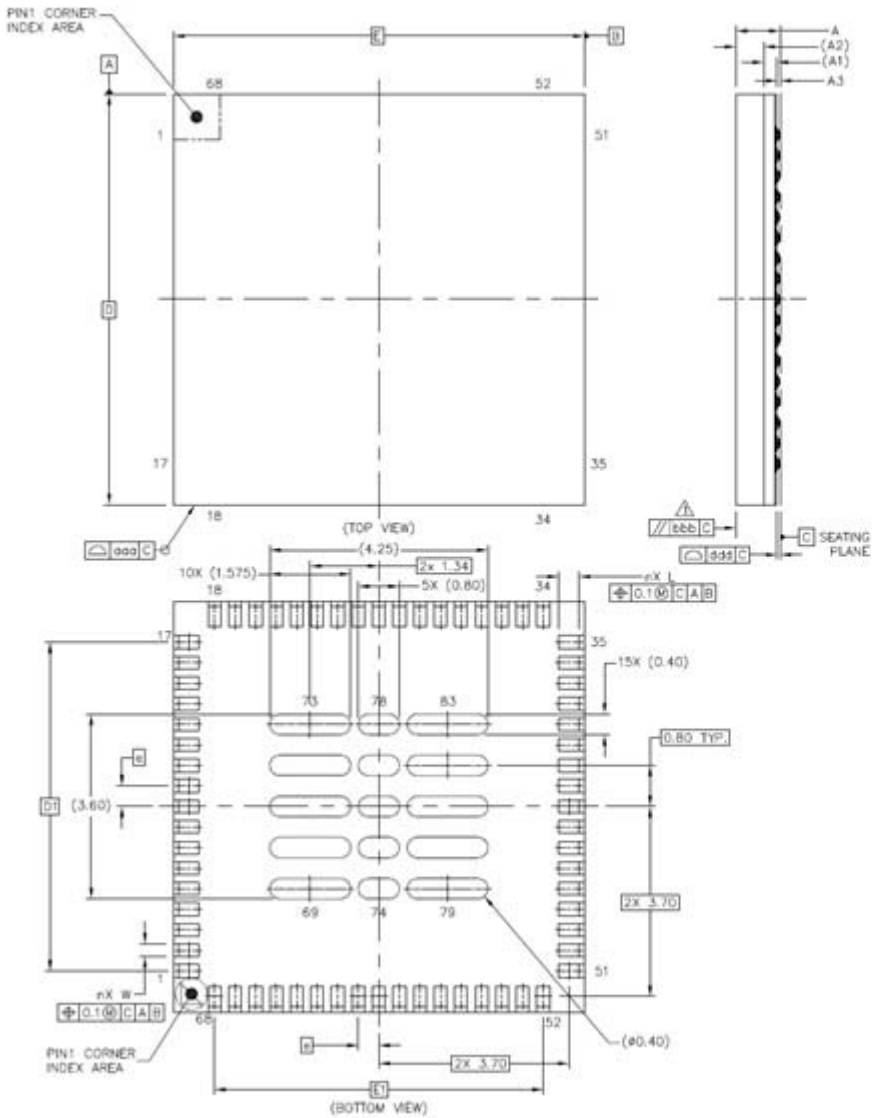


	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.26	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		8	BSC
	E		8	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		68	
EDGE BALL CENTER TO CENTER	D1		6.4	BSC
	E1		6.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER	A3	0.02	---	0.1
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

NOTES:

⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

FIGURE 9-6: IS2064 - SAC305 PACKAGE DETAILS



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.26	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		8	BSC
	E		8	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		68	
EDGE BALL CENTER TO CENTER	D1		6.4	BSC
	E1		6.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER	A3	0.02	---	0.1
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

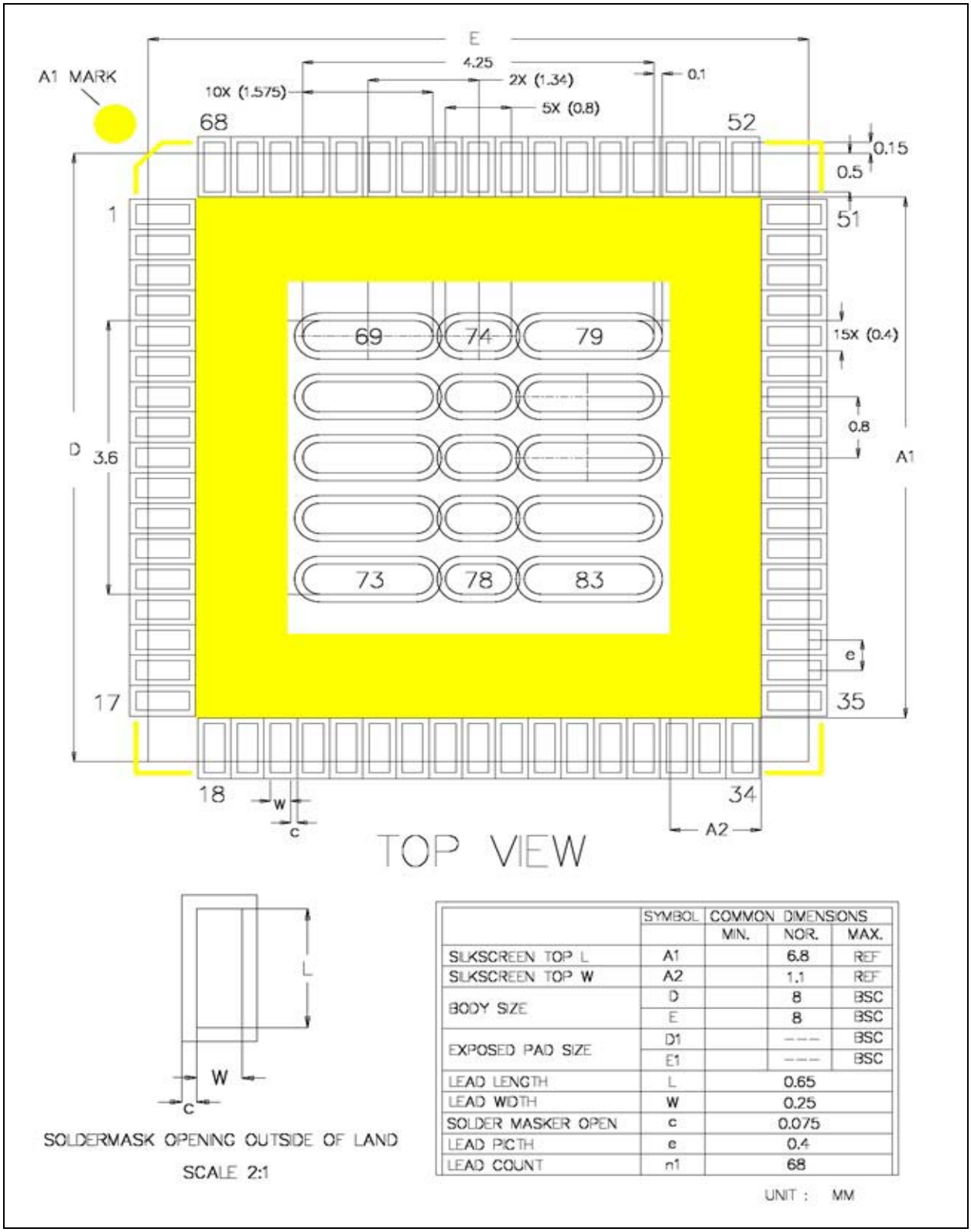
NOTES:

1. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.5 Footprint Dimensions

Figure 9-7 illustrates the footprint dimensions of the IS2064 SoC.

FIGURE 9-7: IS2064 FOOTPRINT DIMENSIONS



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		6.8	REF
SILKSCREEN TOP W	A2		1.1	REF
BODY SIZE	D		8	BSC
	E		8	BSC
EXPOSED PAD SIZE	D1		---	BSC
	E1		---	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.25	
SOLDER MASKER OPEN	c		0.075	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		68	

UNIT : MM

NOTES:

10.0 REFLOW PROFILE AND STORAGE CONDITION

Figure 10-1 and Figure 10-2 illustrate reflow profiles and stencil information of the IS2062/64 SoC.

10.1 Stencil of SMT Assembly Suggestion

10.1.1 STENCIL TYPE & THICKNESS

- Laser cutting
- Stainless steel
- Thickness: 0.5 mm Pitch, thickness more than 0.15 mm

10.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

- Aspect ratio (width/thickness) more than 1.5
- Aperture shape
  - The stencil aperture is designed to match the pad size on the PCB
  - Oval-shape opening is used to get the optimum paste release
  - Rounded corners to minimize clogging
  - Positive taper walls (5° tapering) with bottom opening larger than the top

10.1.3 APERTURE DESIGN FOR THERMAL PAD

- Small multiple openings are used instead of one big opening, see Figure 10-1
- 60~80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper walls (5° tapering) with bottom opening larger than the top, see Figure 10-2

FIGURE 10-1: REFLOW PROFILE APERTURE DESIGN

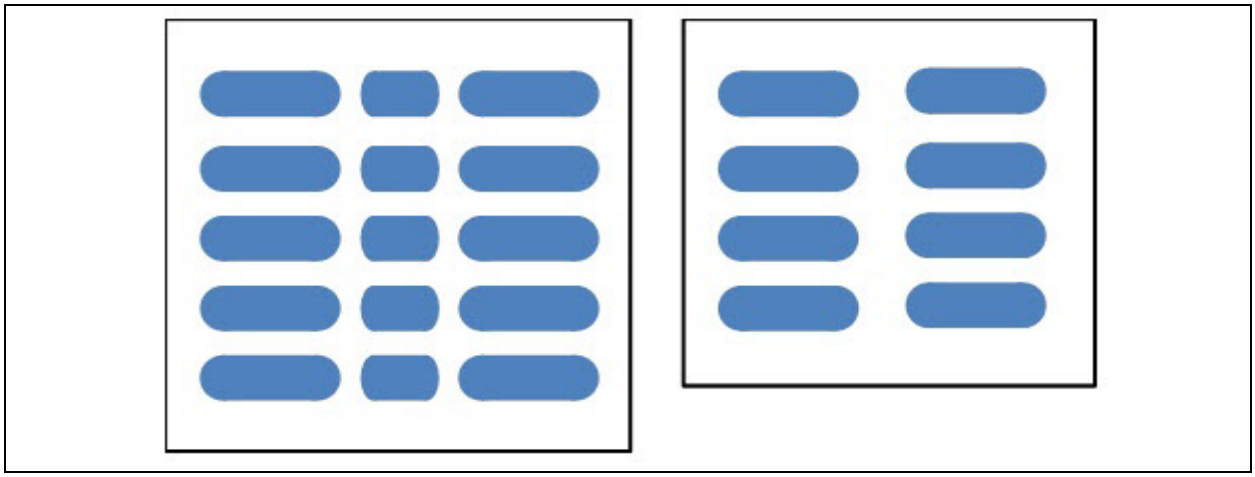
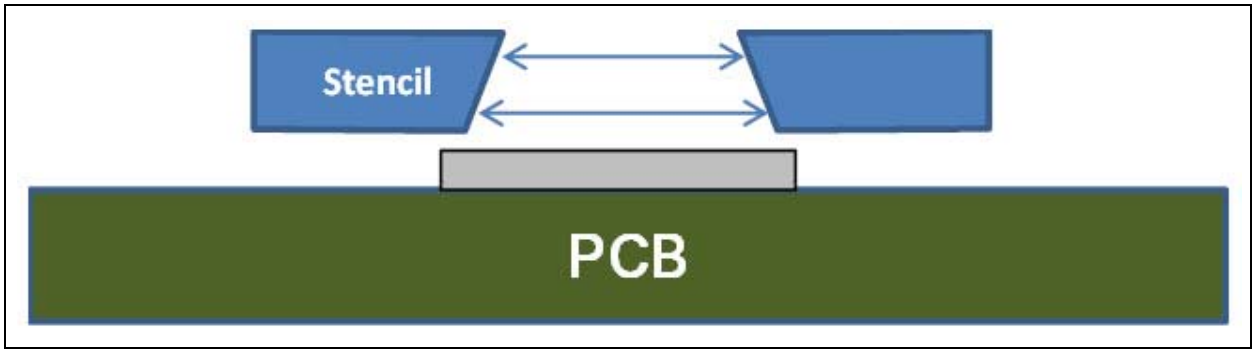


FIGURE 10-2: STENCIL TYPE

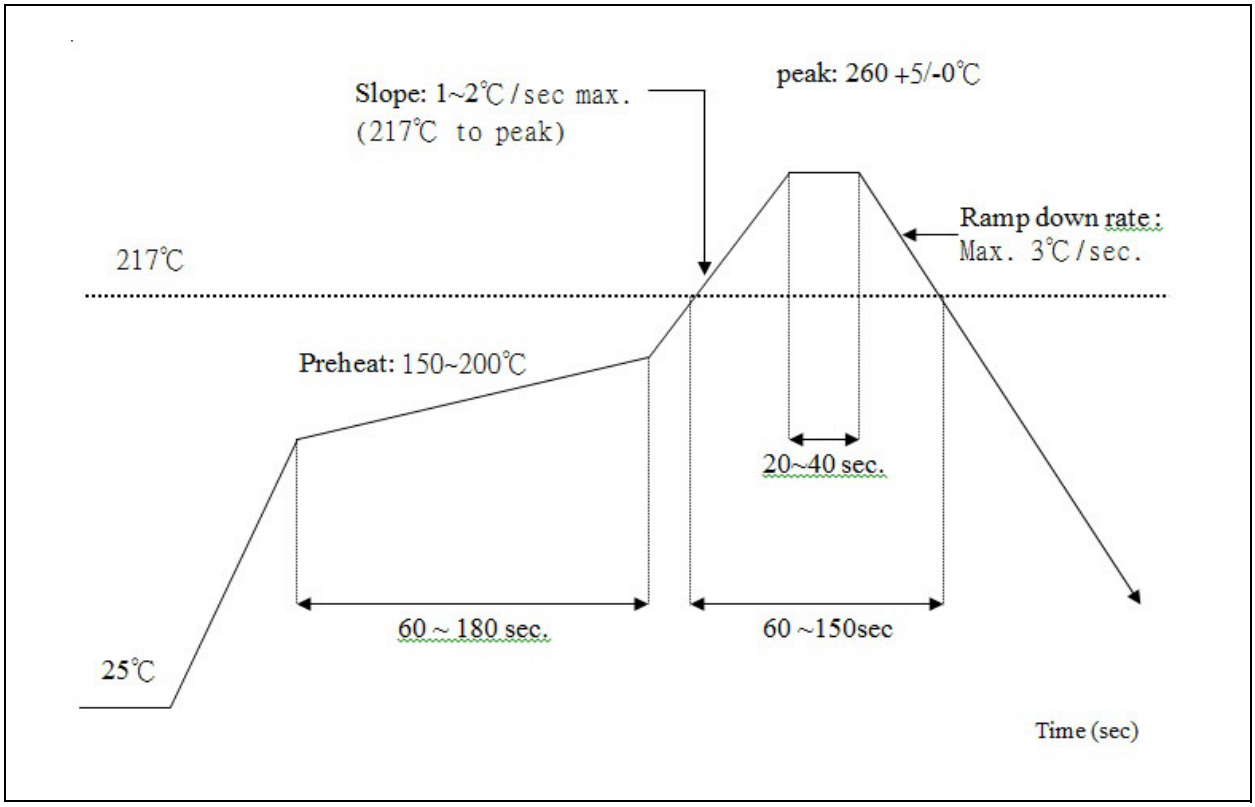


10.2 Reflow Condition

Figure 10-3 illustrates the reflow profile and the following are its specific features:

- Standard condition: IPC/JEDEC J-STD-020
- Preheat: 150~200 ℃ ~60~180 seconds
- Average ramp-up rate (+217 ℃ to peak): 1~2 ℃ /sec max
- Temperature maintain above 217: 60~150 seconds
- Time within +5℃ of actual peak temperature: 20 ~ 40 seconds
- Peak temperature: 260 +5/-0 ℃
- Ramp-down rate (peak to +217℃): +3℃/sec. max
- Time +25 ℃ to peak temperature: 8 minutes max
- Cycle interval: 5 minutes

FIGURE 10-3: REFLOW PROFILE



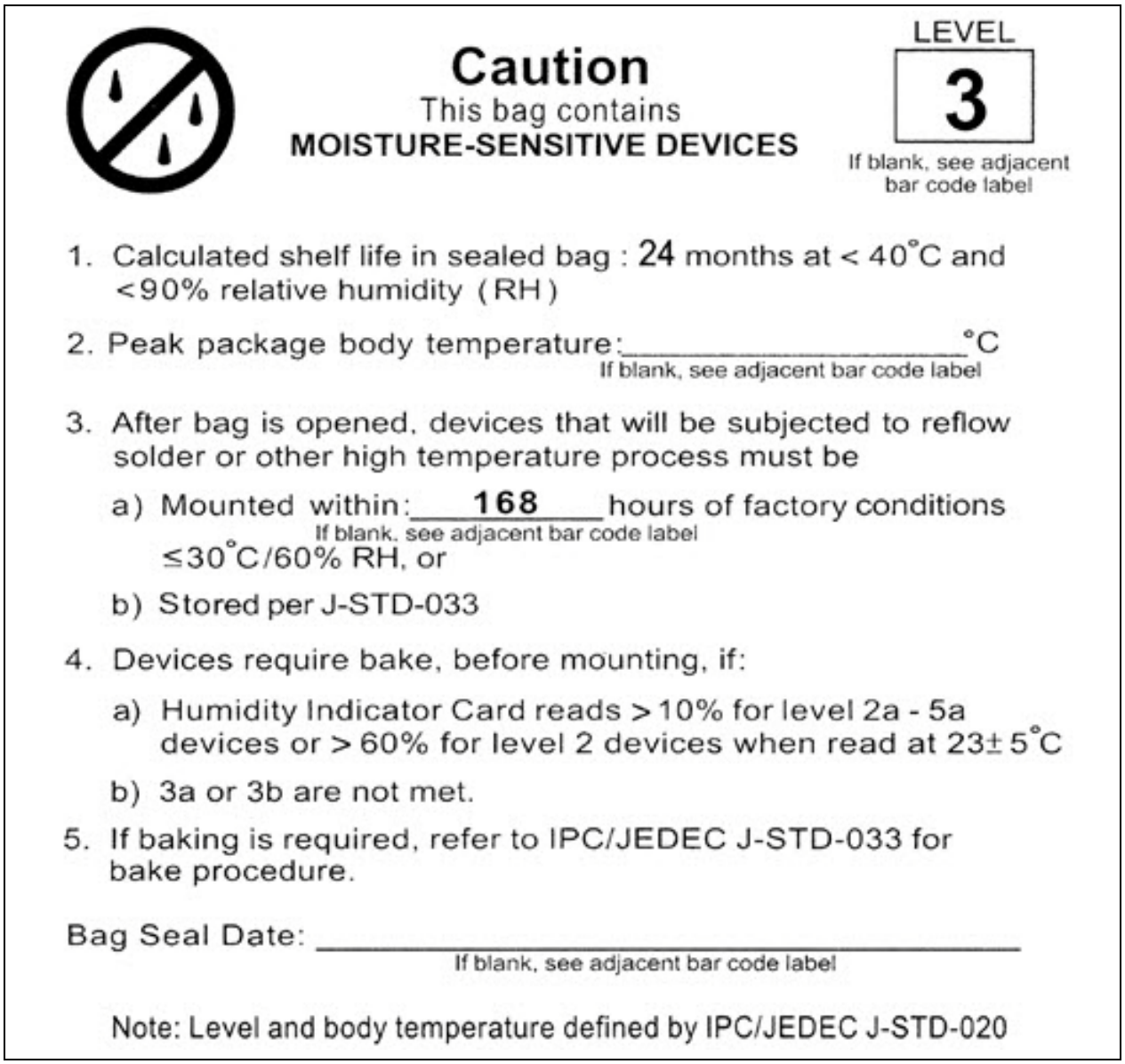
10.3 Storage Condition

Users must follow these specific storage conditions for the IS2062/64 SoC.

- Calculated shelf life in the sealed bag: 24 months at <40 ℃ and <90% Relative Humidity (RH)
- Once the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, that is <30 ℃ /60% RH.

Figure 10-4 shows the IS2062/64 SoC bag labeling details.

FIGURE 10-4: IS2062/64 SoC STORAGE CONDITIONS



NOTES:

11.0 ORDERING INFORMATION

Table 11-1 provides the ordering information of the IS2062/64 SoC.

TABLE 11-1: ORDERING INFORMATION

Device	Bluetooth Version	Package	Part Number
IS2062	Bluetooth 4.2, BDR/EDR/BLE SoC with integrated 2 mic and stereo speaker output	7 x 7 x 0.9 mm, 56LGA package	IS2062GM-012
IS2064	Bluetooth 4.2, BDR/EDR/BLE, with integrated 1 mic and stereo speaker output and I^2S digital interface	8 x 8 x 0.9 mm, 68LGA package	IS2064GM-012

Note: The IS2062/64 SoC can be purchased through a Microchip representative, Go to http://www.microchip.com/ for ordering information.

NOTES:

APPENDIX A: REFERENCE CIRCUIT

Figure A-1 through Figure A-5 illustrate the IS2062 reference schematics for a stereo headset application.

FIGURE A-1: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

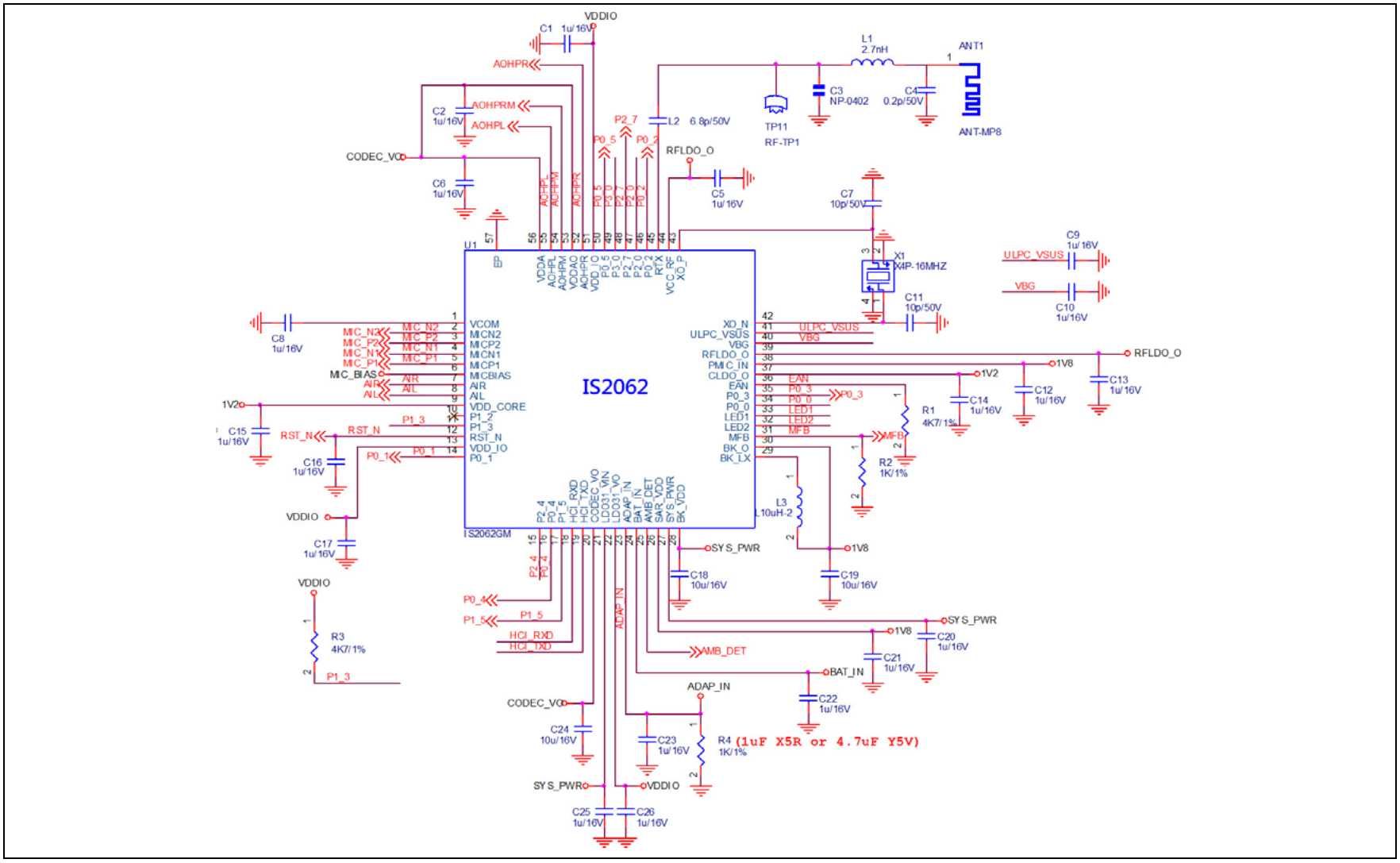
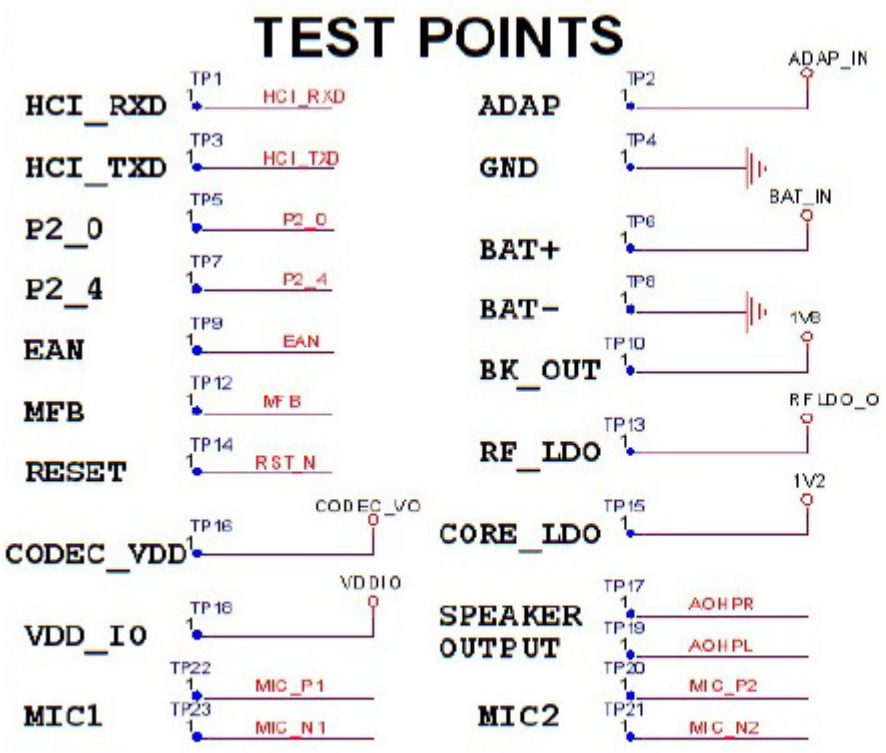


FIGURE A-2: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET



	GPIO Description (General)
P0_0	TX_IND
P0_1	FWD
P0_2	Play/Pause
P0_3	REV
P0_4	NFC
	External Amplifier Enable
P0_5	Volume down
P1_5	SLIDE SWITCH
	External Amplifier Enable
P2_0	System Configuration
P2_4	System Configuration
P2_7	Volume up
P3_0	Line-in detection

FIGURE A-3: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

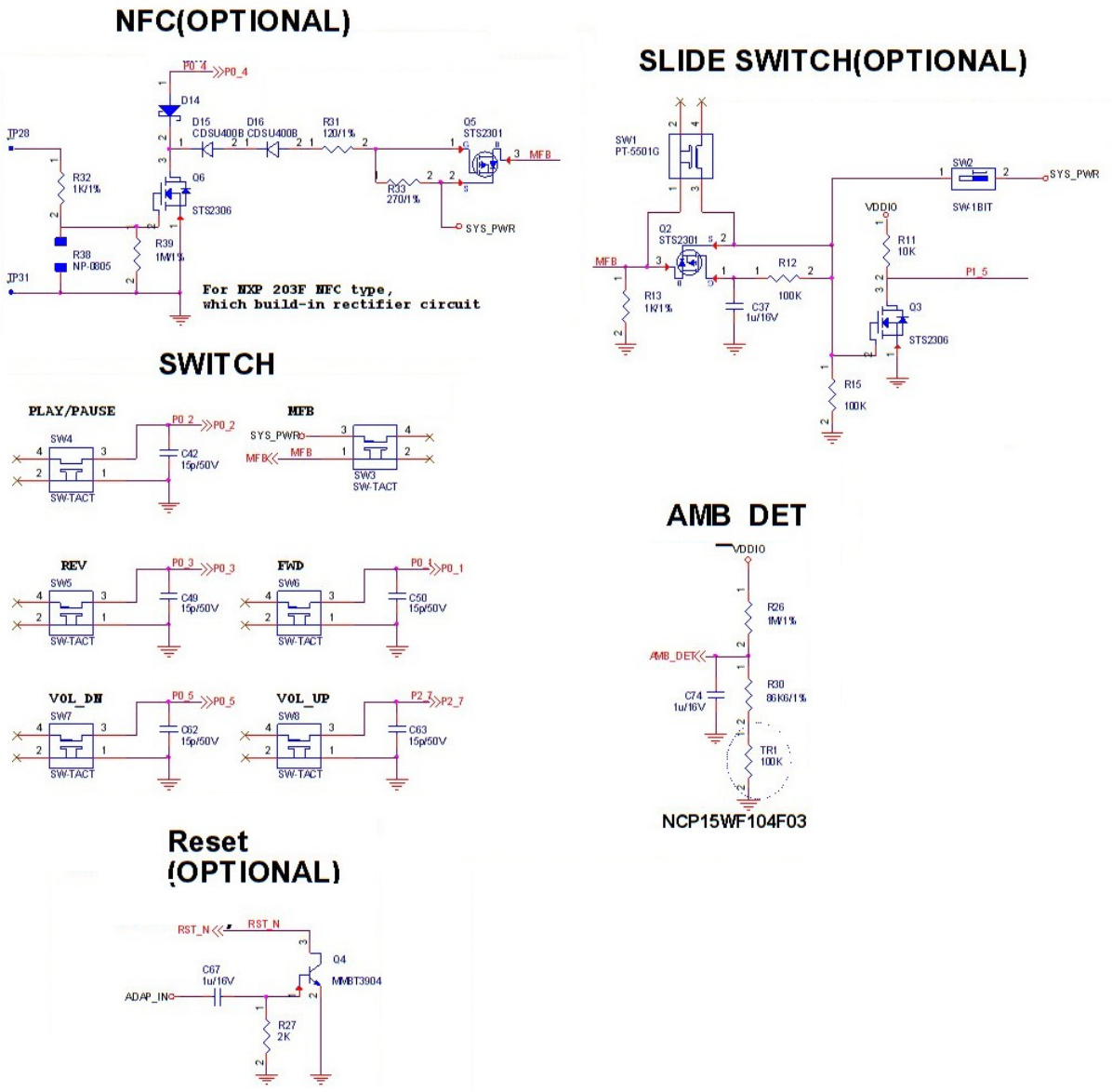


FIGURE A-4: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

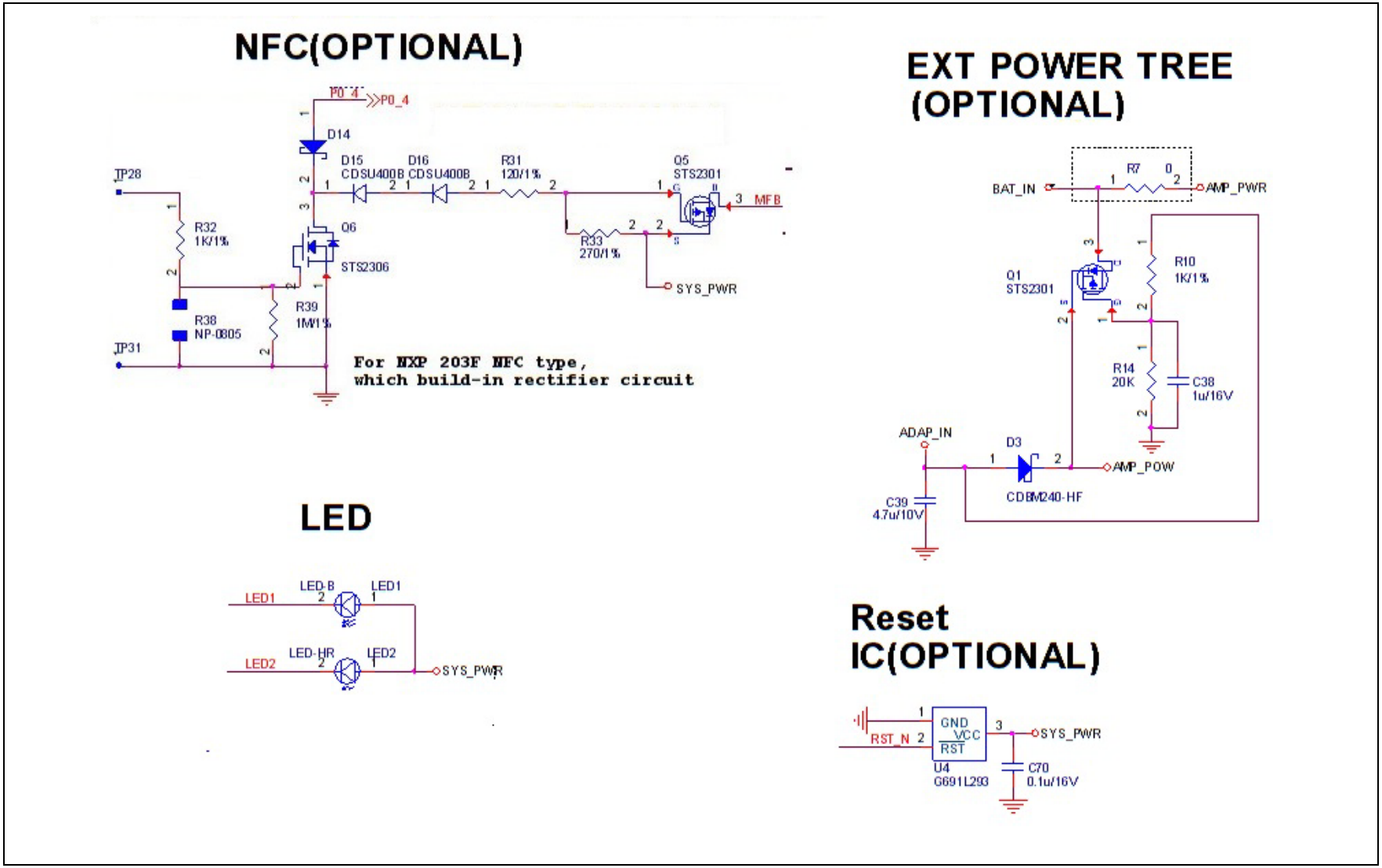
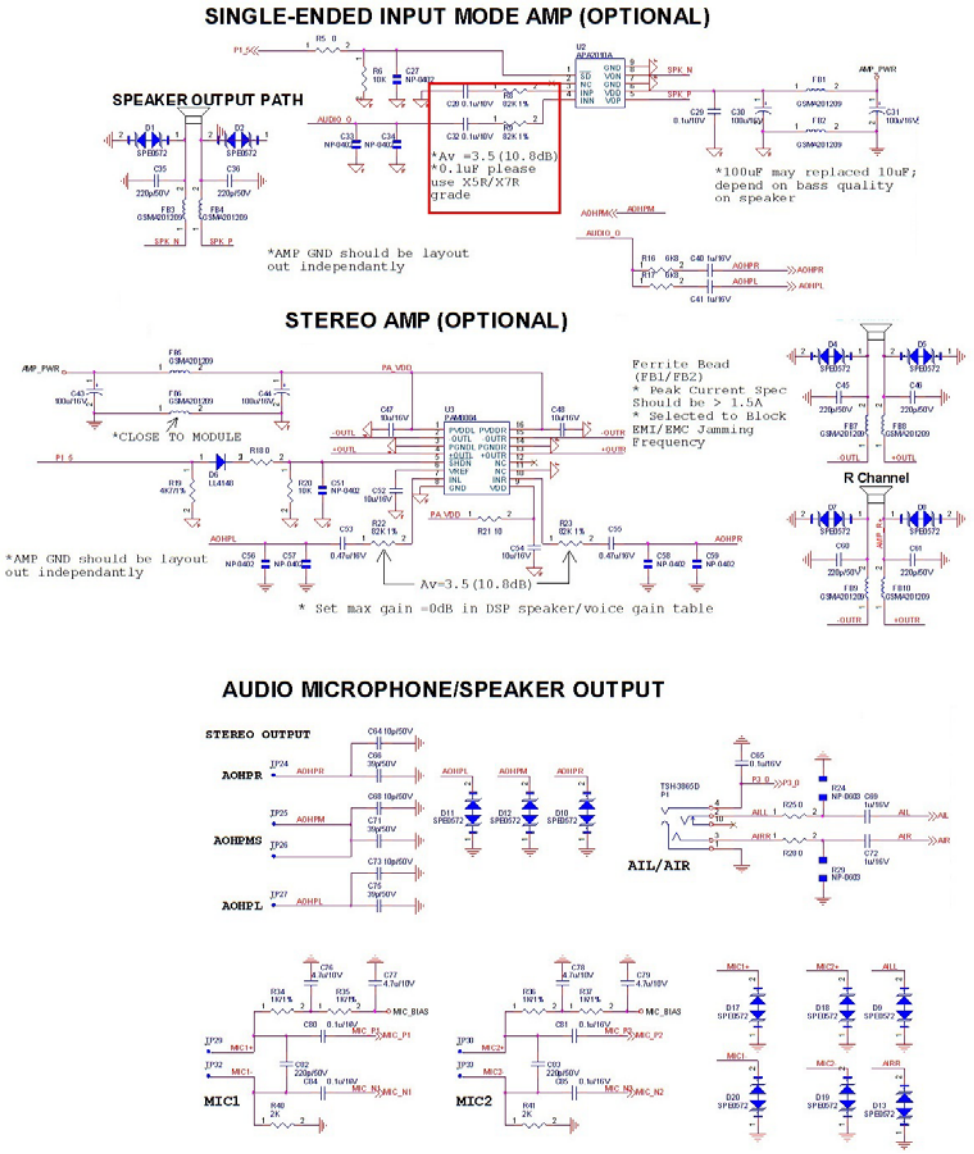


FIGURE A-5: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET



Note: All ESD diodes in this schematics are reserved for testing.

Figure A-6 through Figure A-9 illustrate the IS2064 reference schematic for a stereo headset application.

FIGURE A-6: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET

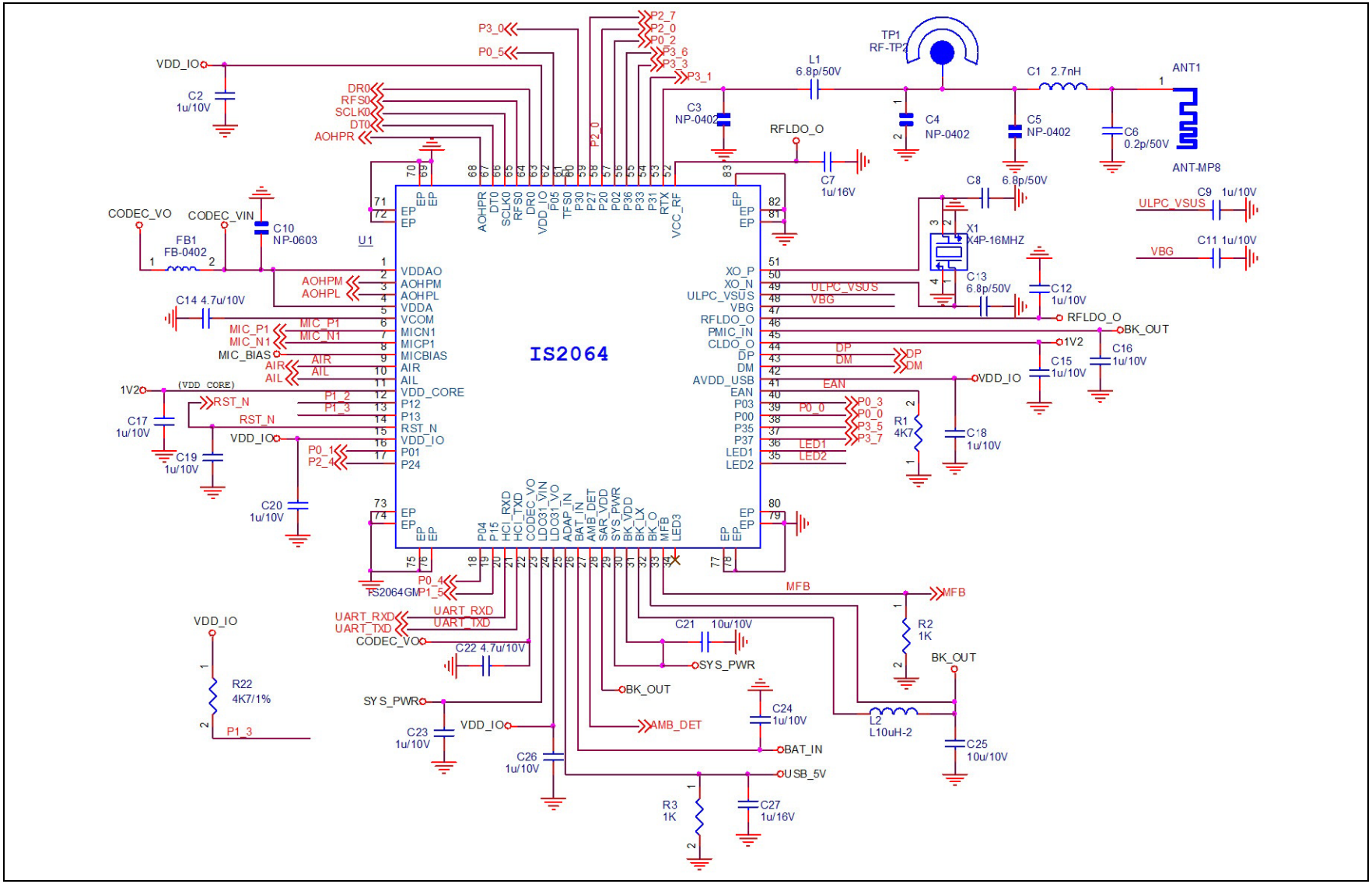
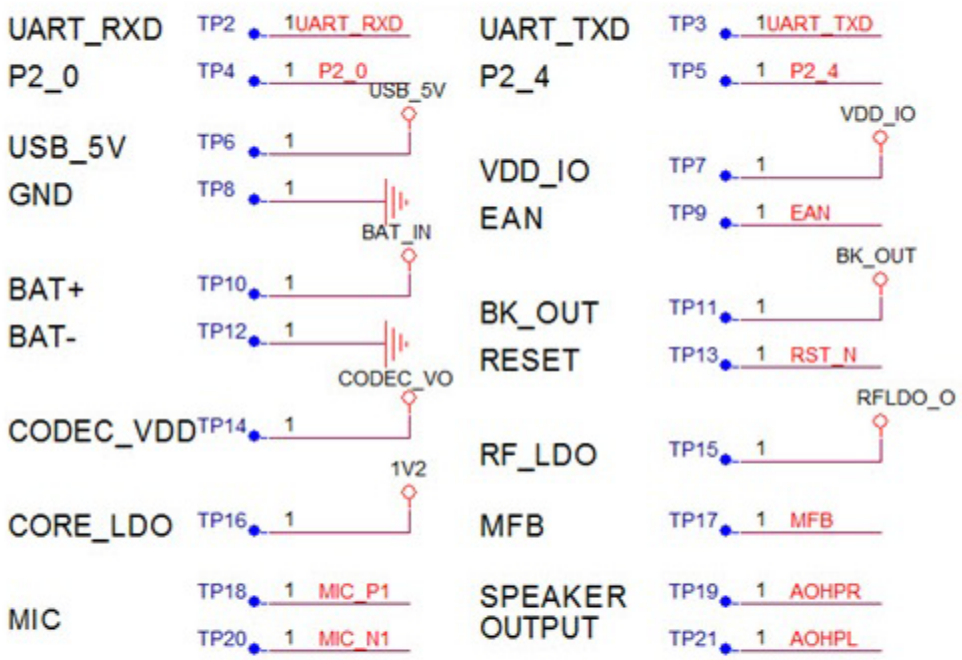


FIGURE A-7: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET



GPIO DESCRIPTION

MFB	UART_RX_IND; MFB
P0_0	SLIDE SWITCH
P0_2	PLAY/PAUSE
P0_4	AMP_EN/NFC
P0_5	VOL-
P2_7	VOL+
P3_0	AUX IN Detection
P3_7	UART_TX_IND
P1_5	AMP_EN/SLIDE SWITCH
	Single/Double setting
P3_6	Single/Double setting
P2_0	System Configuration
EAN	System Configuration

FIGURE A-8: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET

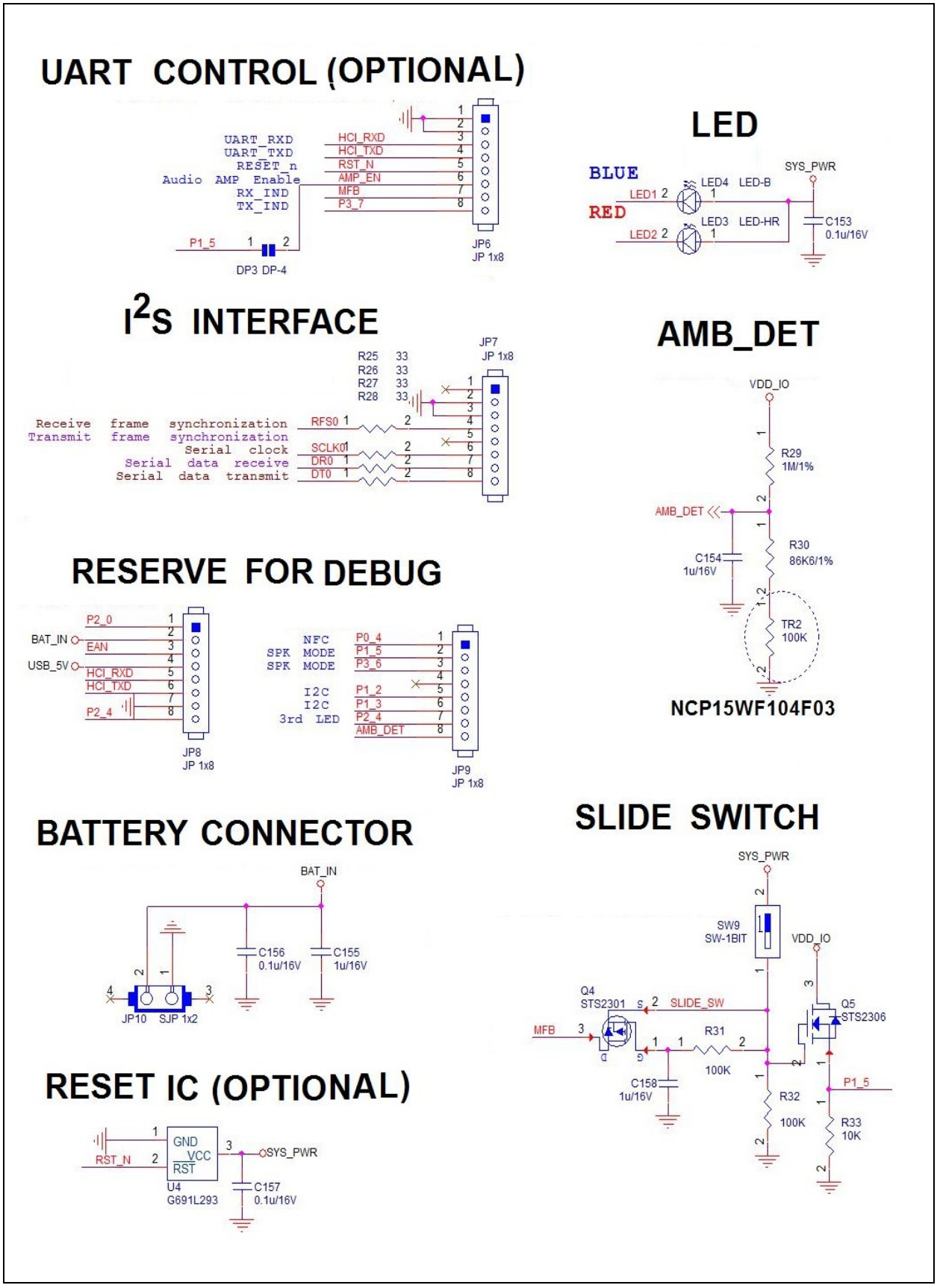
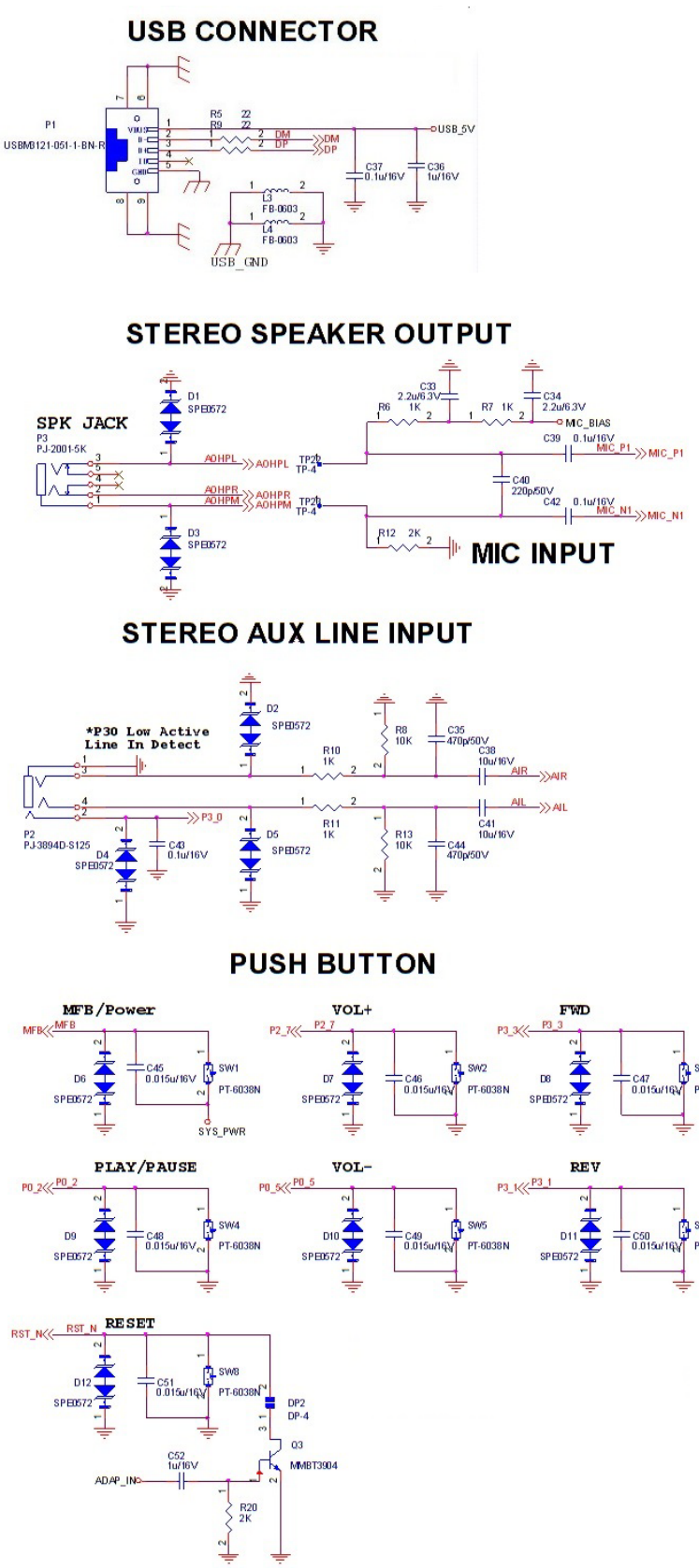


FIGURE A-9: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET



Note: All ESD diodes in this schematics are reserved for testing.

NOTES:

APPENDIX B: REVISION HISTORY

Revision A (May 2016)

This is the initial released version of this document.

NOTES:

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