

# RMLV0414E Series

4Mb Advanced LPSRAM (256-kword × 16-bit)

R10DS0216EJ0100  
Rev.1.00  
2014.2.27

## Description

The RMLV0414E Series is a family of 4-Mbit static RAMs organized 262,144-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0414E Series has realized higher density, higher performance and low power consumption. The RMLV0414E Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44-pin TSOP (II).

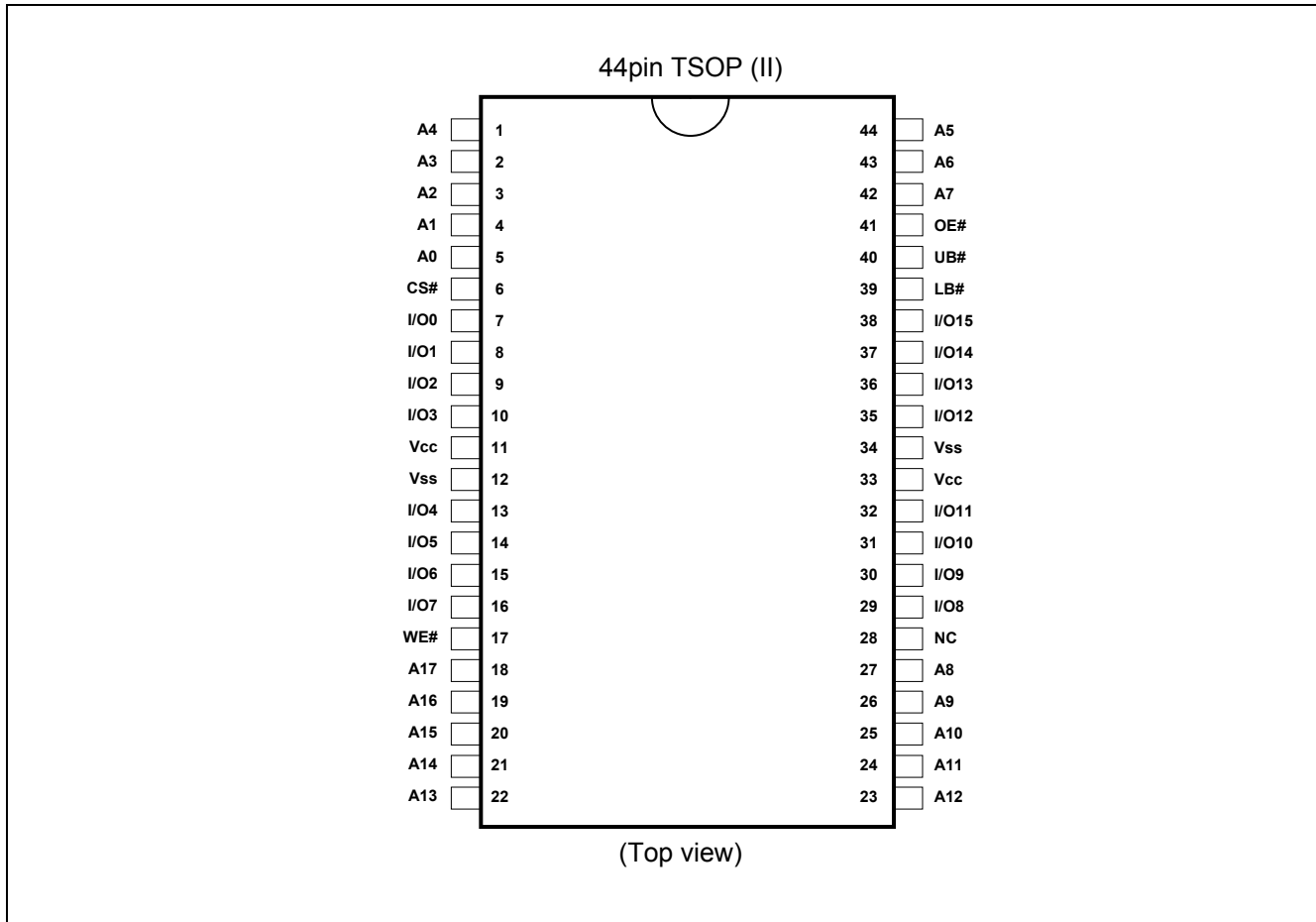
## Features

- Single 3V supply: 2.7V to 3.6V
- Access time: 45ns (max.)
- Current consumption:
  - Standby: 0.4μA (typ.)
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

## Part Name Information

Part name	Access time	Temperature range	Package	Shipping container
RMLV0414EGSB-4S2#AA0	45 ns	-40 ~ +85°C	400-mil 44pin plastic TSOP (II)	Tray Max. 135pcs/Tray Max. 1080pcs/Inner box
RMLV0414EGSB-4S2#HA0				Embossed tape 1000pcs/Reel

## Pin Arrangement



## Pin Description

Pin name	Function
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
NC	No connection



## Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>2</sup> to $V_{CC}+0.3$ <sup>3</sup>	V
Power dissipation	$P_T$	0.7	W
Operation temperature	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-65 to +150	°C
Storage temperature range under bias	$T_{bias}$	-40 to +85	°C

Note 2. -3.0V for pulse  $\leq 30$ ns (full width at half maximum)

3. Maximum voltage is +4.6V.

## DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC}+0.3$	V	
Input low voltage	$V_{IL}$	-0.3	—	0.6	V	4
Ambient temperature range	$T_a$	-40	—	+85	°C	

Note 4. -3.0V for pulse  $\leq 30$ ns (full width at half maximum)

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	$\mu A$	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu A$	$CS\# = V_{IH} \text{ or } OE\# = V_{IH} \text{ or } WE\# = V_{IL}$ or $LB\# = UB\# = V_{IH}$ , $V_{I/O} = V_{SS} \text{ to } V_{CC}$
Operating current	$I_{CC}$	—	—	10	mA	$CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0$ mA
Average operating current	$I_{CC1}$	—	—	20	mA	Cycle = 55ns, duty = 100%, $I_{I/O} = 0$ mA, $CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$
		—	—	25	mA	Cycle = 45ns, duty = 100%, $I_{I/O} = 0$ mA, $CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$
	$I_{CC2}$	—	—	2.5	mA	Cycle = 1 $\mu s$ , duty = 100%, $I_{I/O} = 0$ mA $CS\# \leq 0.2V$ , $V_{IH} \geq V_{CC}-0.2V$ , $V_{IL} \leq 0.2V$
Standby current	$I_{SB}$	—	0.1 <sup>5</sup>	0.3	mA	$CS\# = V_{IH}$ , Others = $V_{SS} \text{ to } V_{CC}$
Standby current	$I_{SB1}$	—	0.4 <sup>5</sup>	2	$\mu A$	$\sim +25^\circ C$
		—	—	3	$\mu A$	$\sim +40^\circ C$
		—	—	5	$\mu A$	$\sim +70^\circ C$
		—	—	7	$\mu A$	$\sim +85^\circ C$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1$ mA
	$V_{OH2}$	$V_{CC}-0.2$	—	—	V	$I_{OH} = -0.1$ mA
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2$ mA
	$V_{OL2}$	—	—	0.2	V	$I_{OL} = 0.1$ mA

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V ( $T_a = 25^\circ C$ ), and not 100% tested.

## Capacitance

( $V_{CC} = 2.7V \sim 3.6V$ ,  $f = 1$ MHz,  $T_a = -40 \sim +85^\circ C$ )

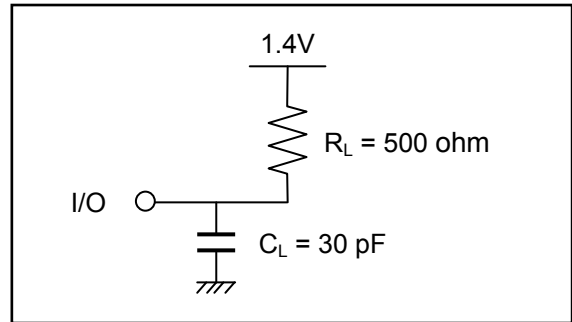
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0V$	6
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0V$	6

Note 6. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions ( $V_{CC} = 2.7V \sim 3.6V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

- Input pulse levels:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



### Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	$t_{RC}$	45	—	ns	
Address access time	$t_{AA}$	—	45	ns	
Chip select access time	$t_{ACS}$	—	45	ns	
Output enable to output valid	$t_{OE}$	—	22	ns	
Output hold from address change	$t_{OH}$	10	—	ns	
LB#, UB# access time	$t_{BA}$	—	45	ns	
Chip select to output in low-Z	$t_{CLZ}$	10	—	ns	7,8
LB#, UB# enable to low-Z	$t_{BLZ}$	5	—	ns	7,8
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	7,8
Chip deselect to output in high-Z	$t_{CHZ}$	0	18	ns	7,8,9
LB#, UB# disable to high-Z	$t_{BHZ}$	0	18	ns	7,8,9
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	7,8,9

Note 7. This parameter is sampled and not 100% tested.

8. At any given temperature and voltage condition,  $t_{CHZ}$  max is less than  $t_{CLZ}$  min,  $t_{BHZ}$  max is less than  $t_{BLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

9.  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

## Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	$t_{WC}$	45	—	ns	
Address valid to write end	$t_{AW}$	35	—	ns	
Chip select to write end	$t_{CW}$	35	—	ns	
Write pulse width	$t_{WP}$	35	—	ns	10
LB#,UB# valid to write end	$t_{BW}$	35	—	ns	
Address setup time to write start	$t_{AS}$	0	—	ns	
Write recovery time from write end	$t_{WR}$	0	—	ns	
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write end	$t_{DH}$	0	—	ns	
Output enable from write end	$t_{OW}$	5	—	ns	11
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	11,12
Write to output in high-Z	$t_{WHZ}$	0	18	ns	11,12

Note 10.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

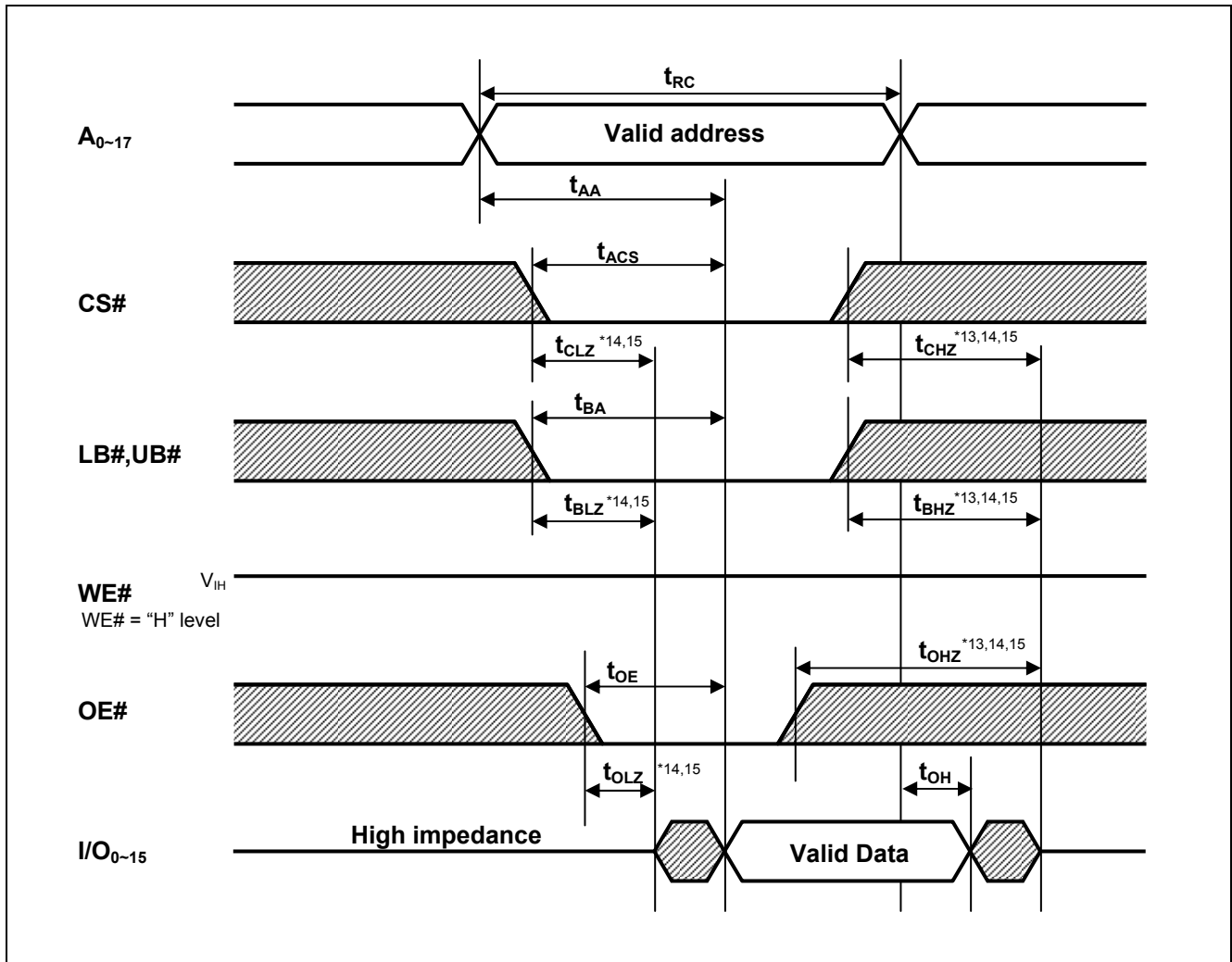
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

11. This parameter is sampled and not 100% tested.

12.  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

## Timing Waveforms

## Read Cycle

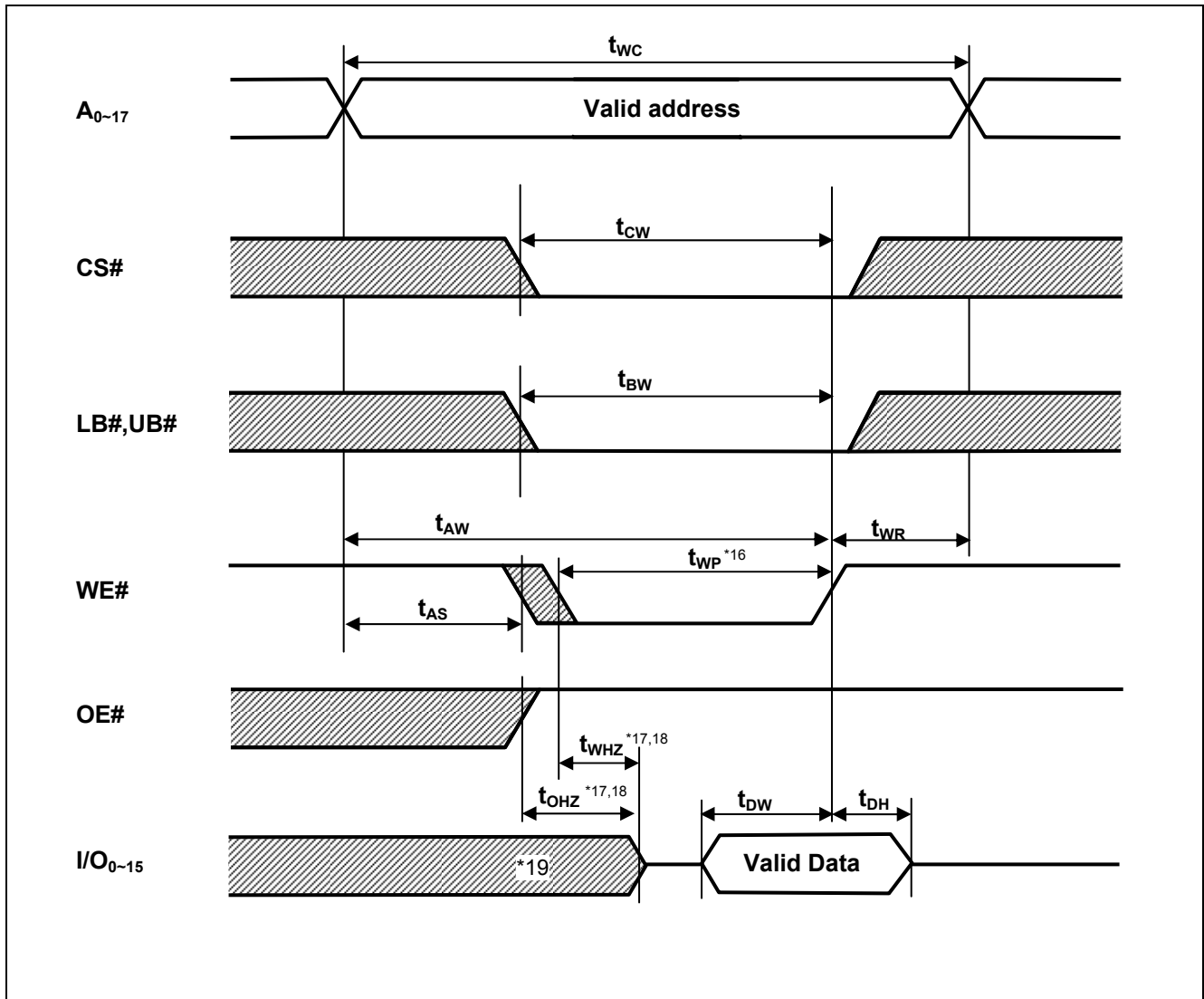


Note 13.  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

14. This parameter is sampled and not 100% tested.

15. At any given temperature and voltage condition,  $t_{CHZ}$  max is less than  $t_{CLZ}$  min,  $t_{BHZ}$  max is less than  $t_{BLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

## Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 16.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

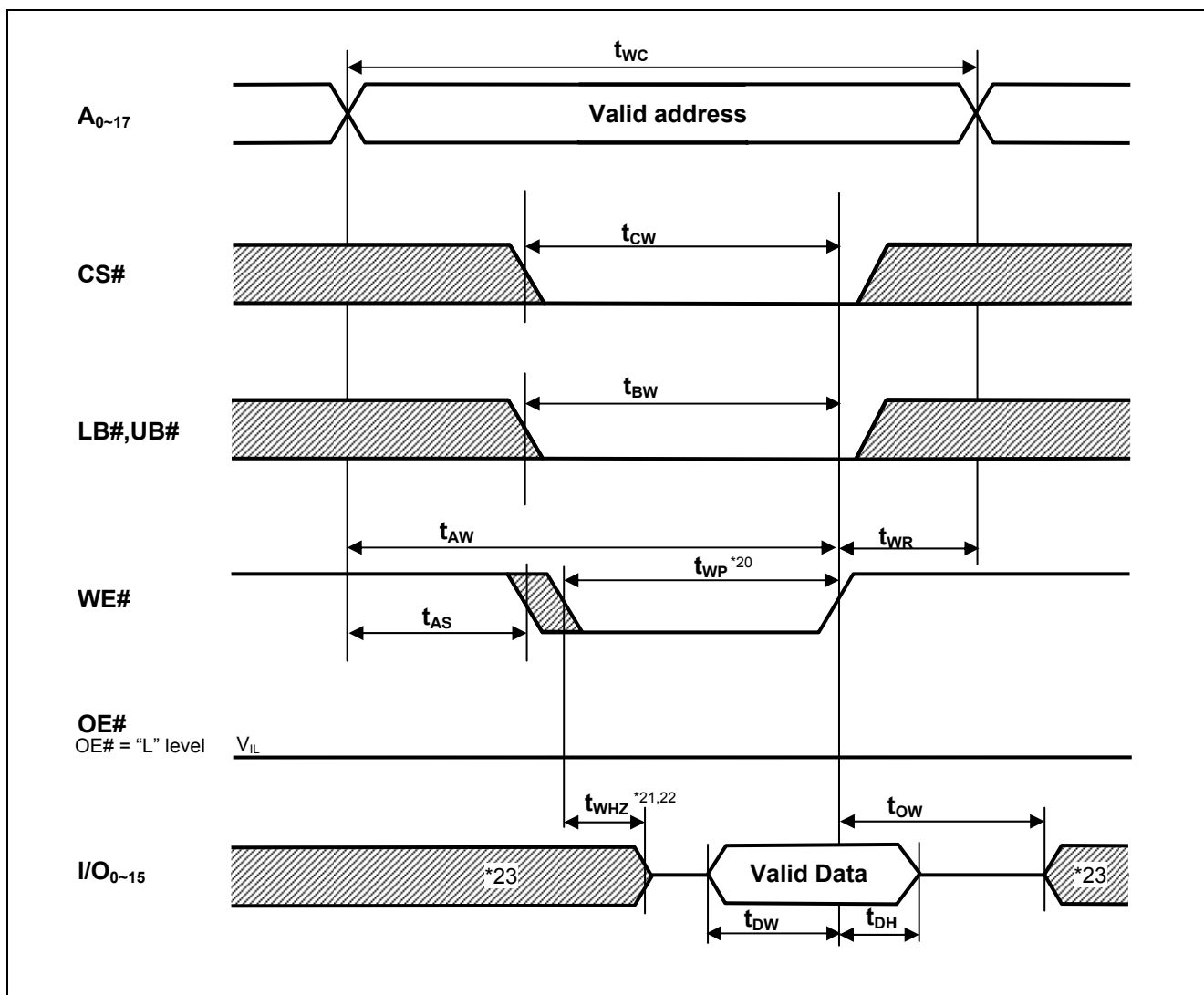
17.  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

18. This parameter is sampled and not 100% tested.

19. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.



## Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 20.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

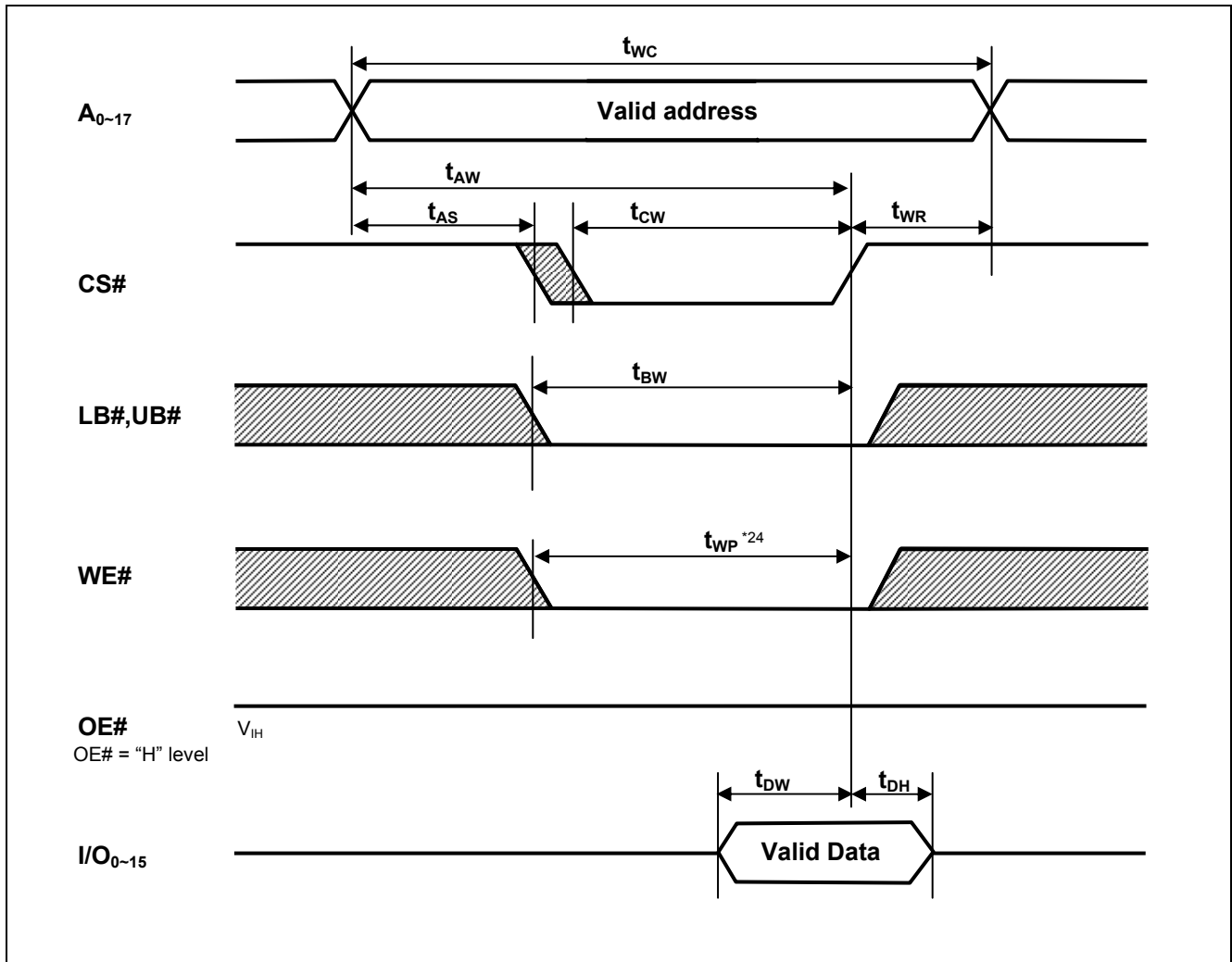
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

21.  $t_{WHZ}$  is defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

22. This parameter is sampled and not 100% tested.

23. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

## Write Cycle (3) (CS# CLOCK)



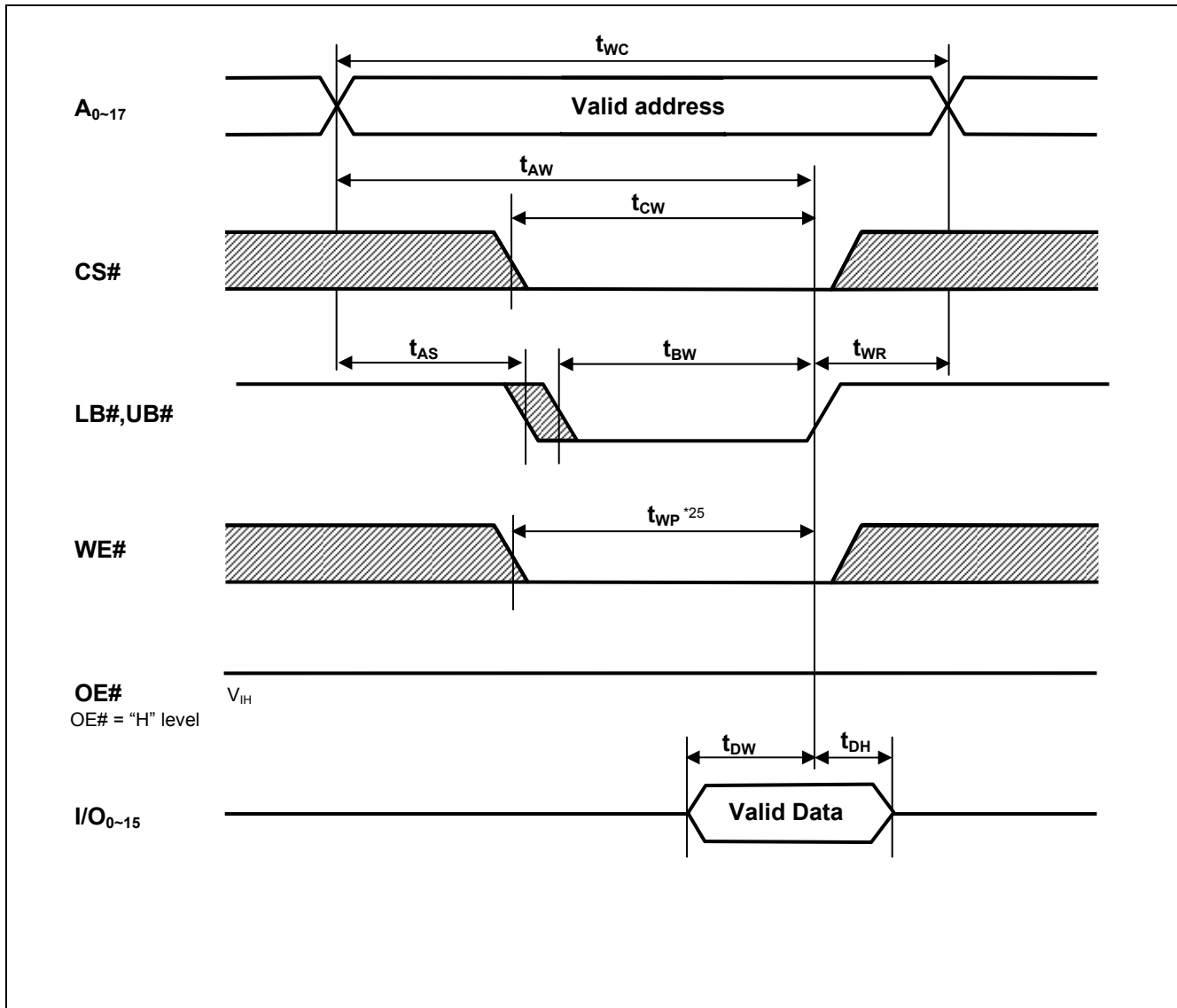
Note 24.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

## Write Cycle (4) (LB#,UB# CLOCK)



Note 25.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

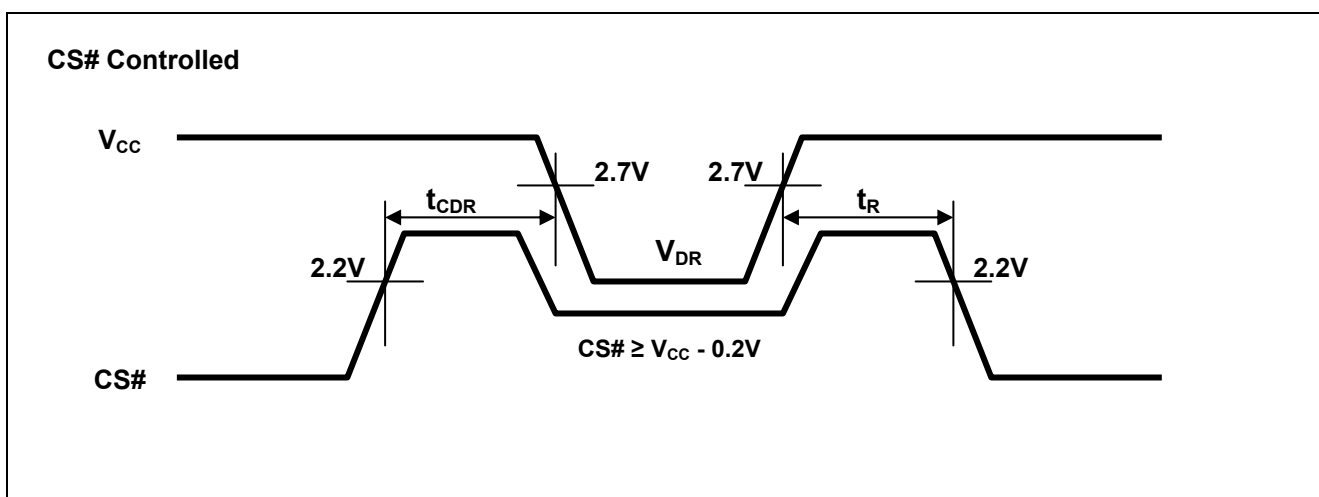
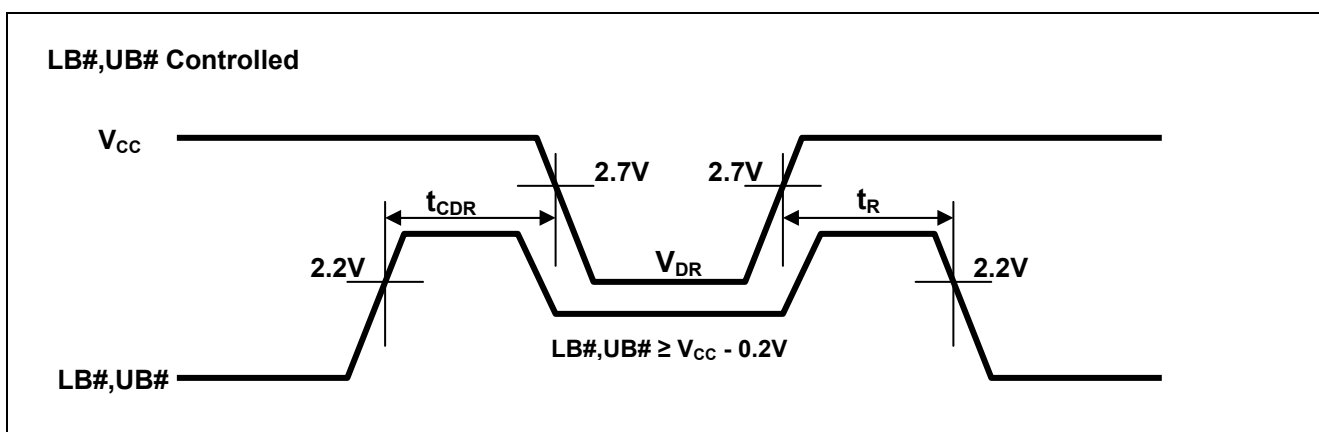
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low  $V_{CC}$  Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>*27</sup>	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	1.5	—	—	V	Vin ≥ 0V, (1) CS# ≥ V <sub>CC</sub> -0.2V or (2) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS# ≤ 0.2V	
Data retention current	I <sub>CCDR</sub>	—	0.4 <sup>*26</sup>	2	μA	~+25°C	V <sub>CC</sub> =3.0V, Vin ≥ 0V, (1) CS# ≥ V <sub>CC</sub> -0.2V or (2) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS# ≤ 0.2V
		—	—	3	μA	~+40°C	
		—	—	5	μA	~+70°C	
		—	—	7	μA	~+85°C	
Chip deselect time to data retention	t <sub>CDR</sub>	0	—	—	ns	See retention waveform.	
Operation recovery time	t <sub>R</sub>	5	—	—	ms		

Note 26. Typical parameter indicates the value for the center of distribution at 3.0V ( $T_a=25^{\circ}C$ ), and not 100% tested.

27.  $CS\#$  controls address buffer,  $WE\#$  buffer,  $OE\#$  buffer,  $LB\#$  buffer,  $UB\#$  buffer and I/O buffer. If  $CS\#$  controls data retention mode,  $V_{in}$  levels (address,  $WE\#$ ,  $OE\#$ ,  $LB\#$ ,  $UB\#$ , I/O) can be in the high-impedance state.

Low  $V_{CC}$  Data Retention Timing Waveforms ( $CS\#$  controlled)Low  $V_{CC}$  Data Retention Timing Waveforms ( $LB\#, UB\#$  controlled)

Revision History	RMLV0414E Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2014.2.27	—	First edition issued

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