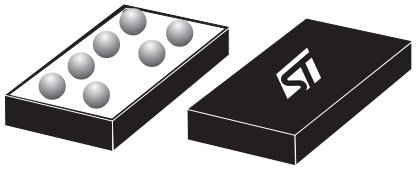
STG4159

Low-voltage 0.3 Ω max. single SPDT switch with break-before-make feature and 10 kV contact ESD protection

Datasheet – production data

Features

- Wide operating voltage range:
  V_{CC} (opr.) = 1.65 to 4.8 V
- Low power dissipation:
  I_{CC} = 0.2 µA (max.) at T_A = 85 °C
- Low on-resistance V_{IN} = 0 V:
  - R_{ON} = 0.40 Ω (max. T_A = 25 °C) at V_{CC} = 2.25 V
  - R_{ON} = 0.35 Ω (max. T_A = 25 °C) at V_{CC} = 3.0 V
  - R_{ON} = 0.30 Ω (max. T_A = 25 °C) at V_{CC} = 4.3 V
- Separate supply voltage for switch and control pin
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD performance tested on common channel (D pin)
  - 10 kV IEC-61000-4-2 ESD, contact discharge
  - 15 kV IEC-61000-4-2 ESD, air discharge
- ESD performance test on all other pins
  - 10 kV IEC-61000-4-2 ESD, contact discharge
  - 500 V machine model (JESD22 A115-A)
  - 1500 V charged-device model (JESD22 C101)



Flip Chip 7

Description

The STG4159 device is a high-speed CMOS low-voltage single-analog SPDT (single-pole dual-throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65 to 4.8 V, making this device ideal for portable applications. It offers low on-resistance (0.30 Ω) at V_{CC} = 4.3 V. The SEL inputs are provided to control the switches.

The switch S1 is ON (connected to common port D) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common port D) when the SEL input is held low and OFF (high impedance state exists between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra low-power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
STG4159BJR	Flip Chip 7	Tape and reel

Contents

1 Logic diagram

Figure 1. Functional diagram

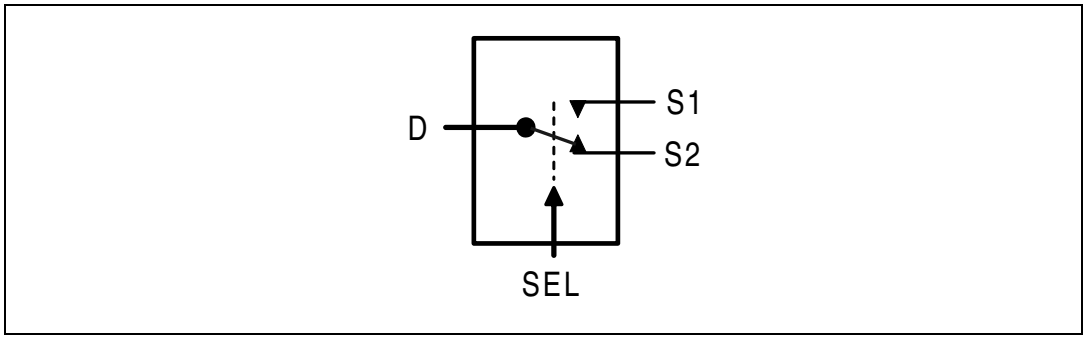


Figure 2. Input equivalent circuit

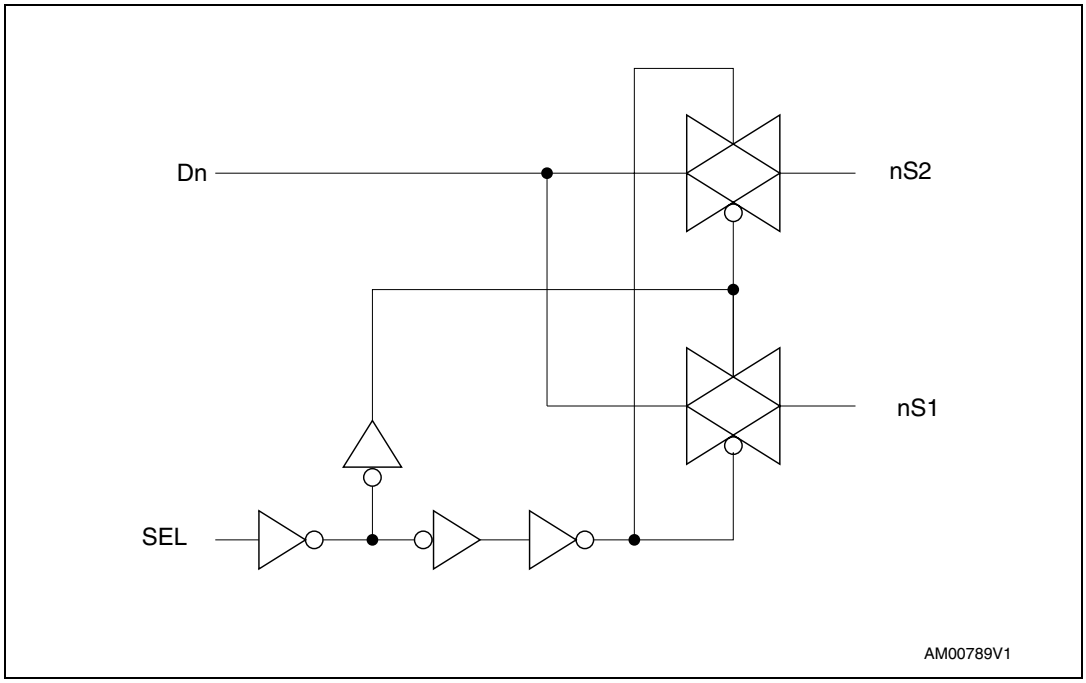


Table 2. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF(1)
L	OFF(1)	ON

1. High impedance.

Figure 3. Pin connections

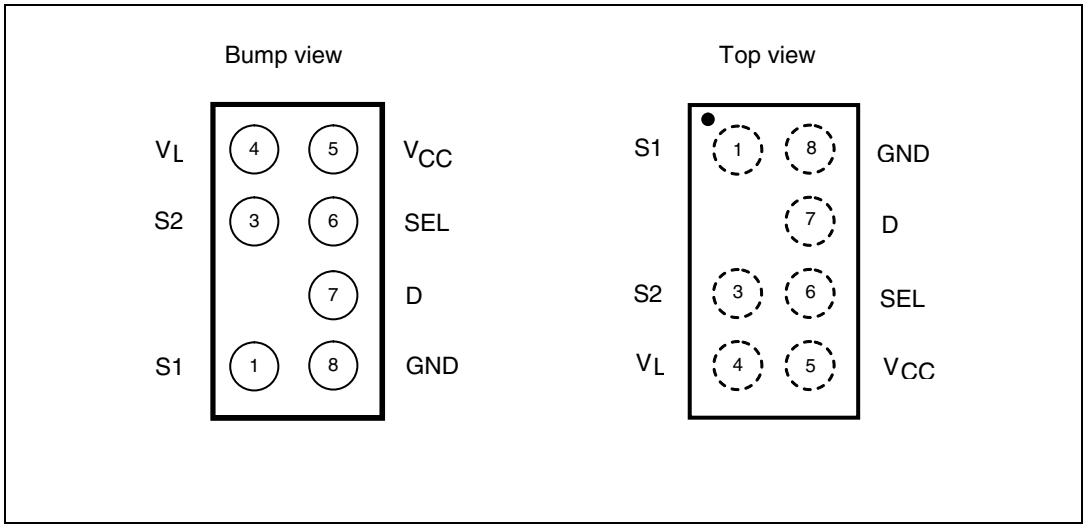


Table 3. Pin assignment

Pin number	Symbol	Name and function
1	S1	Independent channels
3	S2	Independent channels
4	V_L	Logic supply voltage
5	V_{CC}	Positive supply voltage
6	SEL	Control
7	D	Common channel
8	GND	Ground (0 V)

2 Maximum rating

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_L	Logic supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to V_L + 0.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL} < 0 V)	-50	mA
I_{IK}	DC input diode current (V_{SEL} < 0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C(1)	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec.)	260	°C

1. Derate above 70 °C by 18.5 mW/C.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.8	V
V_L	Logic supply voltage(1)		1.65 to V_{CC}	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to V_L	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_L = 1.65 to 2.7 V	0 to 20	ns/V
		V_L = 3.0 to 4.8 V	0 to 10	

1. V_L pin should not be left floating.

3 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High level input voltage	1.65 - 4.3	1.65 - 1.95		1.25	–	–	1.25	–	V
			2.3 - 2.7		1.75	–	–	1.75	–	
			3.0 - 3.6		2.35	–	–	2.35	–	
			4.3		2.8	–	–	2.8	–	
V_{IL}	Low level input voltage	1.65 - 4.3	1.65 - 1.95		–	–	0.6	–	0.6	V
			2.3 - 2.7		–	–	0.8	–	0.8	
			3.0 - 3.6		–	–	1.05	–	1.05	
			4.3		–	–	1.5	–	1.5	
R_{ON}	On-resistance	1.8	1.65 - 4.3	V_S = 0 V to V_{CC} I_S = 100 mA	–	0.49	0.65	–	0.85	Ω
		2.25			–	0.30	0.40	–	0.50	
		3			–	0.25	0.35	–	0.45	
		3.7			–	0.22	0.32	–	0.42	
		4.3			–	0.21	0.30	–	0.40	
ΔR_{ON}	On-resistance match between channels(1)	1.8	1.65 - 4.3	V_S = 0 V to V_{CC} I_S = 100 mA	–	5	–	–	–	mΩ
		2.25			–	3	–	–	–	
		3			–	3	–	–	–	
		3.7			–	3	–	–	–	
		4.3			–	3	–	–	–	
R_{FLAT}	On-resistance flatness(2)	1.8	1.65 - 4.3	V_S = 0 V to V_{CC} I_S = 100 mA	–	300	400	–	450	mΩ
		2.5			–	130	170	–	230	
		3			–	90	120	–	170	
		3.7			–	90	120	–	170	
		4.3			–	90	120	–	170	
I_{OFF}	Sn OFF state leakage current	1.65 - 4.3	1.65 - 4.3	V_S = 0.3 to 4.0 V_D = 0.3 to 4.0	-30	–	30	-300	300	nA

Table 6. DC specifications (continued)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
I_{ON}	Sn ON state leakage current	1.65 - 4.3	1.65 - 4.3	V_S = 0.3 to 4.0 V_D = open	-20	—	20	-100	100	nA
I_D	D ON state leakage current	1.65 - 4.3	1.65 - 4.3	V_S = open V_D = 0.3 to 4.0	-20	—	20	-100	100	nA
I_{CC}	Quiescent supply current	1.65 - 4.3	1.65 - 4.3	V_{SEL} = V_{CC} or GND	-0.05	—	0.05	-0.2	0.2	µA
I_{SEL}	SEL leakage current	1.65 - 4.3	1.65 - 4.3	V_{SEL} = 4.3 V or GND	-0.1	—	0.1	-1	1	µA

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$5 ns)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation delay	1.65 - 1.95	1.65 - 4.3		—	0.13	—	—	—	ns
		2.3 - 2.7			—	0.15	—	—	—	
		3.0 - 3.3			—	0.16	—	—	—	
		3.6 - 4.3			—	0.16	—	—	—	
t_{ON}	Turn-on time	1.65 - 1.95	1.65 - 4.3	V_S = V_{CC} R_L = 50 Ω C_L = 30 pF	—	95	123	—	160	ns
		2.3 - 2.7			—	48	62	—	80	
		3 - 3.6			—	33	43	—	56	
		4.3			—	29	38	—	49	
t_{OFF}	Turn-off time	1.65 - 1.95	1.65 - 4.3	V_S = V_{CC} R_L = 50 Ω C_L = 30 pF	—	12	15	—	20	ns
		2.3 - 2.7			—	12	16	—	21	
		3 - 3.6			—	13	17	—	22	
		4.3			—	13	17	—	22	
t_D	Break-before-make time delay	1.65 - 1.95	1.65 - 4.3	C_L = 35 pF R_L = 50 Ω V_S = V_{CC}/2	10	42	—	—	—	ns
		2.3 - 2.7			10	22	—	—	—	
		3 - 3.6			5	15	—	—	—	
		4.3			5	12	—	—	—	

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤5 ns) (continued)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
Q	Charge injection	1.65 - 1.95	1.65 - 4.3	C_L = 1 nF V_{GEN} = 0 V	–	83	–	–	–	pC
		2.3 - 2.7			–	98	–	–	–	
		3.0 - 3.3			–	114	–	–	–	
		3.6 - 4.3			–	140	–	–	–	

Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
OIRR	OFF-isolation(1)	1.65 - 4.3	4.3	V_S = 1 V_{RMS} f = 100 kHz	–	-69	–	–	–	dB
Xtalk	Crosstalk	1.65 - 4.3	4.3	V_S = 1 V_{RMS} f = 100 kHz	–	-69	–	–	–	dB
THD	Total harmonic distortion	2.3 - 4.3	4.3	R_L = 600 Ω C_L = 50 pF V_S = V_{CC} V_{PP} f = 600 Hz to 20 kHz	–	0.01	–	–	–	%
BW	-3 dB bandwidth (switch ON)	1.65 - 4.3	4.3	R_L = 50 Ω	–	28	–	–	–	MHz
C_{SEL}	Control pin input capacitance	1.8 - 4.3	1.8 - 4.3	V_L = V_{CC}	–	30	–	–	–	pF
C_{Sn}	Sn port capacitance	1.8 - 4.3	1.8 - 4.3	V_L = V_{CC}	–	94	–	–	–	
C_D	D port capacitance when switch is enabled	1.8 - 4.3	1.8 - 4.3	V_L = V_{CC}	–	227	–	–	–	

1. OFF-isolation = 20 $\log_{10}$ (V_D/V_S), V_D = output, V_S = input to off switch.

4 Test circuits

Figure 4. On-resistance

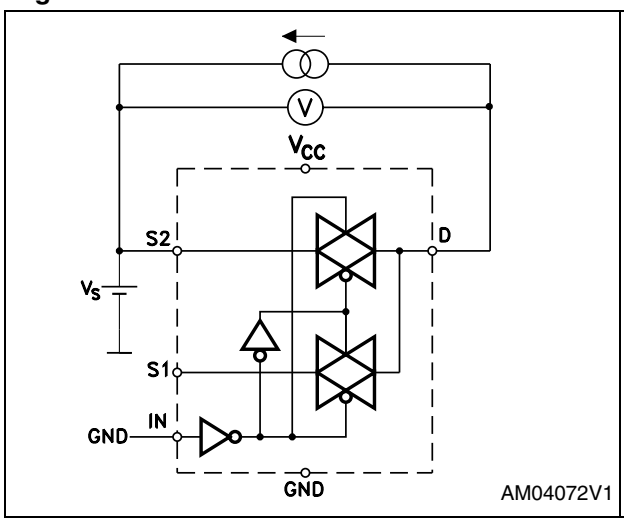


Figure 5. Bandwidth

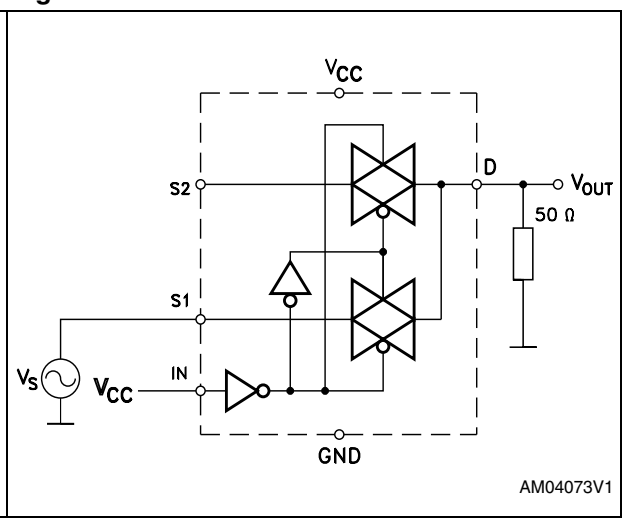


Figure 6. OFF leakage

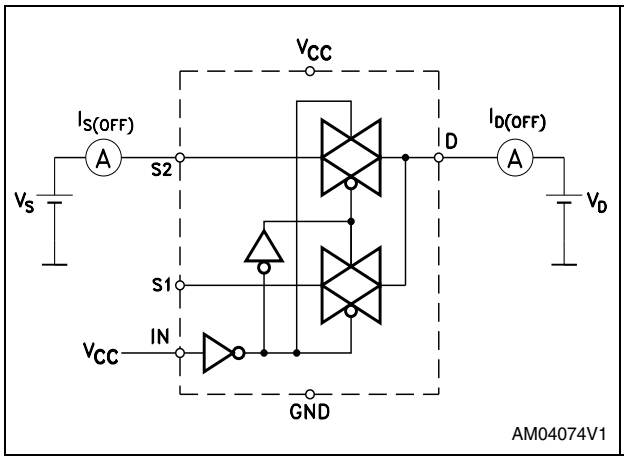


Figure 7. Channel-to-channel crosstalk

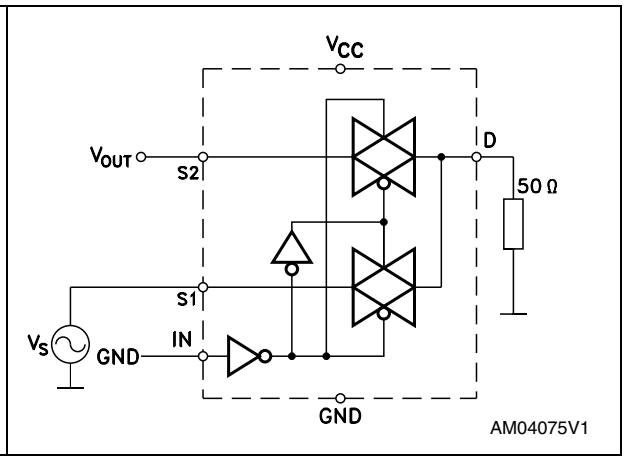


Figure 8. OFF-isolation

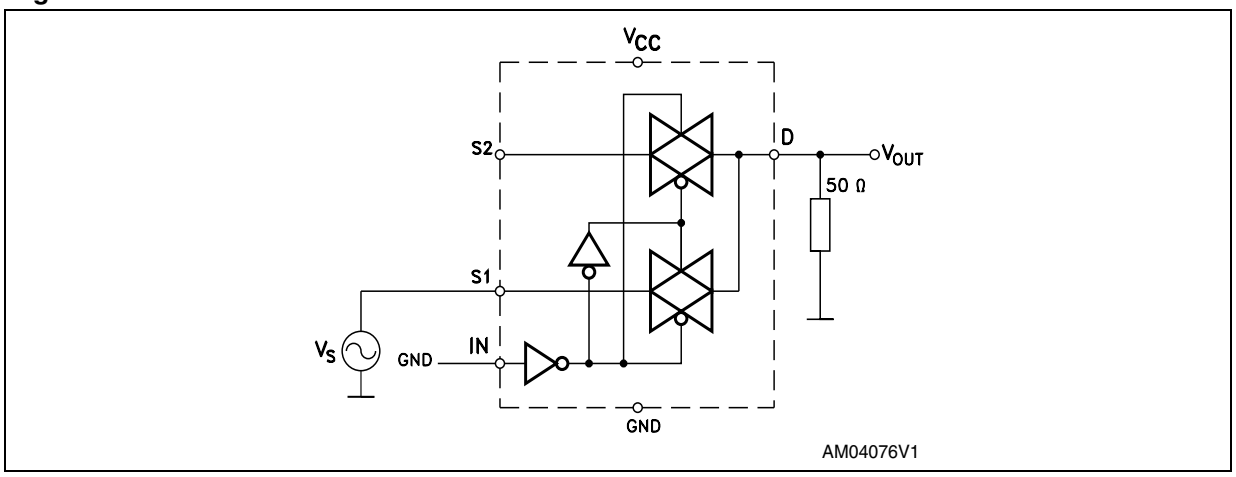
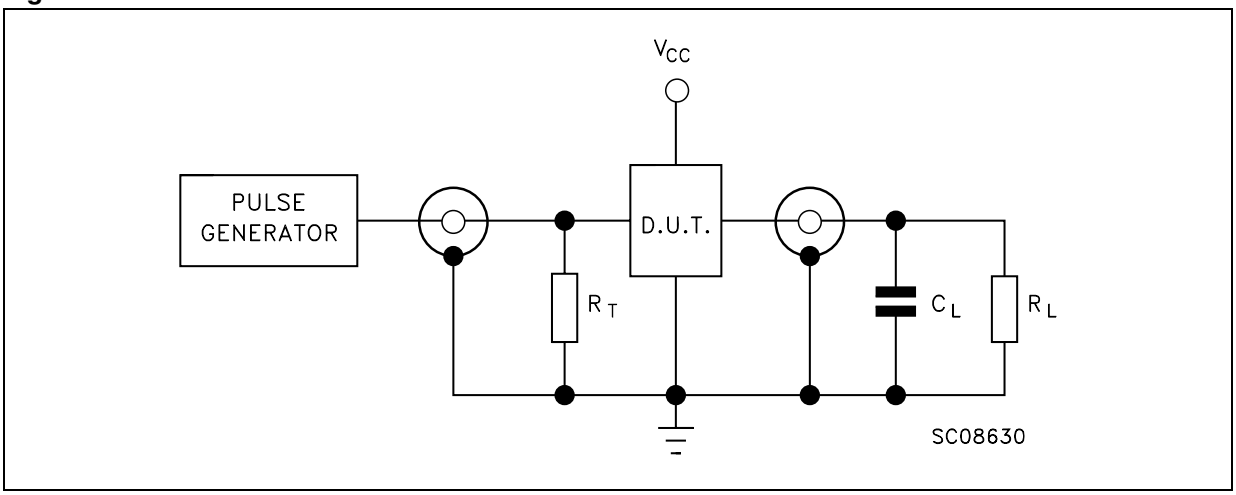
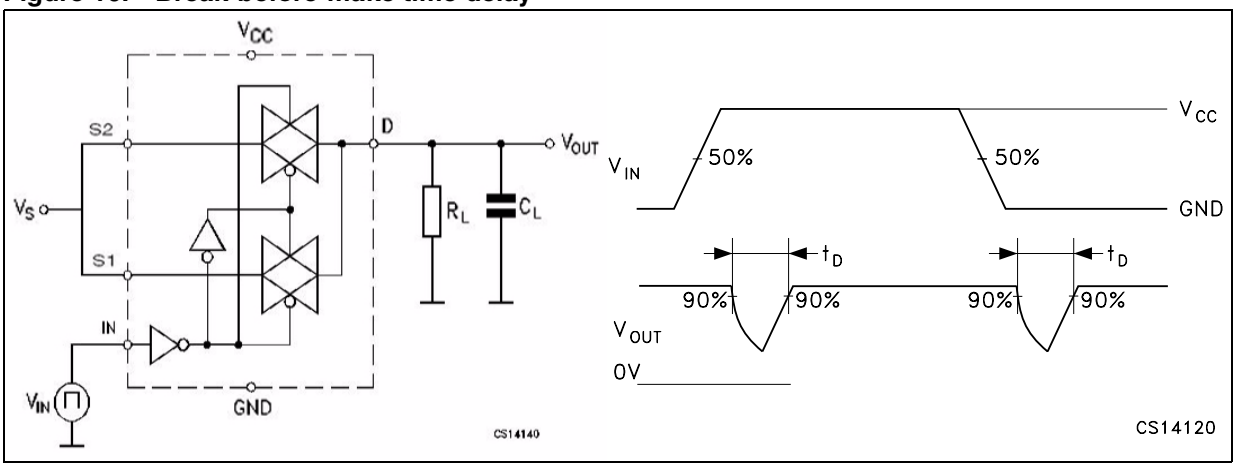


Figure 9. Test circuit



1. C_L = 5/35 pF or equivalent: (includes jig capacitance).
2. R_L = 50 Ω or equivalent.
3. $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

Figure 10. Break-before-make time delay



1. V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF.

Figure 11. Switching time and charge injection

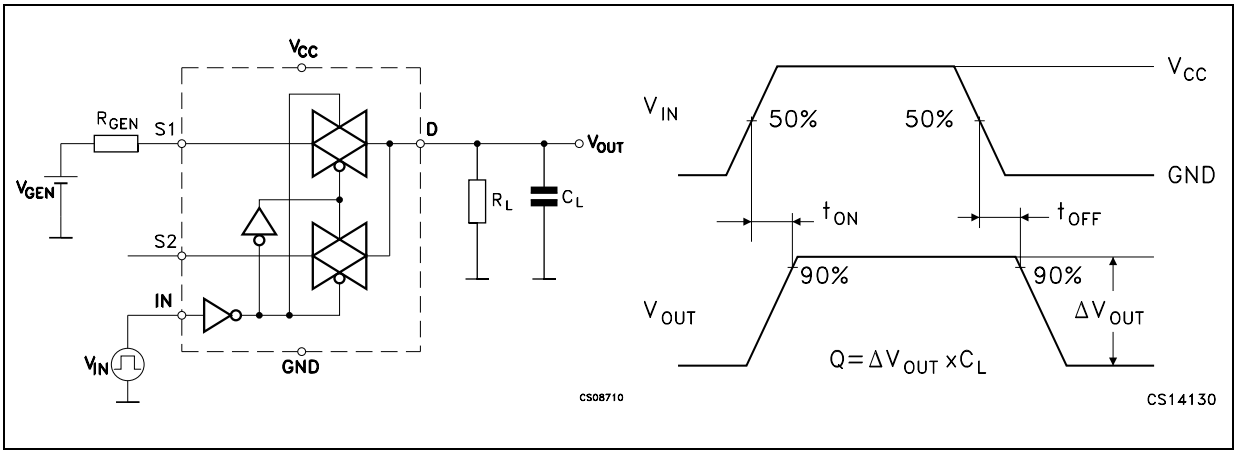
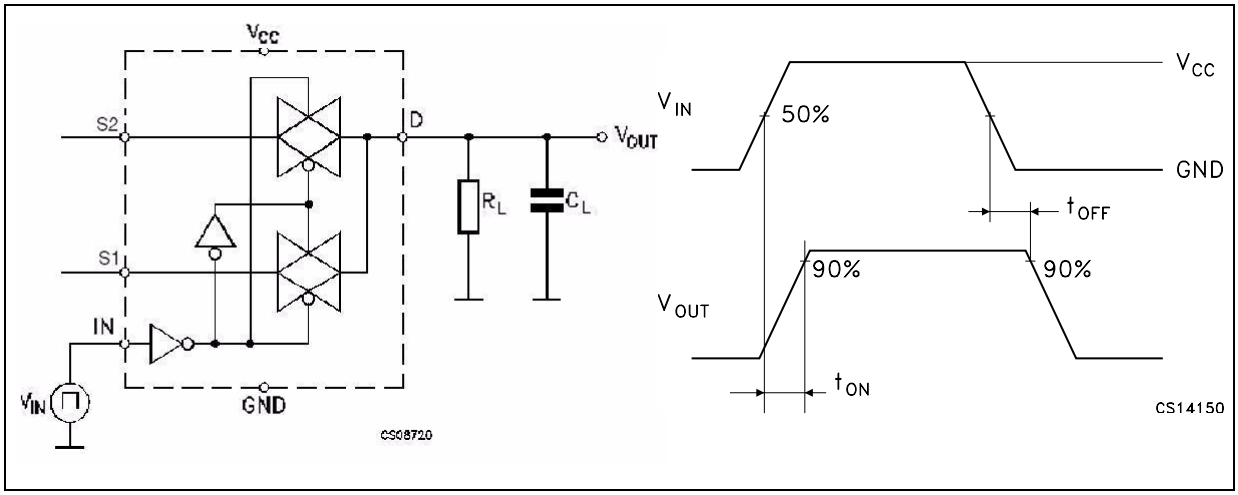


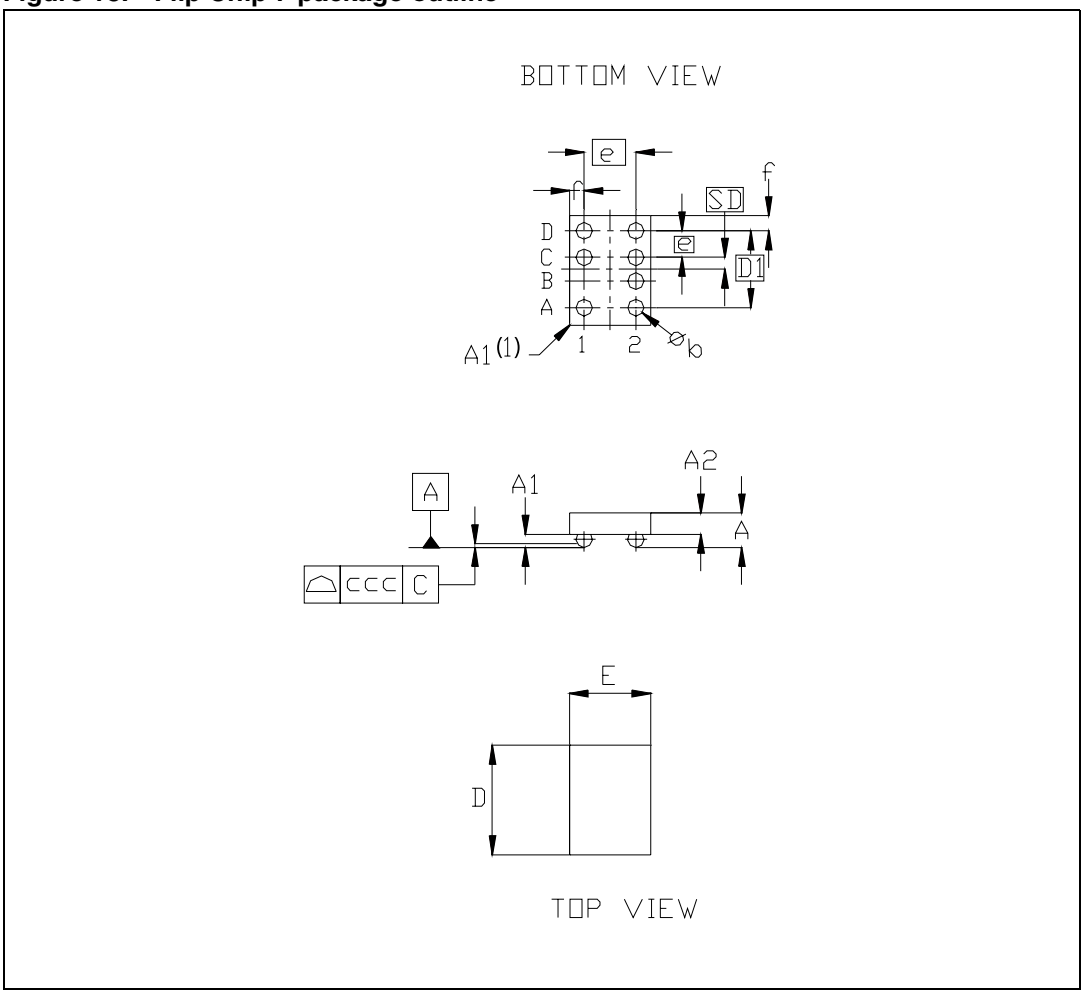
Figure 12. Turn-on, turn-off delay time



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 13. Flip Chip 7 package outline



1. The terminal pin 1 on the bumps side is identified by a distinguishing feature (for instance by a circular “clear area” - typically 0.1 mm diameter). The terminal pin 1 on the back-side of the product is identified by a distinguishing feature (for instance by a circular “dot” - typically 0.5 mm diameter).
2. Drawing not to scale.

Table 9. Flip Chip 7 package mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.585	0.65	0.715
A1	0.21	0.25	0.29
A2	–	0.4	–
b	0.265	0.315	0.365
D	1.018	1.068	1.118
D1	–	0.5	–
E	2.018	2.068	2.118
E1	–	1.5	–
e	0.45	0.5	0.55
f	–	0.284	–
ccc	–	0.08	–
SD	–	0.25	–

Figure 14. Footprint recommendations

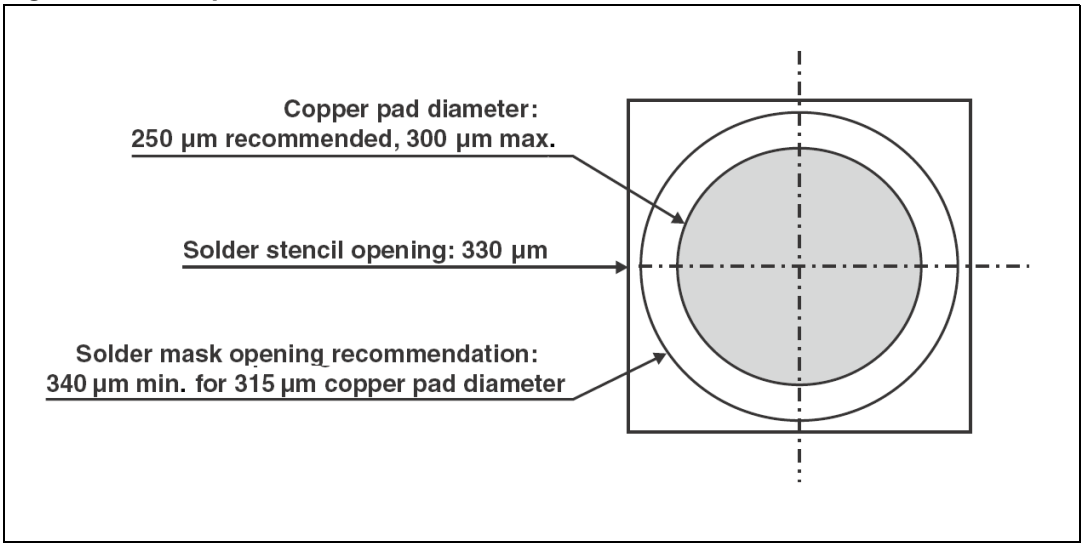


Figure 15. Marking

Dot, ST logo
S1 = marking
V = manufacturing location
yww = datecode (y = year, ww = week)

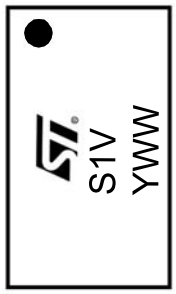


Figure 16. Flip Chip 7 tape specification

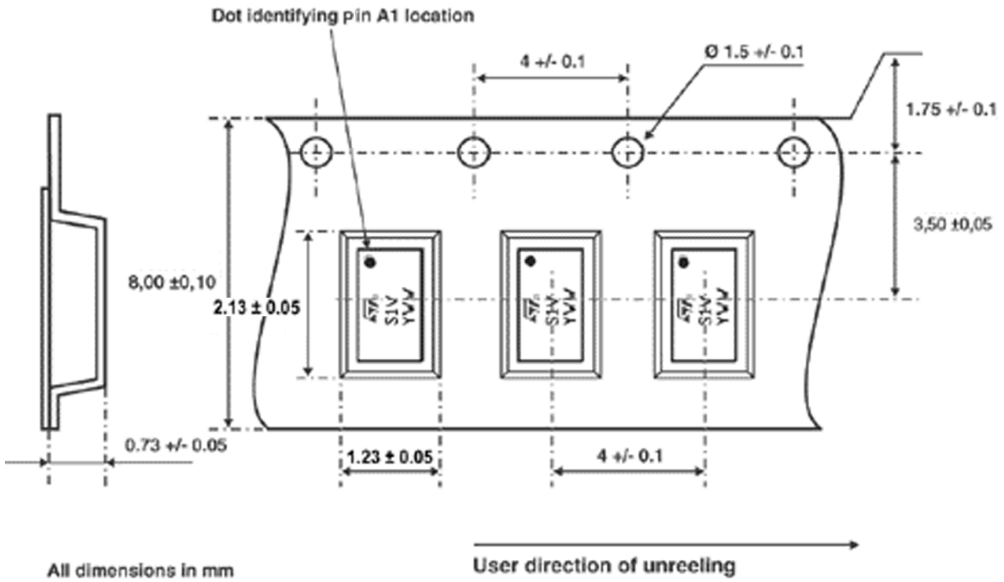


Figure 17. Flip Chip 7 reel information (front view)

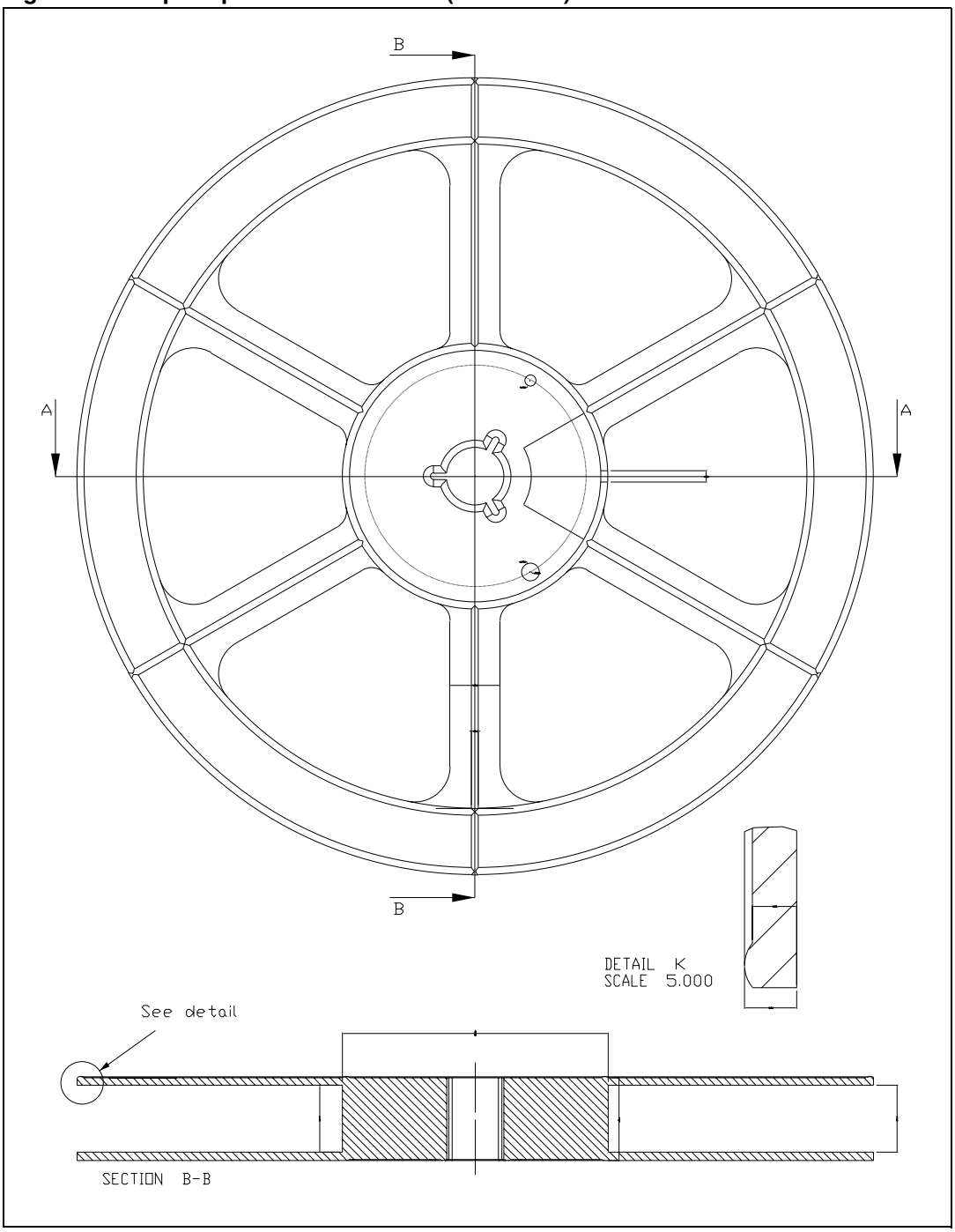
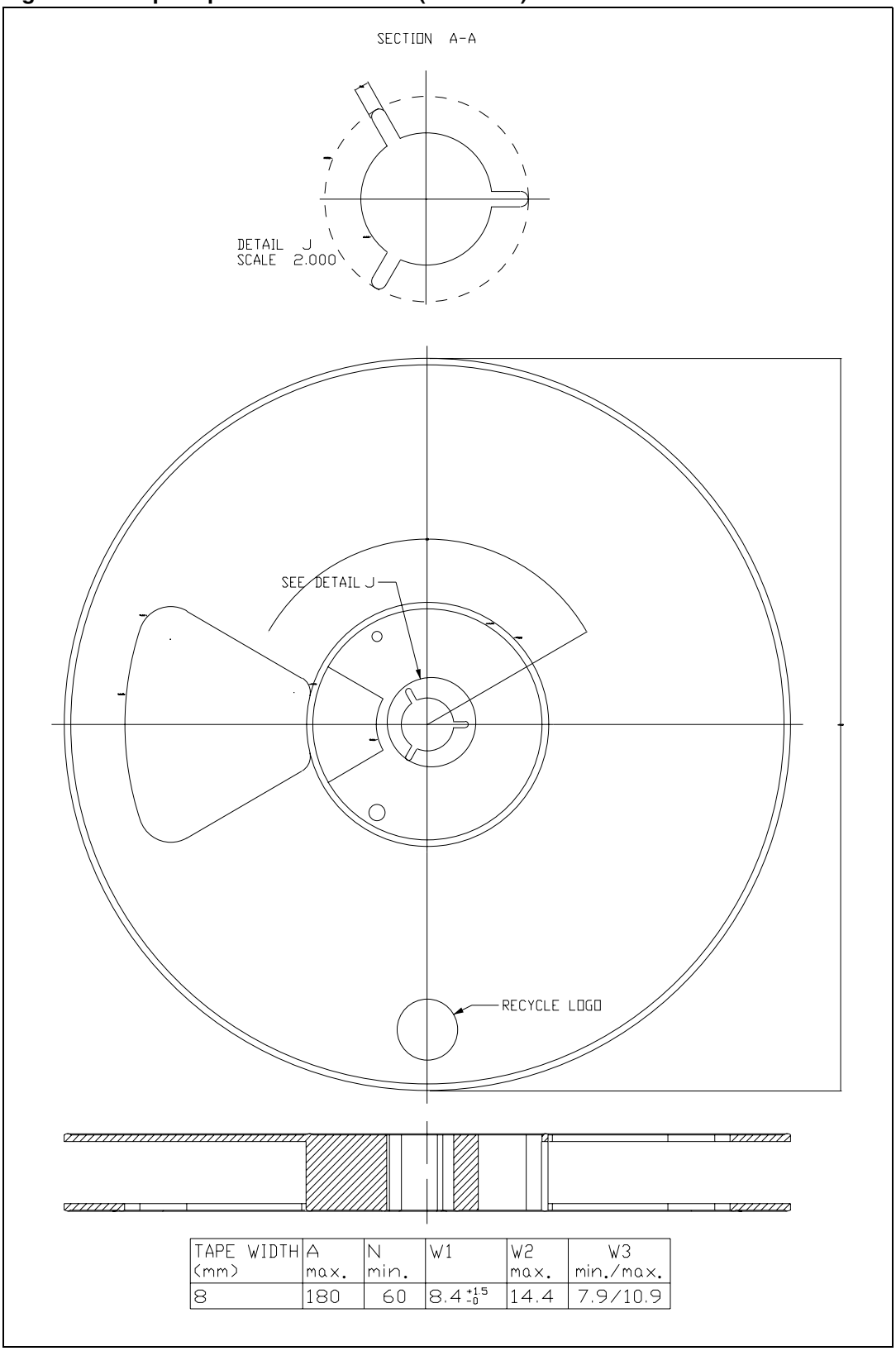


Figure 18. Flip Chip 7 reel information (rear view)



TAPE WIDTH (mm)	A max.	N min.	W1	W2 max.	W3 min./max.
8	180	60	$8.4^{+1.5}_{0}$	14.4	7.9/10.9

6 Revision history

Table 10. Revision history

Date	Revision	Changes
05-May-2006	1	First release
22-Nov-2006	2	Schematic *Figure 1 on page 3* updated
17-Apr-2007	3	Typo in cover page description
06-May-2009	4	Device summary table updated, watermark removed from all pages.
01-Oct-2009	5	Modified: *Figure 2*, *Figure 3*, *Section 4: Test circuits* and *Figure 13*. Updated: T_{stg} values in *Table 4*, removed footnote in *Table 5*.
30-Aug-2012	6	Updated *Section 2* (added cross-references), reformatted *Section 5*, added notes below *Figure 13*, updated *Table 9* (added “SD” value, renumbered *Table 9*, removed footnote), renamed *Figure 17* and *Figure 18*, minor corrections throughout document.

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