PRELIMINARY DATA SHEET

AC104X

2.5V 4-Port 10/100-TX Ethernet Transceiver

GENERAL DESCRIPTION

The AC104X is a highly integrated, 2.5V, low power, four port, 10BASE-T/100BASE-TX, Ethernet transceiver implemented in 0.25mm CMOS technology. Multiple modes of operation, including normal operation, test mode and power saving mode, are available through either hardware or software control.

Features include ENDECs, Scrambler/Descrambler, and Auto-Negotiation (ANeg) with support for parallel detection. The transmitter includes a dual-speed clock synthesizer that only needs one external clock source. The chip has built-in wave shaping driver circuit for both 10Mbps and 100Mbps, eliminating the need for an external hybrid filter. The receiver has an adaptive equalizer / DC restoration circuit for accurate clock / data recovery for the 100BASE-TX signal. It also provides an on-chip low pass filer / Squelch circuit for the 10BASE-T signal.

FEATURES

- 4 ports with RMII MAC interface
- 4 ports with 10/100 TX media interface
  - Full-Duplex or Half-Duplex
- Very small package
  - 100PQFP
- Very low power - TYP < 280mW / port
  - Cable Detect mode - TYP < 40 mW / port
  - Power Down mode - TYP < 3.3 mW / port
- 2.5V .25 micron CMOS
- RMII 3.3V tolerant I/O
- Fully compliant with
  - IEEE 802.3 / 802.3u
  - RMII
- Baseline Wander Compensation
- Multi-Function LED outputs
- Cable length indicator
- Reverse polarity detection and correction with Register Bit indication - Automatic or Forced
- HP Auto-MDIX
- 8 programmable interrupts

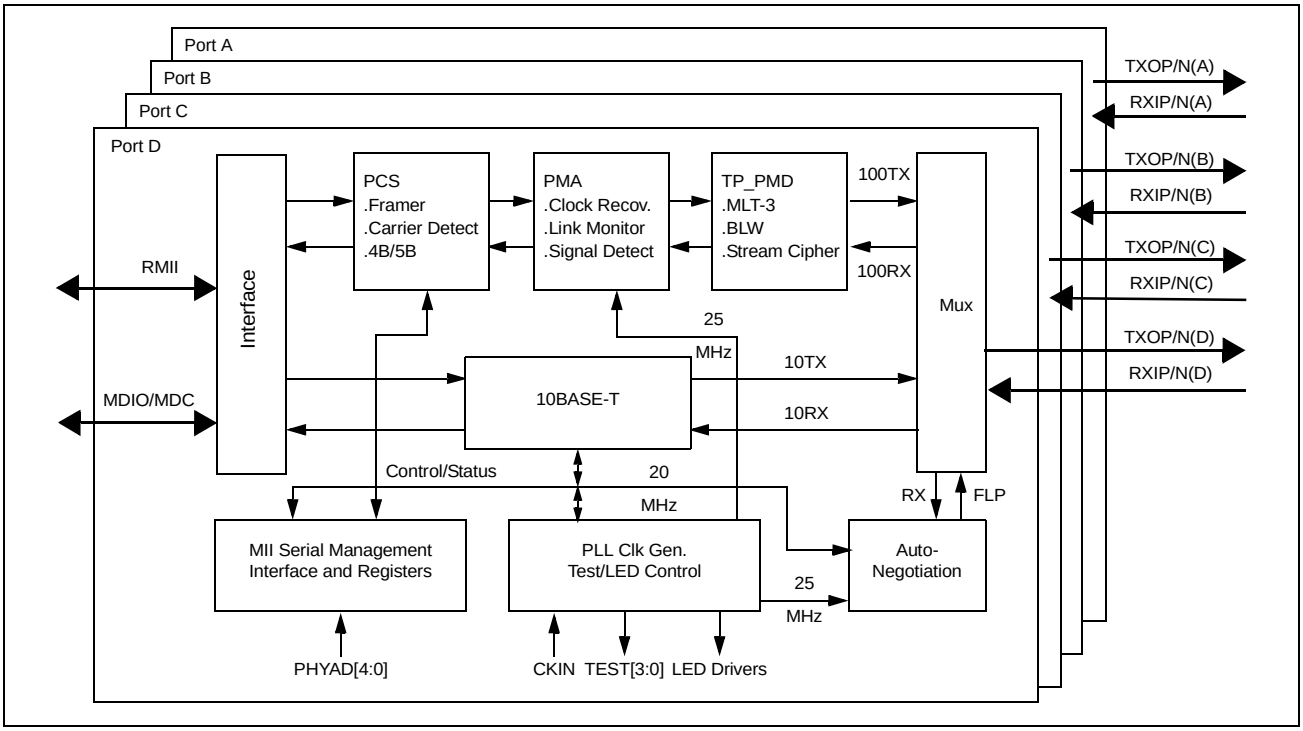

Figure 1: Functional Block Diagram

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REVISION HISTORY

Revision	*Date*	*Change Description*
AC104X-DS00-R	12/11/01	Initial Release.

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Section 1: Functional Description

The AC104X physical layer device (PHY) integrates the 100BASE-TX and 10BASE-T functions in a single four port chip that is used in Fast Ethernet 10/100 Mbps applications. The 100BASE-TX section consists of PCS, PMA, and PMD functions and the 10BASE-T section is consisted of Manchester ENDEC and transceiver functions. The device performs the following functions:

- 4B/5B
- MLT3
- NRZI
- Manchester Encoding and Decoding
- Clock and Data Recovery
- Stream Cipher Scrambling / De-Scrambling
- Adaptive Equalization
- Line Transmission
- Carrier Sense
- Link Integrity Monitor
- Auto-Negotiation (ANeg)
- Auto-MDI/MDIX
- RMII MAC connectivity
- MII Management Function

It also provides an RMII consortium compatible Reduced Media Independent Interface (RMII) to communicate with an Ethernet Media Access Controller (MAC). Selection of 10 or 100 Mbps operation is based on the settings of internal Serial Management Interface registers or determined by the on-chip ANeg logic. The device can operate in 10 or 100 Mbps with full-duplex or half-duplex mode on a per-port basis.

MAC Interface

RMII

The Reduced Media Independent Interface (RMII) is used to connect the PHY with the MAC. The PHY and MAC obtain their clock from a common 50 MHz source, such as a clock oscillator. This clock is shared by all ports within the PHY for transmitting and receiving data on 2 individual 2-bit data buses. In 100M mode, RXD[1:0] is sampled on every cycle of REFCLK. In 10M mode, RXD[1:0] is sampled on every 10th cycle of REFCLK. RXER is generated by the PHY to indicate a receive error to the MAC. TX_EN is generated by the MAC to indicate to the PHY when there is valid data on the transmit bus. In 100M mode, the PHY will read 2 bits from TXD[1:0] for each cycle of REFCLK. In 10M mode, the PHY will read 2 bits of data from TXD[1:0] every 10th cycle of REFCLK.

The Serial Management Interface (SMI) is shared between all ports in the PHY. This totals 7 pins per port plus 3 per PHY.

SMI

The PHY's internal registers are accessible only through the MII 2-wire Serial Management Interface (SMI). MDC is a clock input to the PHY, which is used to latch in or out data and instructions for the PHY. The clock can run from 2.5MHz to 25 MHz. MDIO is a bi-directional connection used to write instructions to, write data to, or read data from the PHY. Each data bit is latched either in or out on the rising edge of MDC. MDC is not required to maintain any speed or duty cycle, provided no half cycle is less than 20ns and that data is presented synchronous to MDC.

MDC/MDIO are a common signal pair to all ports on a design. Therefore, each port needs to have its own unique Physical Address. The Physical Address of the PHY is set using the pins defined as PHYAD[4:2]. These input signals are strapped externally and sampled as reset is negated. PHYAD[1:0] are addressed for each port internal to the PHY. Internal addresses are either 00, 01, 10, 11 or 01, 10, 11, 00 depending on the polarity of PHYAD_ST during reset.

At idle, the PHY is responsible to pull MDIO line to a high state. Therefore, a 1.5K Ohm resistor is used to pull the MDIO signal high. The PHYAD can be reprogrammed via software. A detailed definition of the Serial Management registers can be found in the next section.

At the beginning of a read or write cycle, the MAC will send a continuous 32 bits of one at the MDC clock rate to indicate preamble. A zero and a one will follow to indicate start of frame. A read OP code is a one and a zero, while a write OP code is a zero and a one. These will be followed by 5 bits to indicate PHY address and 5 bits to indicate register address. Then 2 bits follow to allow for turn around time. For read operation, the first bit will be high impedance. Neither the PHY nor the station will assert this bit. During the second bit time, the PHY will assert this bit to a zero. For write operation, the station will drive a one for the first bit time, and a zero for the second bit time. The 16 bits data field is then presented. The first bit that is transmitted is bit 15 of the register content.

INTERRUPT

The INTR pin on the PHY will be asserted whenever one of 8 selectable interrupt events occur. Selection is made by setting the appropriate bit in the upper half of the Interrupt Control / Status register. When the INTR bit goes active, the MAC interface is required to read the Interrupt Control / Status register to determine which event caused the interrupt. The Status bits are read only and clear on read. When INTR is not asserted, the pin is held in a high impedance state.

MEDIA INTERFACE

10BASE-T

When configured to run in 10BASE-T mode, either through hardware configuration, software configuration or ANeg, the PHY will support all the features and parameters of the industry standards.

TRANSMIT FUNCTION

Parallel to Serial logic is used to convert the 2-bit data into the serial stream. The serialized data goes directly to the Manchester encoder where it is synthesized through the output waveshaping driver. The waveshaper reduces any EMI emission by filtering out the harmonics, therefore eliminating the need for an external filter.

RECEIVE FUNCTION

The received signal passes through a low-pass filter, which filters out the noise from the cable, board, and transformer. This eliminates the need for a 10BASE-T external filter. A Manchester decoder converts the incoming serial stream. Serial to Parallel logic is used to generate the 2-bit data.

LINK MONITOR

The received signal passes through a low-pass filter, which filters out the noise from the cable, board, and transformer. This eliminates the need for a 10BASE-T external filter. A Manchester decoder converts the incoming serial stream. Serial to Parallel logic is used to generate the 2-bit data.

100BASE-TX

When configured to run in 100BASE-TX mode, either through hardware configuration, software configuration or Aneg.

TRANSMIT FUNCTION

In 100BASE-TX mode, the PHY transmit function converts synchronous 2-bit data to a pair of 125 Mbps differential serial data streams. The serial data is transmitted over network twisted pair cables via an isolation transformer. Data conversion includes 4B/5B encoding, scrambling, parallel to serial, NRZ to NRZI, and MLT-3 encoding. The entire operation is synchronous to 25 MHz and 125 MHz clock. Both clocks are generated by an on-chip PLL clock synthesizer that is locked on to an external 25 MHz clock source.

The transmit data is transmitted from the MAC to the PHY via the TXD[1:0] signals. The 4B/5B encoder replaces the first two nibbles of the preamble from the MAC frame with a /J/K/ code-group pair Start-of-Stream Delimiter (SSD), following the onset of TX_EN signal. The 4B/5B encoder appends a /T/R/ code-group pair End-of-Stream Delimiter (ESD) to the end of transmission in place of the first two IDLE code-groups that follow the negation of the TX_EN signal. The encapsulated data stream is converted from 4-bit nibbles to 5-bit code-groups. During the inter-packet gap, when there is no data present, a continuous stream of IDLE code-groups are transmitted. When TX_ER is asserted while TX_EN is active, the Transmit Error code-group /H/ is substituted for the translated 5B code word. The 4B/5B encoding is bypassed when Reg. 21.1 is set to “1”, or the PCSBP pin is strapped high.

In 100BASE-TX mode, the 5-bit transmit data stream is scrambled as defined by the TP-PMD Stream Cipher function in order to reduce radiated emissions on the twisted pair cable. The scrambler encodes a plain text NRZ bit stream using a key stream periodic sequence of 2047 bits generated by the recursive linear function:

$$X[n] = X[n-11] + X[n-9] \text{ (modulo 2)}$$

The scrambler reduces peak emissions by randomly spreading the signal energy over the transmitted frequency range, thus eliminating peaks at any single frequency. For repeater applications, where all ports transmit the same data simultaneously, signal energy is spread further by using a non-repeating sequence for each PHY, i.e., the scrambled seed is unique for each different PHY based on the PHY address.

PARALLEL TO SERIAL, NRZ TO NRZI, AND MLT3 CONVERSION

The 5-bit NRZ data is clocked into PHY's shift register with a 25 MHz clock, and clocked out with a 125 MHz clock to convert it into a serial bit stream. The serial data is converted from NRZ to NRZI format, which produces a transition on Logic 1 and no transition on Logic 0. To further reduce EMI emissions, the NRZI data is converted to an MLT-3 signal. The conversion offers a 3dB to 6dB reduction in EMI emissions. This allows system designers to meet the FCC Class B limit. Whenever there is a transition occurring in NRZI data, there is a corresponding transition occurring in the MLT-3 data. For NRZI data, it changes the count up/down direction after every single transition. For MLT-3 data, it changes the count up/down direction after every two transitions. The NRZI to MLT-3 data conversion is implemented without reference to the bit timing or clock information. The conversion requires detecting the transitions of the incoming NRZI data and setting the count up/down direction for the MLT-3 data.

The slew rate of the transmitted MLT-3 signal can be controlled to reduce EMI emissions. The MLT-3 signal after the magnetic has a typical rise/fall time of approximately 4 ns, which is within the target range specified in the ANSI TP- PMD standard. This is guaranteed with either 1:1 or 1.25:1 transformer.

RECEIVE FUNCTION

The 100BASE-TX receive path functions as the inverse of the transmit path. The receive path includes a receiver with adaptive equalization and DC restoration in the front end. It also includes a MLT-3 to NRZI converter, 125 MHz data and clock recovery, NRZI/NRZ conversion, Serial-to-Parallel conversion, de-scrambler, and 5B/4B decoder. The receiver circuit starts with a DC bias for the differential RX+/- inputs, followed with a low-pass filter to filter out high frequency noise from the transmission channel media. An energy detect circuit is also added to determine whether there is any signal energy on the media. This is useful in the power-saving mode. The amplification ratio and slicer's threshold is set by the on-chip bandgap reference.

BASELINE WANDER COMPENSATION

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion. This creates jitter and possible increase in the bit error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of the DC component. This PHY implements a patent-pending DC restoration circuit. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. This design simplifies the circuit design and eliminates any random/systematic offset on the receive path. In the 10BASET, the baseline wander correction circuit is not required, and therefore is disabled.

CLOCK/DATA RECOVERY

The equalized MLT-3 signal passes through the slicer circuit, and gets converted to NRZI format. The PHY uses a proprietary mixed-signal phase locked loop (PLL) to extract clock information from the incoming NRZI data. The extracted clock is used to re-time the data stream and set the data boundaries. The transmit clock is locked to the 50 MHz clock input while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to the data stream, extracts the 125 MHz clock, and uses it for the bit framing for the recovered data. The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase alignment and locks to data in one transition. Its data/clock acquisition time after power-on is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, i.e. when the SD is de-asserted, the PLL will switch and lock on to REFCLK. At the PCS interface, the 5 bit data RXD[4:0] is synchronized to the 25 MHz RX_CLK.

DECODER/DE-SCRAMBLER

The de-scrambler detects the state of the transmit Linear Feedback Shift Register (LFSR) by looking for a sequence representing consecutive idle codes. The de-scrambler acquires lock on the data stream by recognizing IDLE bursts of 30 or more bits and locks its frequency to its de-ciphering LFSR.

Once lock is acquired, the device can operate with an inter-packet-gap (IPG) as low as 40 nS. However, before lock is acquired, the de-scrambler needs a minimum of 270 nS of consecutive idles in between packets in order to acquire lock.

The de-ciphering logic also tracks the number of consecutive errors received while the CRS_DV is asserted. Once the error counter exceeds its limit currently set to 64 consecutive errors, the logic assumes that the lock has been lost, and the de-cipher circuit resets itself. The process of regaining lock will start again.

Stream cipher de-scrambler is not used in the 10BASE-T modes.

LINK MONITOR

Signal level is detected through a squelch detection circuitry. A signal detect (SD) circuit allows the equalizer to assert high whenever the peak detector detects a post-equalized signal with peak to ground voltage greater than 400 mV. This is approximately 40% of a normal signal voltage level. In addition, the energy level must be sustained for longer than 2~3 mS in order for the signal detect signal to stay on. The SD gets de-asserted approximately 1~2 ms after the energy level drops consistently below 300 mV from peak to ground.

The link signal is forced low during a local loopback operation (Loopback register bit is set) and forced to high when a remote loopback is taking place (EN_RPBK is set).

In forced 100BASE-TX mode, when a cable is unplugged or no valid signal is detected on the receive pair, the link monitor enters in the "link fail" state and NLP's are transmitted. When a valid signal is detected for a minimum period of time, the link monitor enters Link Pass State and transmits MLT-3 signal.

10BASE-T/100BASE-TX

MULTI-MODE TRANSMIT DRIVER

The multi-mode driver transmits the MLT-3 coded signal in 100BASE-TX mode and Manchester coded signal in 10BASE-T mode.

In 10BASE-T mode, high frequency pre-emphasis is performed to extend the cable-driving distance without the external filter. The FLP and NLP pulses are also drive out through the 10BASE-T driver.

The 10BASE-T and 100BASE-TX transmit signals are multiplexed to the transmit output driver. This arrangement results in using the same external transformer for both the 10BASE-T and the 100BASE-TX. The driver output level is set by a built-in bandgap reference and an external resistor connected to the IBREF pin. The resistor sets the output current for all modes of operation. The TXOP/N outputs are open drain devices with a serial source to I/O pad resistance of 10 W max. When the 1:1 transformer is used, the current rating is 40 mA for the 2Vp-p MLT-3 signal, and 100 mA for the 5Vp-p Manchester signal. One can use a 1.25:1 transmit transformer for a 20% output driver power reduction. This will decrease the drive current to 32 mA for 100BASE-TX operation, and 80 mA for 10BASE-T operation.

ADAPTIVE EQUALIZER

The PHY is designed to accommodate a maximum of 150 meters UTP CAT-5 cable. An AT&T 1061 CAT-5 cable of this length typically has an attenuation of 31 dB at 100 MHz. A typical attenuation of 100-meter cable is 21 dB. The worst case cable attenuation is around 24-26 dB as defined by TP-PMD specification.

The amplitude and phase distortion from the cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pair cable. The equalizer has the ability to changes its equalizer frequency response according to the cable length. The equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

PLL CLOCK SYNTHESIZER

The PHY includes an on-chip PLL clock synthesizer that generates a 125 MHz clocks for the 100BASE-TX circuitry. It also generates 20 MHz and 100 MHz clocks for the 10BASE-T and ANeg circuitry. The PLL clock generator uses a fully differential VCO cell that introduces very low jitter. The Zero Dead Zone Phase Detection method implemented in the PHY design provides excellent phase tracking. A charge pump with charge sharing compensation is also included to further reduce jitter at different loop filter voltages. The on-chip loop filter eliminates the need for external components and minimizes the external noise sensitivity. Only one external 50 MHz crystal or clock source is required as a reference clock.

After power-on or reset, the PLL clock synthesizer generates the 20 MHz clock output until the 100BASE-X operation mode is selected.

JABBER AND SQE (HEARTBEAT)

After the MAC transmitter exceeds the jabber timer (46mS), the transmit and loopback functions will be disabled and COL signal get asserted. After TX_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse with 5-15BT is asserted after each transmitted packet. SQE is enabled in 10BASE-T by default, and can be disabled via SQE Test Inhibit.

REVERSE POLARITY DETECTION AND CORRECTION

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the PHY has the ability to detect the fact that either 8 NLPs or a burst of FLPs are inverted and automatically reverse the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

If the Auto Polarity Disable bit is set, then the Reverse Polarity bit can be written to force the polarity reversal of the receiver.

INITIALIZATION AND SETUP

HARDWARE CONFIGURATION

Several different states of operation can be chosen through hardware configuration. External pins may be pulled either high or low at reset time. The combination of high and low values determines the power on state of the device.

Many of these pins are multi-function pins which change their meaning when reset ends.

SOFTWARE CONFIGURATION

Several different states of operation can be chosen through software configuration. Please refer to the "SMI" on page 1 as well as Section 3 "Register Descriptions" on page 16.

LEDS

Each of the 4 ports has 3 individual LED outputs available to indicate Speed, Duplex/Collision, and Link/Activity. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active output states. If a multi-function pin is pulled up during reset to select a particular function, then that LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

AUTO-NEGOTIATION

By definition the 10/100 Transceiver is able to run at either 10Mbps or 100Mbps. In addition the PHY is able to run in either half-duplex or full-duplex. To determine the operational state, the PHY has hardware selects and software selects while also supporting Auto- Negotiation and Parallel Detection.

Legitimate operating states are:

- 10BASE-T half-duplex
- 10BASE-T full-duplex
- 100BASE-TX half-duplex
- 100BASE-TX full-duplex

The PHY can be hardware configured to force any one of the above mentioned modes. By forcing the mode, the PHY will only run in that mode, hence limiting the locations where the product will operate.

The PHY is able to negotiate its mode of operation using the Auto-Negotiation mechanism defined in the clause 28 of IEEE 802.3u specification. ANeg can be enabled or disabled by hardware (ANEGA pin) or software (Reg. 0.12) control. When the ANeg is enabled, the PHY chooses its mode of operation by advertising its abilities and comparing them with the ability received from its link partner. It can be configured to advertise 100BASE-TX or 10BASE-T operating in either full- or half-duplex.

Register 4 contains the current capabilities, speed and duplex, of the PHY, determined through hardware selects or chip defaults. The contents of Reg. 4 is sent to its link partner during the ANeg process using Fast Link Pulses (FLPs). An FLP is a string of 1s and 0s, each of which has a particular meaning, the total of which is called a Link Code Word. After reset, software can change any of these bits from 1 to 0 and back to 1, but not from 0 to 1. Therefore, the hardware has priority over software.

When ANeg is enabled, the PHY sends out FLPs during the following conditions:

- Power on
- Link loss
- Restart ANeg command by software

During this period, the PHY continually sends out FLPs while monitoring the incoming FLPs from the link partner to determine their optimal mode of operation. If FLPs are not detected during this phase of operation, Parallel Detection mode is entered (see below).

When the PHY receives 3 identical link code words (ignoring acknowledge bit) from its link partner, it stores these code words in Reg. 5, sets the acknowledge bit it the generated FLPs, and waits to receive 3 identical code word with the acknowledge bit set from the link partner. Once this occurs the PHY configures itself to the highest technology that is common to both ends. The technology priorities are:

1 100BASE-TX, full-duplex

2 100BASE-TX, half-duplex

3 10BASE-T, full-duplex

4 10BASE-T half-duplex.

Once the ANeg is complete, Reg. 1.5 is set, Reg. 1.[14:11] reflects negotiated speed and duplex mode, and the PHY enters the negotiated transmission and reception state. This state will not change until link is lost or the PHY is reset through either hardware or software, or the restart negotiation bit (Reg. 0.9) is set.

PARALLEL DETECTION

Because there are many devices in the field that do not support the ANeg process, but must still be communicated with, it is necessary to detect and link through the Parallel Detection process.

The parallel detection circuit is enabled in the absence of FLPs. The circuit is able to detect:

- Normal Link Pulse (NLP)
- 10BASE-T receive data
- 100BASE-TX idle

The mode of operation gets configured based on the technology of the incoming signal. If any of the above is detected, the device automatically configures to match the detected operating speed in the half-duplex mode. This ability allows the device to communicate with the legacy 10BASE-T and 100BASE-TX systems, while maintaining the flexibility of Auto-Negotiation.

AUTOMATIC MDI/MDIX CONFIGURATION

The AC104X supports the MDI/MDIX automatic configuration function. The automatic MDI/MDIX is intended to eliminate the need for crossover cables between similar devices. The assignment of pin-outs for the Auto-MDI/MDIX is shown below:

Table 1: Auto-MDI/MDIX Pinout Assignments

Contact	*PHY*	*MDI*	*MDIX*
1	TXOP	TXOP	RXIP
2	TXON	TXON	RXIN
3	RXIP	RXIP	TXOP
4	N/C	N/C	N/C
5	N/C	N/C	N/C
6	RXIN	RXIN	TXON
7	N/C	N/C	N/C
8	N/C	N/C	N/C

DIAGNOSTICS

LOOPBACK OPERATION

Local Loopback is provided for testing purposes. It can be enabled by writing to Reg. 0.14.

The Local Loopback routes transmitted data through the transmit path back to the receiving path's clock and data recovery module. The loopback data are presented to the PCS in 5 bits symbol format. This loopback is used to check the operation of the 5-bit symbol decoder and the phase locked loop circuitry. In Local Loopback, the SD output is forced to logic one and TXOP/N outputs are tri-stated.

CABLE LENGTH INDICATOR

In 100BASE-T mode, the PHY can detect the approximate length of the cable it's attached and display the result in Reg. 20.[7:4]. A reading of [0000] translates to < 10m cable used, [0001] translates to ~ 10 meter of cable, and [1111] translates to 150 meter cable. The cable length value can be used by the network manage to determine the proper connectivity of the cable and to manage the cable plant distribution

RESET AND POWER

The PHY can be reset in three ways:

- During initial power on.
- Hardware Reset: A logic low signal of 150 µs pulse width is applied to RST* pin.
- Software Reset: Write a one to SMI Reg. 0.15.

The power consumption of the device is significantly reduced due to its built-in power management features. Separate power supply lines are used to power the 10BASE-T circuitry and the 100BASE-TX circuitry. Therefore, the two circuits can be turned on and turned off independently. When the PHY is set to operate in 100BASE-TX mode, the 10BASE-T circuitry is powered down, and vice versa.

The following power management features are supported:

- Power down mode: This can be achieved by writing to Register 0.11 or pulling PWRDN pin high. During power down mode, the device is still be able to interface through the MDC/MDIO management interface.

- Energy detect/power saving mode: Energy detect mode turns off the power to select internal circuitry when there is no live network connected. Energy Detect (ED) circuit is always turned on to monitor if there is a signal energy present on the media. The SMI circuitry is also powered on and ready to respond to any management transaction. The transmit circuit still send out link pulses with minimum power consumption. If a valid signal is received from the media, the device powers up and resumes normal transmit/receive operation. (Patent Pending)
- Reduced Transmit Drive Strength mode: Additional power saving can be gained at the PHY level by designing with 1.25:1 turns magnetic ratio and asserting the TP125 pin at reset.

CLOCK

The clock input must have a TTL clock oscillator measured at 50 MHz-100PPM.

Section 2: Pin Description

PIN DIAGRAM

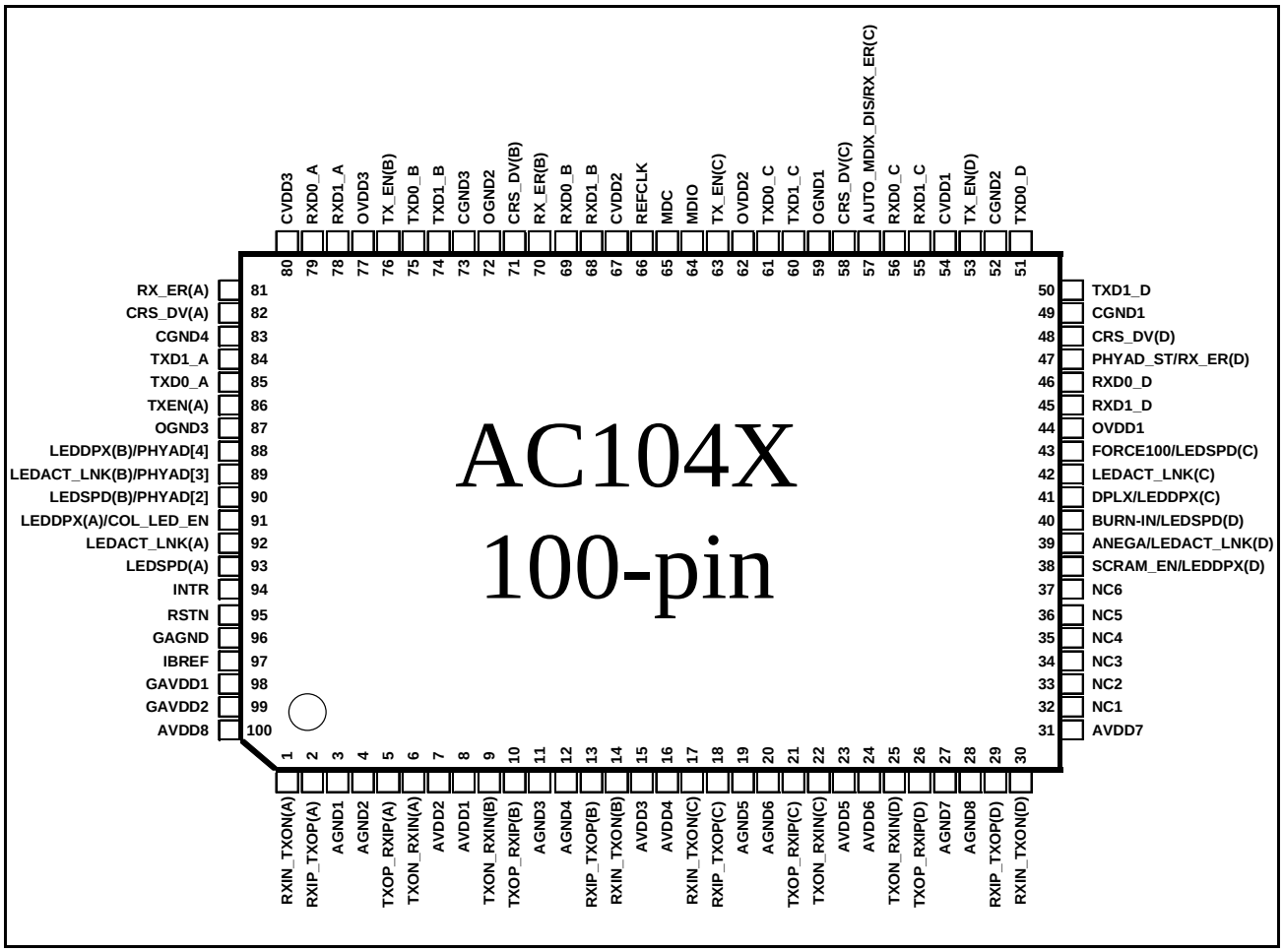

Figure 2: AC104X 100-pin

PIN DESCRIPTIONS

Many of the pins of these devices have multiple functions. Designate the multi-function pins by bolding the pin number. Designers must assure that they have identified all modes of operation prior to final design.

The pin assignment shown below and in the pin description table is subject to change without notice. Contact Altima Communications Inc. before implementing any design based on the information provided in this data sheet.

Signal types:

- I = inputs
- O = outputs
- Z = high impedance
- U = pull up
- D = pull down
- A = analog signal
- * = Active Low Signal
- NC = No Connect pin

Table 2: MDI (Media Dependent Interface) Pins

Pin Name	*Pin #*	*Type*	*Description*
RXIN_TXON(A)	1	AI/O	MDI: Receiver input Negative for both 10BASE-T and 100BASE-TX.
RXIN_TXON(B)	14	AI/O	MDIX: Transmitter output Negative for both 10BASE-T and 100BASE-TX.
RXIN_TXON(C)	17	AI/O	
RXIN_TXON(D)	30	AI/O	
RXIP_TXOP(A)	2	AI/O	MDI: Receiver input Positive for both 10BASE-T and 100BASE-TX.
RXIP_TXOP(B)	13	AI/O	MDIX: Transmitter output Positive for both 10BASE-T and 100BASE-TX.
RXIP_TXOP(C)	18	AI/O	
RXIP_TXOP(D)	29	AI/O	
TXON_RXIN(A)	6	AI/O	MDI: Transmitter output Negative for both 10BASE-T and 100BASE-TX.
TXON_RXIN(B)	9	AI/O	MDIX: Receiver input Negative for both 10BASE-T and 100BASE-TX.
TXON_RXIN(C)	22	AI/O	
TXON_RXIN(D)	25	AI/O	
TXOP_RXIP(A)	5	AI/O	MDI: Transmitter output Positive for both 10BASE-T and 100BASE-TX.
TXOP_RXIP(B)	10	AI/O	MDIX: Receiver input Positive for both 10BASE-T and 100BASE-TX.
TXOP_RXIP(C)	21	AI/O	
TXOP_RXIP(D)	26	AI/O	

Table 3: RMII (Reduced Media Independent Interface) Pins

Pin Name	Pin #	Type	Description
TXD[1:0](A) TXD[1:0](B) TXD[1:0](C) TXD[1:0](D)	84, 85 74, 75 60, 61 50, 51	I,D I,D I,D I,D	RMII Transmit Data. The MAC sources the TXD[1:0](n) synchronous with REFCLK when TX_EN(n) is asserted.
TX_EN(A) TX_EN(B) TX_EN(C) TX_EN(D)	86 76 63 53	I,D I,D I,D I,D	RMII Transmit Enable. TX_EN(n) is asserted high by the MAC to indicate that valid data for transmission is presented on the TXD[1:0](n).
RXD[1:0](A) RXD[1:0](B) RXD[1:0](C) RXD[1:0](D)	78,79 68,69 55,56 45,46	O O O O	RMII Receive Data. The PHY sources the RXD[1:0](n) synchronous with REFCLK when CRS_DV(n) is asserted.
CRS_DV(A) CRS_DV(B) CRS_DV(C) CRS_DV(D)	82 71 58 48	O O O O	CRS_DV(n) is asserted high when media is non-idle.
RX_ER(A) RX_ER(B) RX_ER(C) RX_ER(D)	81 70 57 47	O O I/O,D I/O,D	RMII Receive Error. When RX_ER is asserted high, it indicates an error has been detected during frame reception.
REFCLK	66	I	Reference Clock Input – 50 MHz-100PPM TTL

Table 4: SMI (Serial Management Interface) Pins

Pin Name	Pin #	Type	Description
MDIO	64	I/O, D	Management Data Input/Output. Bi-directional data interface. 1.5K pull up resistor required (as specified in IEEE-802.3).
MDC	65	I, D	Management Data Clock. 0 to 25 MHz clock sourced by the MAC for transfer of MDIO data.
INTR	94	Z	Interrupt. See Register 17. The INTR pin has a high impedance output. A 1KΩ Resister pull-up is required for this active low signal.

Table 5: PHY Address Pins

Pin Name	Pin #	Type	Description
PHYAD_ST	47	I/O,D	This pin sets the two least significant digits of the PHY address for all four ports according to the two options below: 1 at reset = A-XXX00, B-XXX01, C-XXX10, D-XXX11 0 at reset = A-XXX01, B-XXX10, C-XXX11, D-XXX00
PHYAD [4] PHYAD [3] PHYAD [2]	88 89 90	I/O I/O I/O	PHY Address [4:2]. These pins set the three most significant digits for the PHY address. PHYAD [4] sets the most significant digit. PHYAD [1:0] are internally set according to the status of PHYAD_ST. The PHYAD determines the scramble seed, and helps to reduce EMI when there are multiple ports switching at the same time.

Table 6: Mode Pins

Pin Name	Pin #	Type	Description
AUTO_MDIX_DIS	57	I/O	Auto-MDIX Disable. Pulled up upon reset will turn off the Auto-MDIX future.
DPLX	41	I/O	Full-Duplex Mode. The default value of the control bit (Reg.0.8) is dependent on this pin when the ANEGA pin is pulled-low/asserted-low. When asserted high, the PHY operates in full-duplex mode as the default mode.
FORCE100	43	I/O	FORCE100: Force 100BASE-TX Operation. When this signal is pulled high and ANEGA is low upon reset, all ports are forced to 100BASE-TX operation. When asserted low and ANEGA is low, all ports are forced to 10BASE-T operation. When ANEGA is high, FORCE100 has no effect on operation.
SCRAM_EN	38	I/O	Scrambler Enable. Pulled high under normal circumstances to enable scrambler and de-scrambler. If pulled low upon reset, scrambling functions will be disabled.
ANEGA	39	I/O	Auto-Negotiation Ability. Asserted high means auto-negotiation enable while low means manual selection through DPLX, FORCE100.
BURN_IN*	40	I/O	Burn-In mode. Burn-in mode for reliability assurance control. This is reserved for factory testing only.
COL_LED_EN	91	I/O	If pulled high with 10kΩ, LEDDPX pins will toggle whenever there is a Collision detected in half-duplex. (Should be pulled-high!) If pulled low, LEDDPX pins will not toggle.

Table 7: LED Pins

Pin Name	Pin #	Type	Description
LEDDPX[A] LEDDPX[B] LEDDPX[C] LEDDPX[D]	91 88 41 38	O O O O	Port[n] Duplex LED. Active state indicates Full-Duplex. In half-duplex, this pin is designed to blink to indicate collision.
LEDACT_LNK[A] LEDACT_LNK[B] LEDACT_LNK[C] LEDACT_LNK[D]	92 89 42 39	O O O O	Port[n] Activity/Link LED. Active state indicates a valid link. When there is receive or transmit activity, LED toggles between high and low for 250 ms interval.
LEDSPD[A] LEDSPD[B] LEDSPD[C] LEDSPD[D]	93 90 43 40	O O O O	Port[n] Speed LED. Active state indicates 100BASE-TX mode.

Polarity of LEDs is determined by polarity of mode pins.

Table 8: Miscellaneous Pins

Pin Name	Pin #	Type	Description
RSTN	95	I, U	Reset. An active low input forces a known initialization state. The reset pulse duration must be > 100 us. Setting MII Reg. 0.15 asserts software reset, which has the same functionality as the hardware reset.
Reserved	32 33 34 35 36 37	AO	Should be left un-connected.
IBREF	97	A	Reference Bias Resistor. Must be tied to analog ground through an external 10KΩ (1%) resistor.

Table 9: Power and Ground Pins

Pin Name	Pin #	Type	Description
OVDD	44, 62, 77	P	Digital +2.5V power supply for I/O.
OGND	59, 72, 87	G	Digital ground for I/O.
CVDD	54, 67, 80	P	Digital +2.5V power supply for core logic.
CGND	49, 52, 73, 83	G	Digital ground for core logic.
AVDD	7, 8, 15, 16, 23, 24, 31, 100	P	+2.5V power supply for analog circuit.
AGND	3, 4, 11, 12, 19, 20, 27, 28	G	Ground for analog circuit.
GAVDD	98,99	P	+2.5V power supply for common analog circuits.
GAGND	96	G	Ground for common analog circuits.

Section 3: Register Descriptions

The first seven registers of the MII register set are defined by the MII specification. In addition to these required registers are several Altima Communications Inc. specific registers. There are reserved registers and/or bits that are for Altima internal use only. The following standard registers are supported. Register numbers are in decimal format; the values are in hex format.

When writing to registers it is recommended that a read/modify/write operation be performed, as unintended bits may get to unwanted states. This applies to all registers, including those with reserved bits.

LEGEND

RW	Read and Write Access
SC	Self Clearing
LL	Latch Low until cleared by reading
RO	Read Only
RC	Cleared on Read
LH	Latch High until cleared by reading

Table 10: Registers 0-7

Register	*Description*	*Default*
0	Control Register	3000
1	Status Register	7849
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	5542
4	Auto-Negotiation Advertisement Register	01E1
5	Auto-Negotiation Link Partner Ability Register	0001
6	Auto-Negotiation Expansion Register	0004
7	Next Page Advertisement Register	2001

Table 11: Registers 8-31

Register	Description	Default
8-15	Reserved	XXXX
16	BT and Interrupt Level Control Register	1000
17	Interrupt Control/Status Register	0000
18,19	Reserved	XXXX
20	Cable measurement Capability Register	XXXX
21	Receive Error Counter Register	0000
22-31	Reserved	XXXX

Table 12: Register 0: Control

Bit	Name	Description	Mode	Default
0.15	Reset	1 = PHY reset. This bit is self-clearing.	RW/SC	0
0.14	Loopback	1 = Enable loopback mode. This loopbacks the TXD to RXD and ignores all the activity on the cable media. 0 = Normal operation.	RW	0
0.13	Speed Select	1 = 100 Mbps 0 = 10 Mbps. AutoNeg enabled: This bit is writable but will be ignored.	RW	Set by FORC100 pin
0.12	ANeg Enable	1 = Enable Auto-Negotiate process (overrides 0.13 and 0.8) 0 = Disable Auto-Negotiate process. Mode selection is controlled via bit 0.8, 0.13 or through the mode pins.	RW	Set by ANEGA
0.11	Power Down	1 = Power down. All blocks except for SMI turns off. Setting PWRDN pin to high achieves the same result. 0 = Normal operation.	RW	0
0.10	Isolate	1 = Electrically isolate the PHY from MII. PHY is still able to response to SMI. 0 = Normal operation.	RW	
0.9	Restart ANeg	1 = Restart Auto-Negotiation process. 0 = Normal operation.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex. 0 = Half-duplex. AutoNeg enabled: This bit is writable but will be ignored. The default value is 0 if auto-negotiation is enabled via pin ANEGA.	RW	Set by DPLX and ANEGA pin
0.7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal. Collision test is disabled if PCSBP pin is high. Collision test is enabled regardless of the duplex mode. 0 = Disable COL test.	RW	0
0.[6:0]	Reserved		RW	0000000

Table 13: Register 1: Status

Bit	Name	Description	Mode	Default
1.15	100BASE-T4	Permanently tied to zero indicates no 100BASE-T4 capability.	RO	0
1.14	100BASE-TX Full-Duplex	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	RO	Set by DPLX pin
1.13	100BASE-TX Half-Duplex	1 = 100BASE-TX half-duplex capable. 0 = Not TX half-duplex capable.	RO	1
1.12	10BASE-T Full-Duplex	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	RO	Set by DPLX pin
1.11	10BASE-T Half-Duplex	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	RO	1
1.[10:7]	Reserved		RO	0000
1.6	MF Preamble Suppression	The PHY is able to perform management transaction without MDIO preamble. The management interface needs minimum of 32 bits of preamble after reset.	RO	1
1.5	ANeg Complete	1 = Auto-negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set. 0 = Auto-negotiate process not completed.	RO	0
1.4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit remains set until it is cleared by reading register 1.	RO/LH	0
1.3	ANeg Ability	1 = Able to perform Auto-Negotiation function, default value determined by ANEGA pin. 0 = Unable to perform Auto-Negotiation function.	RO	1
1.2	Link Status	1 = Link is established. If link fails, this bit clears and remains at 0 until register is read again. 0 = Link has gone down.	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detect. 0 = No Jabber condition detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

Table 14: Register 2: PHY Identifier 1

Reg.bit	Name	Description	Mode	Default
2.[15:0]	OUI*	Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022(H)

* = Based on an OUI is 0010A9 (Hex)

Table 15: Register 3: PHY Identifier 2

Bit	Name	Description	Mode	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	010101
3.[9:4]	Model Number	6-bit manufacturer's model number.	RO	010100
3.[3:0]	Revision Number	4-bit manufacturer's revision number.	RO	0010

* = Based on an OUI of 0010A9 (Hex)

Table 16: Register 4: Auto-Negotiation Advertisement

Bit	Name	Description	Mode	Default
4.15	Next Page	1 = Next Page enabled. 0 = Next Page disabled.	RW	0
4.14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4.[13:11]	Reserved			0
4.10	FDFC	Full-Duplex Flow Control 1= Advertise that the DTE(MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0= MAC does not support flow control		
4.9	100BASE-T4	Technology not supported. This bit always 0	RO	0
4.8	100BASE-TX Full-Duplex	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASETX full-duplex capable.	RW	Set by DPLX pin
4.7	100BASE-TX	1 = 100BASE-TX half-duplex capable. 0 = Not TX half-duplex capable.	RW	1
4.6	10BASE-T Full-Duplex	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	RW	Set by DPLX pin
4.5	10BASE-T	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	RW	1
4.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

Table 17: Register 5: Auto-Negotiation Link Partner Ability Register/Link Partner Next Page Message

Bit	Name	Description	Mode	Default
5.15	Next Page	1 = Link partner desires Next Page transfer. 0 = Link partner does not desire Next Page transfer.	RO	0
5.14	Acknowledge	1 = Link Partner acknowledges reception of FLP words. 0 = Not acknowledged by Link Partner.	RO	0
5.[13:10]	Reserved			
5.9	100BASE-T4	1 = 100BASE-T4 supported by Link Partner. 0 = 100BASE-T4 not supported by Link Partner.	RO	0
5.8	100BASE-TX Full-Duplex	1 = 100BASE -X full-duplex supported by Link Partner. 0 = 100BASE-TX full-duplex not supported by Link Partner.	RO	0
5.7	100BASE-TX	1 = 100BASE-TX half-duplex supported by Link Partner. 0 = 100BASE-TX half-duplex not supported by Link Partner.	RO	0
5.6	10BASE-T Full-Duplex	1 = 10 Mbps full-duplex supported by Link Partner. 0 = 10 Mbps full-duplex not supported by Link Partner.	RO	0
5.5	10BASE-T	1 = 10 Mbps half-duplex supported by Link Partner. 0 = 10 Mbps half-duplex not supported by Link Partner.	RO	0
5.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

*When this register is used as Next Page Message, the bit definition is the same as Register 7.

Table 18: Register 6: Auto-Negotiation Expansion

Bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading Register 6, using the management interface. 0 = No fault detected by parallel detection logic.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner supports next page function. 0 = Link partner does not support next page function.	RO	0
6.2	Next Page Able	Next Page is supported.	RO	1
6.1	Page Received	This bit is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.	RO/ LH	0
6.0	Link Partner ANeg-Able	1 = Link partner is Auto-Negotiation capable. 0 = Link partner is not Auto-Negotiation capable.	RO	0

Table 19: Register 7: Auto-Negotiation Next Page Transmit

Bit	Name	Description	Mode	Default
7.15	NP	1 = Another Next Page desired. 0 = No other Next Page Transfer desired.	RW	0
7.14	Reserved		RO	0
7.13	MP	1 = Message page. 0 = Un-formatted page.	RW	1
7.12	ACK2	1 = Will comply with message. 0 = Can not comply with message.	RW	0
7.11	TOG_TX	1 = Previous value of transmitted link code word equals to 0. 0 = Previous value of transmitted link code word equals to 1.	RW	0
17.[10:0]	CODE	Message/Un-formatted Code Field.	RW	001

Table 20: Register 16: BT and Interrupt Level Control

Bit	Name	Description	Mode	Default
16.15	Reserved		RW	0
16.14	Reserved		RO	0
16.13	Reserved		RW	0
16.12	Reserved		RW	1
16.11	SQE Test Inhibit	1 = Disable 10BASE-T SQE testing. 0 = Enable 10BASE-T SQE testing, which generates a COL pulse following the completion of a packet transmission.	RW	0
16.10	BT Normal Loop-back	1 = Enable 10BASE-T normal loop-back. 0 = Disable 10BASE-T normal loop-back.	RW	0
16.[9:6]	Reserved		RO	0
16.5	Auto Polarity Disable	1 = Disable Auto Polarity detection/correction. 0 = Enable Auto Polarity detection/correction.	RW	0
16.4	Reverse Polarity	1= Reverse Polarity when Register 16.5 = 0 0= Normal Polarity when Register 16.5 = 0 If Register 16.5 is set to 1, writing a one to this bit will reverse the polarity of the transmitter.	RW	0
16.[3:0]	Reserved		RO	0

Table 21: Register 17: Interrupt Control/Status

Bit	Name	Description	Mode	Default
17.15	Jabber_IE	Jabber Interrupt Enable.	RW	0
17.14	Rx_Er_IE	Receive Error Interrupt Enable.	RW	0
17.13	Page_Rx_IE	Page Received Interrupt Enable.	RW	0
17.12	PD_Fault_IE	Parallel Detection Fault Interrupt Enable.	RW	0
17.11	LP_Ack_IE	Link Partner Acknowledge Interrupt Enable.	RW	0
17.10	Link_Status_Change_IE	Link Status Change Interrupt Enable.	RW	0
17.9	R_Fault_IE	Remote Fault Interrupt Enable.	RW	0
17.8	ANeg_Comp_IE	Auto-Negotiation Complete Interrupt Enable.	RW	0
17.7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17.6	Rx_Er_Int	This bit is set when RX_ER transitions high.	RC	0
17.5	Page_Rx_Int	This bit is set when a new page is received during ANeg.	RC	0
17.4	PD_Fault_Int	This bit is set when parallel detect fault is detected.	RC	0
17.3	LP_Ack_Int	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17.2	Link_Status_Changed_Int	This bit is set when link status switches are changed.	RC	0
17.1	R_Fault_Int	This bit is set when remote fault is detected.	RC	0
17.0	ANeg _Comp Int	This bit is set when ANeg is complete.	RC	0

Table 22: Register 18: Diagnostic

Bit	Name	Description	Mode	Default
18.15	Lp_Inbk	Link pulse loopback. 1 = Loopback the link pulse for auto-negotiation testing.	RW	0
18.14	Send_nlp	1 = Force link pulse generator to send nlp even in auto-negotiation mode.	RW	0
18.13	Force Link Pass bt	1 = Force 10BASE-T link pass.	RW	0
18.12	Force Link Pass tx	1 = Force 100BASE-TX link pass.	RW	0
18.11	DPLX	This bit indicates the result of the auto-negotiation for duplex arbitration.	RO	0
18.10	Speed	This bit indicates the result of the auto-negotiation for data speed arbitration.	RO	0
18.9	RX_PASS	In 10BASE-T mode, this bit indicates the Manchester data has been detected. In 100BASE-T mode, it indicates valid signal has been received but not necessarily locked on to.	RC	0
18.8	RX_LOCK	Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10BASE-T or 100BASE-TX). This bit is set whenever a cycle-slip occurs, and will remain set until it is read.	RC	0
18.[7:4]	ARB_STATE HIGHEST	Highest state of Auto-Negotiation state machine since reset on last read operation.	RC	0000
18.[3:0]	ARB_STATE LOWEST	Lowest state of Auto-Negotiation state machine since reset on last read operation.	RC	1111

Table 23: Register 19: Test Register

Bit	Name	Description	Mode	Default
19.[15:9]	Reserved	Reserved.	RW	00
19.8	Tx_fef	1 = Force FEF transmit.	RW	0
19.7	Error counter full	1 = Error count full. When set indicates the rx_error counter full in the receiver circuit. This event will cause de-scrambler to reset.	RC	0
19.6	Err cnt disable	1 = disable error counter in the receiver module.	RW	0
19.5	Disable watch dog timer for decipher	1 = Disable watch dog timer. 0 = Enable watch dog timer.	RW	0
19.4	Low Power Mode disable	1 = Disable advanced power saving mode. 0 = Enable advanced power saving mode.	RW	0
19.3	Enable digital loopback	1 = enable digital loop back.	RW	0
19.2	Test loop back	1 = enable analog test loop back.	RW	0
19.1	Remote loop back	1 = enable analog remote loop back.	RW	0
19.0	Jabber disable	1 = disable jabber.	RW	0

Table 24: Register 20: Cable Measurement Capability

Bit	Name	Description	Mode	Default
20.15	Reserved		RW	1
20.14	Reserved		RW	1
20.[13:9]	Reserved		RO	0
20.8	Adaption Disable	1 = Disable adaption.	RW	0
20.[7:4]	Cable Measurement Capability	These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100 MHz. The value is a read back from the equalizer, and the measured value is not absolute. These bits are only applicable to the 100BASE-TX mode.	RW	X
20.[3:0]	Adaption Low Limit Value	Adaption setting, when the SD signal is first detected.	RO	X

Table 25: Register 21: Receive Error Counter

Bit	Name	Description	Mode	Default
21.[15:0]	RX_ER Counter	Count Receive Error Events.	RO	0

Table 26: Register 22: Power Management

Bit	Name	Description	Mode	Default
22.[15:14]	Reserved		RO	00
22.13	PD_PLL	1 = Power down PLL circuit.	RO	X
22.12	PD_EQUAL	1 = Power down equalizer circuit.	RO	X
22.11	PD_BT_RCVR	1 = Power down 10 base T receiver.	RO	X
22.10	PD_LP	1 = Power down link pulse receiver.	RO	X
22.9	PD_EN_DET	1 = Power down energy detect circuit.	RO	X
22.8	Reserved		RO	1
22.[7:6]	Reserved		RW	11
22.5	MSK_PLL	0 = Force power up PLL circuit.	RW	1
22.4	MSK_EQUAL	0 = Force power up equalizer circuit.	RW	1
22.3	MSK_BT_RCVR	0 = Force power up 10 base T receiver.	RW	1
22.2	MSK_LP	0 = Force power up link pulse receiver.	RW	1
22.1	MSK_EN_DET	0 = Force power up energy detect circuit.	RW	1
22.0	Reserved		RW	1

Table 27: Register 23: Operation Mode

Bit	Name	Description	Mode	Default
23.[15:14]	Reserved		RW	0
23.13	Clk_rclk_save	1 = Set rclk save mode. Rclk will be shut off after 64 cycles of each packet.	RW	0
23.12	Reserved		RW	0
23.11	Scramble disable	1 = Disable scrambler.	RW	Reset by the SCRAM_EN pin.
23.10	Serial_bt_enable	1 = Enable serial bt mode.	RW	0
23.9	Pcsbp	1 = Enable PCS bypass mode.	RW	0
23.8	Age timer en	1 = Enable age timer in adaptation. 0 = Disable age timer in adaptation.	RW	0
23.7	Auto MDIX disable	1 = Disable auto MDIX feature.	RW	Reset by the AUTO_M_DIX_DIS pin.
23.6	MDIX mode	0 = MDI mode. 1 = Enable MDIX mode. When auto-mdix feature is enabled, this is a status bit, and is read only. When auto-mdix is disabled, this bit controls the mdi, mdix selection.	RW	0
23.5	Reserved		RO	0
23.[4:0]	Dlock drop counter	D lock drop counter	RO	XXXXX

Table 28: Register 24: CRC for Recent Received Packet

Bit	Name	Description	Mode	Default
24.[15:0]	CRC16	CRC16 value displayed. For system level test purpose.	RC	0000H

Table 29: Common Register 0: Common Operation Mode (Map to Phy Channel A, Reg 28)

Bit	Name	Description	Mode	Default
a.28.[15:5]	Reserved		RO	000H
a.28.4	Rmii_enable	1 = Put the chip in shared RMII mode. The MODE1 pin should be pulled down and the MODE0 pin should be pulled high for the default configuration.	RW	1
a.28.3	Interrupt Level	1 = Interrupt active high. 0 = Interrupt active low.	RW	0
a.28.2	Act Select	Act Event selector. 1 = TX or RX activity. 0 = Receive activity.	RW	1
a.28.1	Reserved		RO	0
a.28.0	Reserved		RW	0

Table 30: Common Register 1: Test Mode (Map to Phy Channel A, Reg 29)

Bit	Name	Description	Mode	Default
a.29.15	Reserved		RW	0
a.29.[14:10]	Reserved		RO	00010
a.29.[9:8]	Test Channel	Channel to be tested.	RW	00
a.29.[7:4]	Test mode	0000 = normal operation.	RW	0000
a.29.3	Burn In	1 = Enable Burn In Test mode. 0 = Normal Operation.	RW	Reset by the BURN_IN pin
a.29.2	Output Disable	1 = Disable all digital outputs. 0 = Normal operation.	RW	0
a.29.1	Global phy addr enable	1 = Write to phy addr 0 will write to all 4 phys on the chip. 0 = Normal operation.	RW	0
a.29.0	Reduce timer	1 = Reduce timer for auto-negotiation testing.	RW	0

Table 31: Common Register 2: Analog Settings (Map to Phy Channel A, Reg 30)

Bit	Name	Description	Mode	Default
a.30[15:14]	Edge rate control	Transmit Edge Rate Control.	RW	00
a.30.[13:12]	10 Squelch Level	10BT Slicer Level Control.	RW	01
a.30.[11:10]	Slice Level	Slicer Level.	RW	10
a.30.[9:8]	PBLW	Baseline Wander Bandwidth.	RW	10
a.30.[7:4]	CR_RES		RW	0110
a.30.[3:0]	DRV_RES		RW	0000

Table 32: 4B/5B Code-Group Table

PCS Code Group[4:0]	Symbol Name	MII (TXD/RXD [3:0])	Description
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F

Table 32: 4B/5B Code-Group Table (Cont.)

PCS Code Group[4:0]	Symbol Name	MII (TXD/RXD [3:0])	Description
Idle and Control Code			
11111	I	0000	Inter-Packet Idle; used as inter-stream fill code.
11000	J	0101	Start of stream delimiter, part 1 of 2; always use in pair with K symbol.
10001	K	0101	Start of stream delimiter, part 2 of 2; always use in pair with J symbol.
01101	T	Undefined	End of stream delimiter, part 1 of 2; always use in pair with R symbol.
00111	R	Undefined	End of stream delimiter, part 2 of 2; always use in pair with T symbol.
Invalid Code			
00100	H	Undefined	Transmit Error; used to send HALT code group
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

Table 33: SMI Read/Write Sequence

SMI Read/Write Sequence								
	Pream (32 bits)	Start (2 bits)	OpCode (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	TurnAround (2 bits)	Data (16 bits)	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	D…D	Z
Write	1…1	01	01	AAAAA	RRRRR	10	D…D	Z

Table 34: LED Configurations

Mode	*LEDDPX*	*LEDACT*	*LEDSPD*
10M Link		ON	OFF
10M HDX Transmit	OFF	TOGGLE	OFF
10M HDX Receive	OFF	TOGGLE	OFF
10 HDX Collision	ON during collision	TOGGLE	OFF
10M FDX Transmit	ON	TOGGLE	OFF
10M FDX Receive	ON	TOGGLE	OFF
100M Link		ON	ON
100M HDX Transmit	OFF	TOGGLE	ON
100M HDX Receive	OFF	TOGGLE	ON
100 HDX Collision	ON during collision	TOGGLE	ON
100M FDX Transmit	ON	TOGGLE	ON
100M FDX Receive	ON	TOGGLE	ON

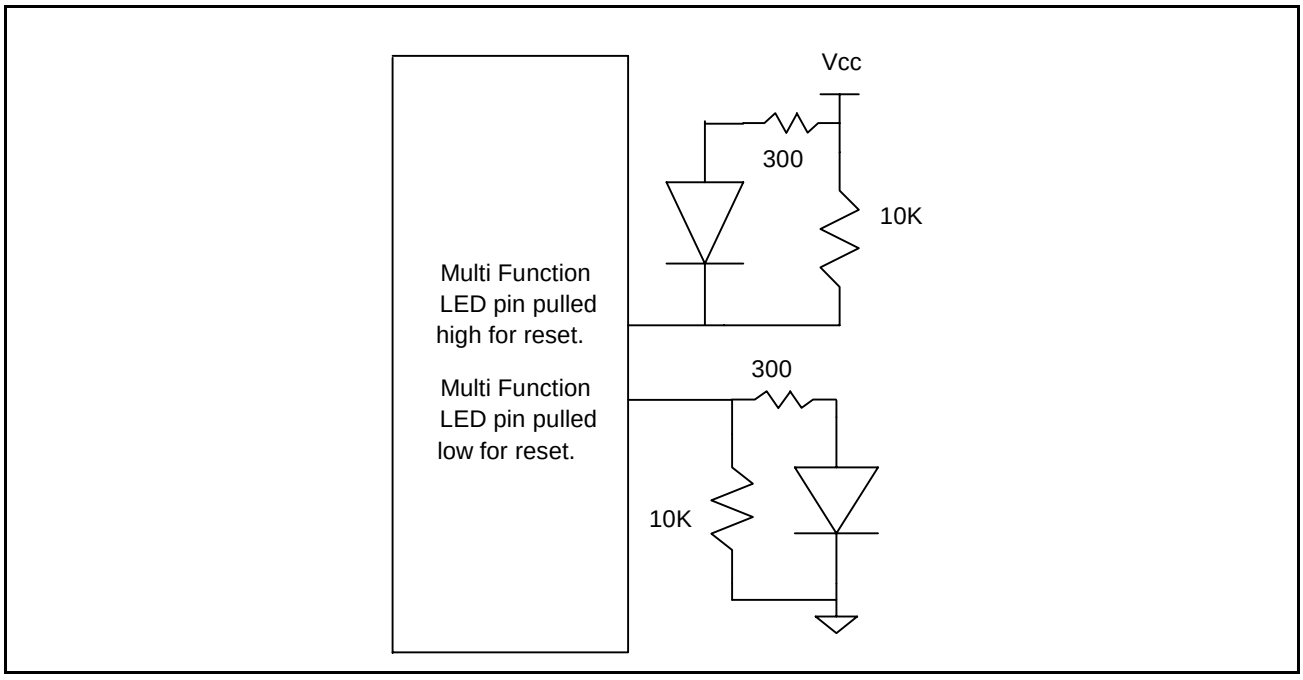

Figure 3: LED Configurations

Section 4: Electrical Characteristics

Note **The following electrical characteristics are design goal rather than characterized numbers.**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature.....-40°C to +125°C

Vcc Supply Referenced to GND..... -0.25V to +2.75V

Digital Input Voltage..... -0.33V to +3.63V

DC Output Voltage.....-0.25V to +2.75V

OPERATING RANGE

Operating Temperature (Ta)..... 0°C to +70°C

Vcc Supply Voltage Range (Vcc).....2.375V to 2.625V

Table 35: DC Characteristics (0°C < Ta < 70°C, 2.375V < V_{CC} < 2.625V, unless otherwise noted)

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Power Supply Current for all 4 ports	Icc	10 BASE-T, idle 10 BASE-T, normal activity traffic ~50% util. 10 BASE-T, Peak continuous 100% utilization 100 BASE-TX 10/100 BASE-TX, low-power without cable Auto-Negotiation Power down		95 290 480 348 75 68	115 310 500 360 85 80 1	mA
Maximum Power Consumption for all 4 ports	P_{MAX}				1.35	W
TTL Input High Voltage	V_{ih}		2.0			V
TTL Input Low Voltage	V_{il}				0.8	V
TTL Input Current	Iin	Vcc = 2.625V	-10		10	µA
TTL Input Capacitance	CIin			10		pF
Output High Voltage	Voh	2.375V ≤ Vcc ≤ 2.625V, I_{oH} = 8 mA	Vcc-0.4			V
Output Low Voltage	Vol	2.375V ≤ Vcc ≤ 2.625V, I_{oL} = 8 mA			0.4	V

Table 35: DC Characteristics ($0^oC < Ta < 70^oC$, $2.375V < V_{CC} < 2.625V$, unless otherwise noted) (Cont.)

Parameter	SYM	Conditions	Min	Typ	Max	Units
Output Transition Time	T_r, T_f.	2.375V ≤ Vcc ≤ 2.625V, 20pf Loading, 0°V~70°V	1.5		6	ns
LED Output Current	I_{OH}				9	mA
Output Tristate Leakage Current	|Ioz|				10	µA
Transmitter, 100BASE-TX (1:1 Transformer Ratio)						
TX± Output Current High	I_{OH}				40	mA
TX± Output Current Low	I_{OL}		0			µA
Transmitter, 10BASE-T (1:1 Transformer Ratio)						
TX± Output Current High	I_{OH}				100	mA
TX± Output Current Low	I_{OL}		0			µA

Table 36: AC Characteristics ($0^oC < Ta < 70^oC$, $2.375V < V_{CC} < 2.625V$, unless otherwise noted)

Parameter	SYM	Conditions	Min	Typ	Max	Units
Transmitter, 100BASE-TX						
Differential Output Voltage, peak-to-peak	V_{OD}	50 Ω from each output to Vcc, Best-fit over 14 bit times	1.9	2.0	2.1	V
Differential Output Voltage Symmetry	V_{OS}	50 Ω from each output to Vcc, |Vp+|/|Vp-|	0.98		1.02	mV
Differential Output Over-shoot	V_{OO}	Percent of Vp+ or Vp-			5	%
Rise/Fall time	t_r, t_f	10 - 90% of Vp+ or Vp-	3	4	5	ns
Duty Cycle Distortion		Deviation from best-fit time-grid, 010101 ... Sequence			±250	ps
Timing jitter		Unscrambled Idle			1.4	ns
Transmitter, 10BASE-T						
Differential Output Voltage, peak-to-peak	V_{OD}	50 Ω from each output to Vcc, all pattern	4.5	5	5.5	V
THD	V_{HD}	dB below fundamental, all ones data	27			dB
Start-of-idle Pulse Width					350	ns

Table 37: Digital Timing Characteristics (0^oC <Ta <70^oC, 2.375V < V_{dd} < 2.625V)

Parameter	SYM	Conditions	Min	Typ	Max	Units
100BASE-TX Transmit System Timing						
Active TX_EN Sampled to first bit of “J” on MDI output				4	18	bits
Inactive TX_EN Sampled to first bit of “T” on MDI output				4		bits
TX Propagation Delay	t_{TXpd}	From TXD[1:0] to TXOP/N		4		bits
100BASE-TX Receive System Timing						
First bit of “J” on MDI input to CRS-DV assert				14	22	bits
First bit of “T” on MDI input to CRS-DV de-assert				20		bits
RX Propagation Delay	t_{RXpd}	From RXIP/N to RDTX[1:0]		12		bits
RST Low Period	t_{RSTI}		10			µs

Table 38: Digital Timing Characteristics (0^oC <Ta <70^oC, 2.375V < V_{dd} < 2.625V)

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
10BASE-T System Timing						
Carrier Sense Turn-on Delay	t_{CSON}				300	ns
Carrier Sense Turn-off Delay	t_{CSOFF}				160	ns
100BASE-TX System Timing						
Setup time relative to the rising edge of REFCLK.			4	-	-	ns
Hold time relative to the rising edge of REFCLK.			2	-	-	ns
RXD data output delay relative to rising edge of REFCLK			-	-	14	ns
10BASE-T System Timing						
Setup time relative to the rising edge of REFCLK.			4	-	-	ns
Hold time relative to the rising edge of REFCLK.			2	-	-	ns
RXD data output delay relative to rising edge of REFCLK			-	-	14	ns

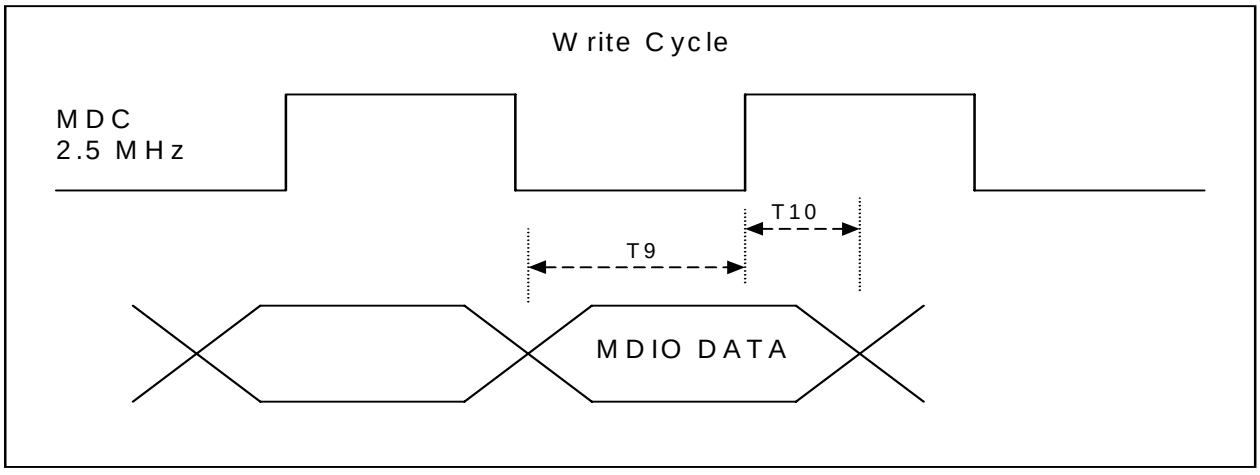

Figure 4: MDC/MDIO Timing Diagram 1

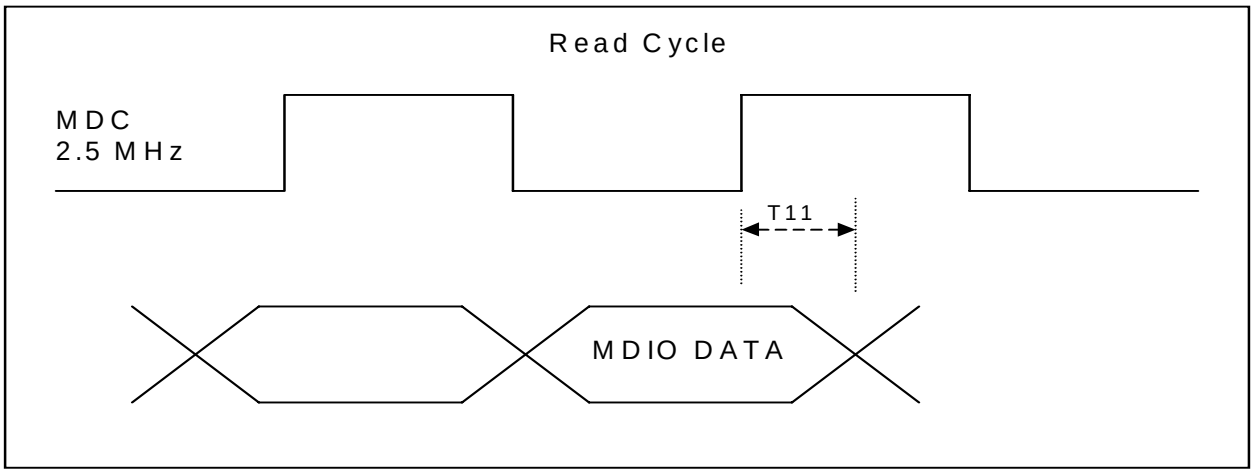

Figure 5: MDC/MDIO Timing Diagram 2

Table 39: MDC/MDIO Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Unit*
Setup time relative to the rising edge of MDC.	T9	MDC is a 2.5 MHz output clock from the MAC controller.	10	-	-	ns
Hold time relative to the rising edge of MDC.	T10	MDC is a 2.5 MHz output clock from the MAC controller.	-	-	10	ns
Output delay relative to the rising edge of MDC.	T11	MDC is a 2.5 MHz output clock from the MAC controller.	0	20	300	ns

RECOMMENDED TERMINATION

Contact Altima Communications Inc. for the latest component value recommendations.

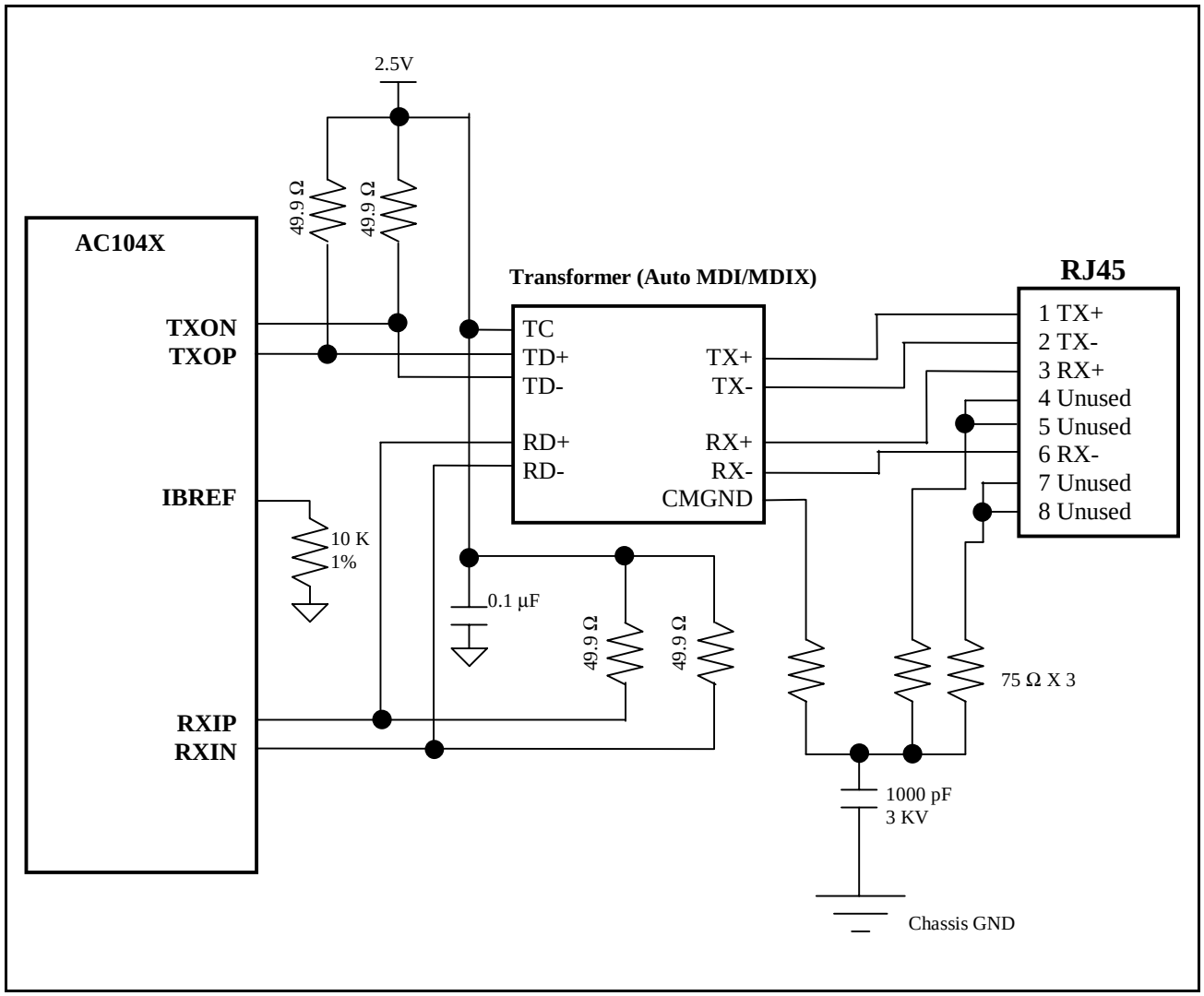

Figure 6: Termination Figure

POWER AND GROUND FILTERING

Contact Altima Communications Inc. for the latest component value recommendations.

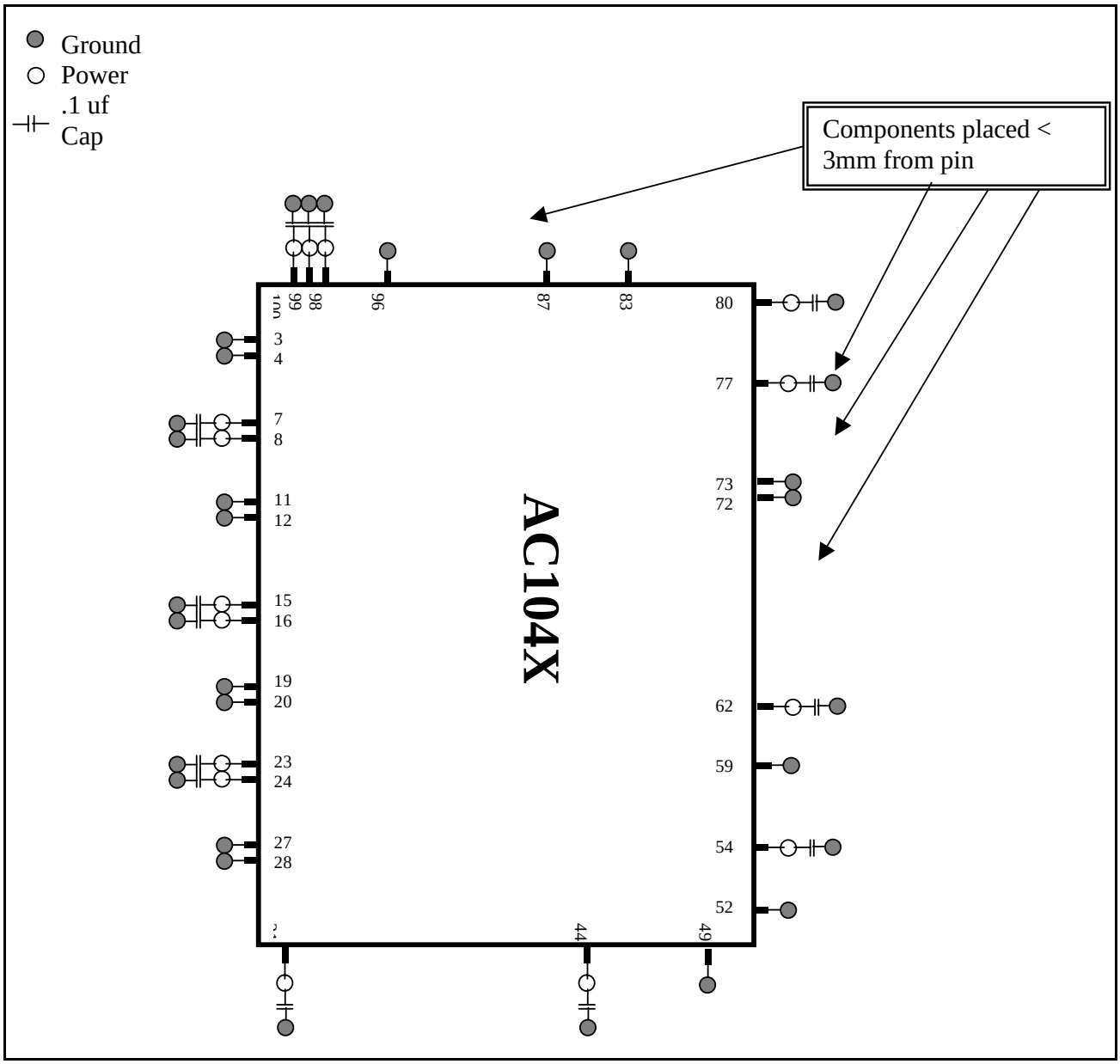

Figure 7: Power and Ground

Section 5: Package Drawing

Table 40: Package Drawing

N	A	A1	A2	B	D	D1	E	E1	e	L	L1
100	3.40 max	0.25 min	2.70 ± 0.2	0.3 ± 0.1	23.20 ± 0.25	20.00 ± 0.10	17.20 ± 0.25	14.00 ± 0.10	0.65	0.88 ± 0.2	1.60 ± 0.12

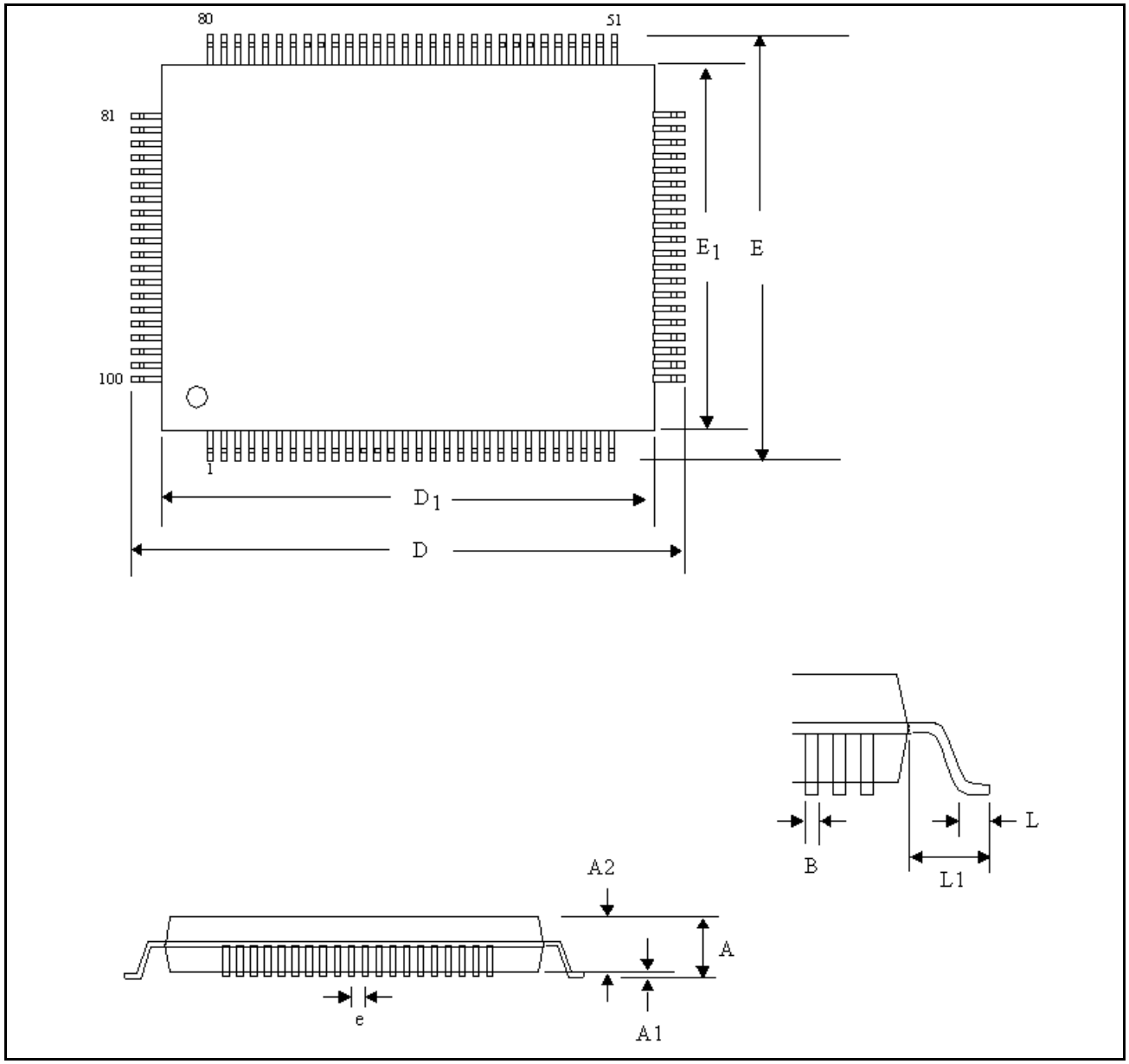

Figure 8: Package Drawing

Section 6: Packaging Thermal Characteristics

100PQFP PACKAGE

Table 41: 100PQFP Package Thermal Characteristics

Airflow (feet per minute)	*0*	*100*	*200*	*400*	*600*
Theta JA (°C/W)	T9	10	-	-	ns

Theta JC (°C/W) at max junction temperature of 125°C.

Section 7: Ordering Information

Part Number	*Package*	*Ambient Temperature*
AC104XKQM	100-pin PQFP	0°C to 70°C

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