SBAS154C – OCTOBER 2000 – REVISED OCTOBER 2002

14-Bit, 10MSPS Self-Calibrating ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SELF-CALIBRATING
- HIGH SFDR: 85dB at NYQUIST
- HIGH SNR: 76dB
- LOW POWER: 250mW
- DIFFERENTIAL OR SINGLE-ENDED INPUTS
- +3V/+5V LOGIC I/O COMPATIBLE
- FLEXIBLE INPUT RANGE
- OVER-RANGE INDICATOR
- INTERNAL OR EXTERNAL REFERENCE

APPLICATIONS

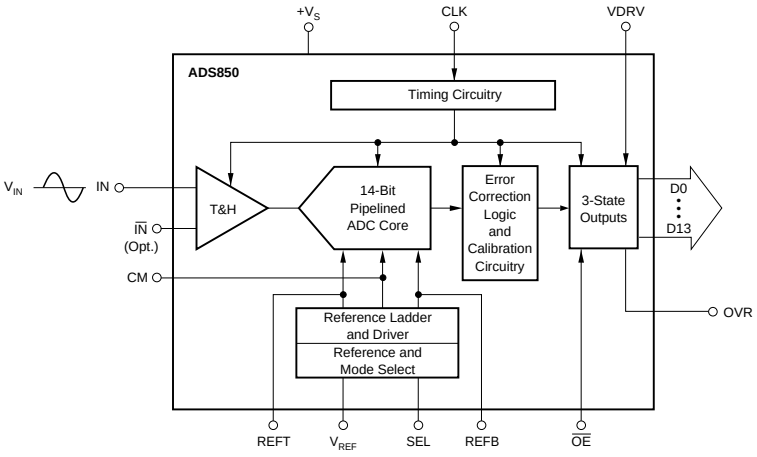
- IF AND BASEBAND DIGITIZATION
- CCD IMAGING SCANNERS
- TEST INSTRUMENTATION
- IR IMAGING

DESCRIPTION

The ADS850 is a high dynamic range, 14-bit Analog-to-Digital Converter (ADC) that utilizes a fully differential input, allowing for either single-ended or differential input interface over varying input spans. This converter features digital error correction techniques ensuring 14-bit linearity and a calibration procedure that corrects for capacitor and gain mismatches. The ADS850 also includes a high-bandwidth track-and-hold that provides excellent spurious performance up to and beyond the Nyquist rate.

The ADS850 provides an internal reference that can be programmed for a 2Vp-p input range for the best spurious performance and ease of driving. Alternatively, the 4Vp-p input range can be used for the lowest input referred noise, offering superior signal-to-noise performance for imaging applications. There is also the capability to set the range between 2Vp-p and 4Vp-p, or to use an external reference. The ADS850 also provides an over-range indicator flag to indicate if the input has exceeded the full-scale input range of the converter.

The low distortion and high signal-to-noise performance provide the extra margin needed for communications, imaging, and test instrumentation applications. The ADS850 is available in a TQFP-48 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	(–0.3V) to ($+V_S$ +0.3V)
Logic Input	(–0.3V) to ($+V_S$ +0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DEMO BOARD ORDERING INFORMATION

PRODUCT	DEMO BOARD
ADS850Y	ADS850Y-EVM

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS850Y	TQFP-48	PFB	–40°C to +85°C	ADS850Y	ADS850Y/250	Tape and Reel, 250
"	"	"	"	"	ADS850Y/2K	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, specified differential input range = 1.5V to 3.5V, internal reference input, sampling rate = 10MSPS after calibration, and V_{REF} = 2V, unless otherwise specified.

		ADS850Y			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESOLUTION			14		Bits
SPECIFIED TEMPERATURE RANGE			–40 to +85		°C
CONVERSION CHARACTERISTICS					
Sample Rate		10k		10M	Samples/s
Data Latency			7		Clk Cycles
ANALOG INPUT					
Single-Ended Input Range	V_{REF} = 1.0	1.5		3.5	V
	V_{REF} = 2.0	0.5		4.5	V
Differential Input Range	V_{REF} = 2.0	1.5		3.5	V
Common-Mode Voltage			2.5		V
			1		V
Input Capacitance			20		pF
Analog Input Bandwidth	–3dBFS Input		270		MHz
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (Largest Code Error)					
f = 4.8MHz			±0.75	±1.0	LSB
No Missing Codes			Tested		
Spurious-Free Dynamic Range[1]					
f = 4.8MHz (–1dB input)	4Vp-p	75	85		dBFS[2]
f = 4.8MHz (–1dB input)	2Vp-p		82		dBFS
Signal-to-Noise Ratio (SNR)					
f = 4.8MHz (–1dB input)	4Vp-p	71	76		dBFS
f = 4.8MHz (–1dB input)	2Vp-p		73		dBFS
Signal-to-(Noise + Distortion) (SINAD)					
f = 4.8MHz (–1dB input)	4Vp-p	70	75		dBFS
f = 4.8MHz (–1dB input)	2Vp-p		72		dBFS
Effective Number of Bits at 4.8MHz[3]			12.2		Bits
Integral Nonlinearity Error					
f = 4.8MHz			±2.5	±5.0	LSB
Aperture Delay Time			1		ns
Aperture Jitter			4		ps rms
Overvoltage Recovery Time	1.5 • FS Input		2		ns
Full-Scale Step Acquisition Time			50		ns

ELECTRICAL CHARACTERISTICS (Cont.)

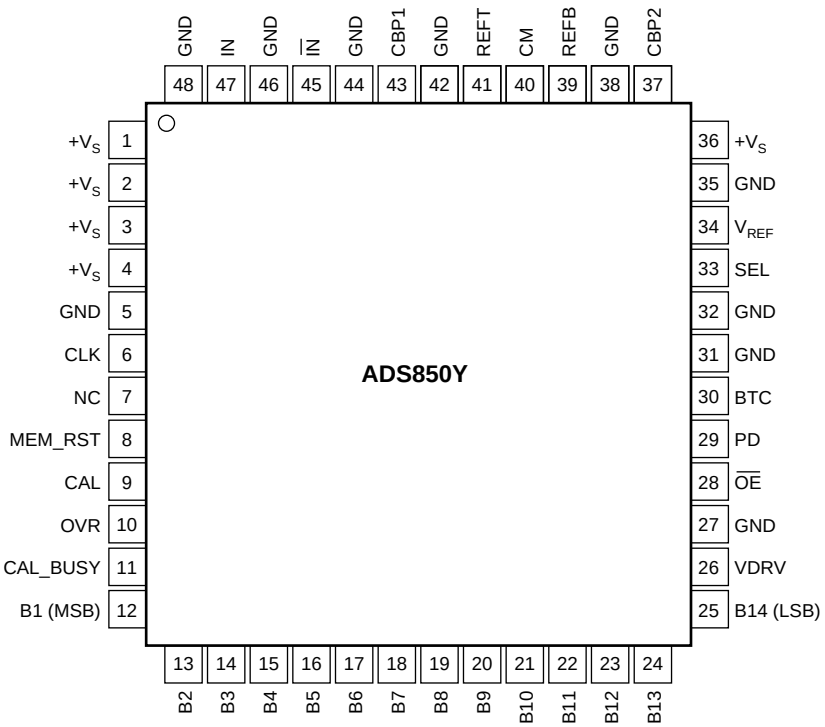
At T_A = full specified temperature range, V_S = +5V, specified differential input range = 1.5V to 3.5V, internal reference input, sampling rate = 10MSPS after calibration, and V_{REF} = 2V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS850Y MIN	ADS850Y TYP	ADS850Y MAX	UNITS
DIGITAL INPUTS					
Logic Family			+3V/+5V Logic Compatible CMOS		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current (V_{IN} = 5V)[4]				100	µA
Low Level Input Current (V_{IN} = 0V)				±10	µA
High Level Input Voltage		+2.0			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			+3V/+5V Logic Compatible CMOS		V
Logic Coding			Straight Offset Binary		
Low Output Voltage	(I_{OL} = 50µA)			0.1	V
Low Output Voltage	(I_{OL} = 1.6mA)			0.4	V
High Output Voltage	(I_{OH} = 50µA)	+4.5			V
High Output Voltage	(I_{OH} = 0.5mA)	+2.4			V
3-State Enable Time	$\overline{OE}$ = LOW		20	40	ns
3-State Disable Time	$\overline{OE}$ = HIGH		2	10	ns
Output Capacitance			5		pF
ACCURACY (4Vp-p Input Range)					
Zero Error (Referred to –FS)	At 25°C		±0.2		%FS
Zero Error Drift (Referred to –FS)			±5		ppm/°C
Gain Error[5]	At 25°C		±0.7		%FS
Gain Error Drift[5]			±15		ppm/°C
Gain Error[6]	At 25°C		±0.042		%FS
Gain Error Drift[6]			±15		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%		82		dB
Reference Input Resistance			1.6		kΩ
Internal Voltage Reference Tolerance (V_{REF} = 2.0V)[7]	At 25°C		±13.5mV		mV
Internal Voltage Reference Tolerance (V_{REF} = 1.0V)[7]	At 25°C		±6mV		mV
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.7	+5.0	+5.3	V
Supply Voltage: VDRV	Operating	+2.7		+5.3	V
Supply Current: $+I_S$	Operating		53		mA
Power Dissipation VDRV = 3V	External Reference		240		mW
VDRV = 5V	External Reference		245		mW
VDRV = 3V	Internal Reference		250	275	mW
VDRV = 5V	Internal Reference		255		mW
	Power-Down		20		mW
Thermal Resistance, θ_{JA}					
TQFP-48			56.5		°C/W

NOTES: (1) Spurious-Free Dynamic Range refers to the difference in magnitude between the fundamental and the next largest harmonic. (2) dBFS means dB relative to full scale. (3) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (4) Internal 50kΩ pull-down resistor. (5) Includes internal reference. (6) Excludes internal reference. (7) Typical reference tolerance based on ±1 sigma of distribution.

PIN CONFIGURATION

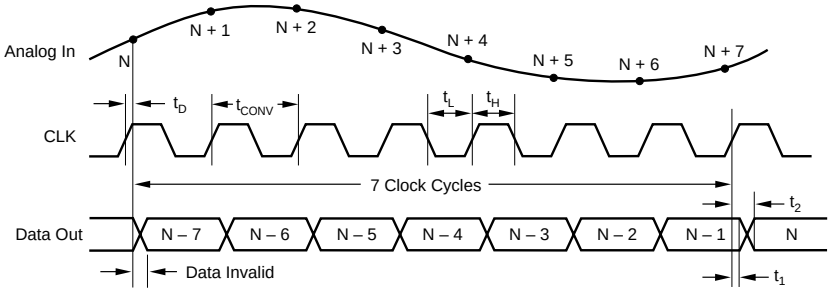
Top View **TQFP**



PIN DESCRIPTIONS

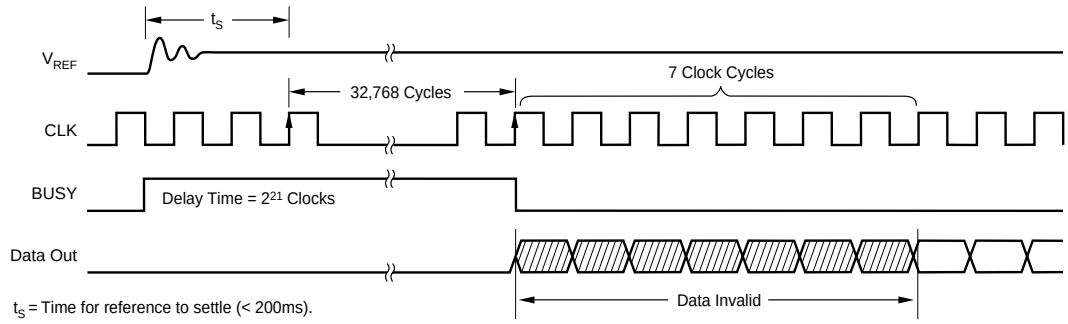
PIN	I/O	DESIGNATOR	DESCRIPTION	PIN	I/O	DESIGNATOR	DESCRIPTION
1		$+V_S$	+5V Supply	27		GND	Ground
2		$+V_S$	+5V Supply	28	I	$\overline{OE}$	Output Enable: HI = High Impedance;
3		$+V_S$	+5V Supply				LO = Normal Operation (50kΩ Internal
4		$+V_S$	+5V Supply				Pull-Down Resistor)
5		GND	Ground	29	I	PD	Power Down: HI = Power Down; LO = Normal
6	I	CLK	Convert Clock Input				Operation (50kΩ Internal Pull-Down Resistor)
7		NC	No Connection	30	I	BTC	HI = Binary Two's Complement (BTC);
8	I	MEM_RST	Memory Reset. When pulsed HIGH,				LO = Straight Offset Binary (SOB)
			resets memory to zero. Not intended as	31		GND	Ground
			a function pin, so should be perma-	32		GND	Ground
			nently tied to ground.	33		SEL	Input Range Select
9	I	CAL	When Pulsed High, puts ADC into Cali-	34	I/O	V_{REF}	Reference Voltage Select
			bration Mode (2 clock cycles).	35		GND	Ground
10		OVR	Over Range Indicator	36		$+V_S$	+5V Supply
11		CAL_BUSY	Indicates in Calibration Mode.	37		CBP2	Calibration Reference Bypass 2 (0.1µF ce-
12	O	B1 (MSB)	Data Bit 1 (D13) (MSB)				ramic capacitor recommended for decou-
13	O	B2	Data Bit 2 (D12)				pling.)
14	O	B3	Data Bit 3 (D11)	38		GND	Ground
15	O	B4	Data Bit 4 (D10)	39	I/O	REFB	Bottom Reference Voltage Bypass
16	O	B5	Data Bit 5 (D9)	40	O	CM	Common-Mode Voltage (mid-scale). Not in-
17	O	B6	Data Bit 6 (D8)				tended for driving a load.
18	O	B7	Data Bit 7 (D7)	41	I/O	REFT	Top Reference Voltage Bypass
19	O	B8	Data Bit 8 (D6)	42		GND	Ground
20	O	B9	Data Bit 9 (D5)	43		CBP1	Calibration Reference Bypass 1 (0.1µF ce-
21	O	B10	Data Bit 10 (D4)				ramic capacitor recommended for decou-
22	O	B11	Data Bit 11 (D3)				pling.)
23	O	B12	Data Bit 12 (D2)	44		GND	Ground
24	O	B13	Data Bit 13 (D1)	45	I	$\overline{IN}$	Complementary Analog Input (–)
25	O	B14 (LSB)	Data Bit 14 (D0) (LSB)	46		GND	Ground
26		VDRV	Output Driver Voltage	47	I	IN	Analog Input (+)
				48		GND	Ground

TIMING DIAGRAMS

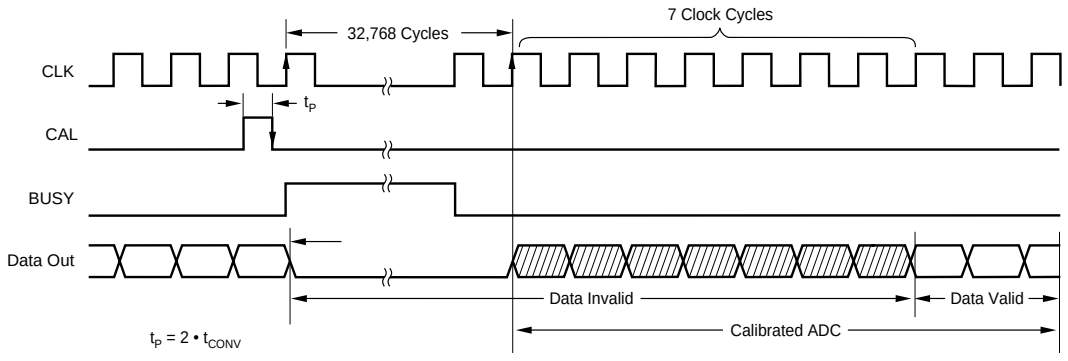


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	100		100µs	ns
t_L	Clock Pulse LOW	48	$t_{CONV}/2$		ns
t_H	Clock Pulse HIGH	48	$t_{CONV}/2$		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

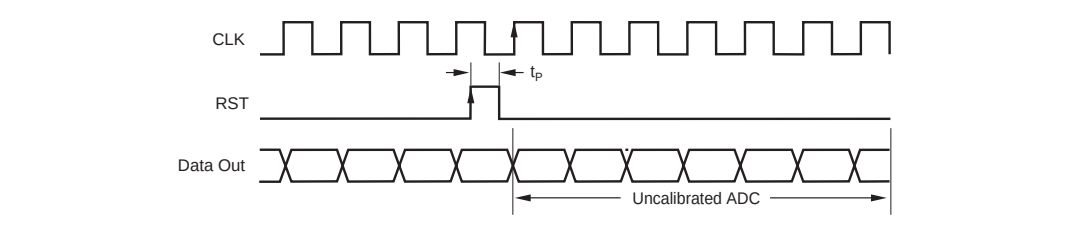
TIMING DIAGRAM 1. Pipeline Delay Timing.



TIMING DIAGRAM 2. Power-On Calibration Mode Timing.



TIMING DIAGRAM 3. Calibration-On-Demand Mode Timing.

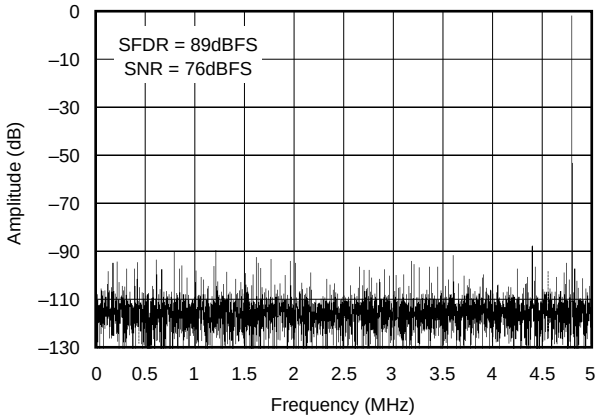


TIMING DIAGRAM 4. Reset Mode Timing.

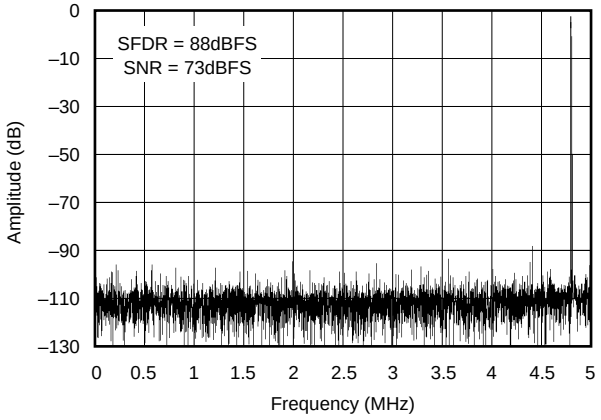
TYPICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, specified input range = 1.5V to 3.5V, differential internal reference input and sampling rate = 10MSPS after calibration, V_{REF} = 2V, –1dB input, unless otherwise specified.

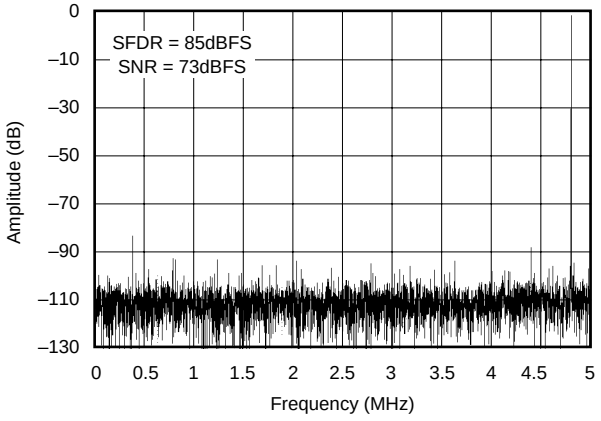
SPECTRAL PERFORMANCE
(4Vp-p, Differential, f_{IN} = 4.8MHz)



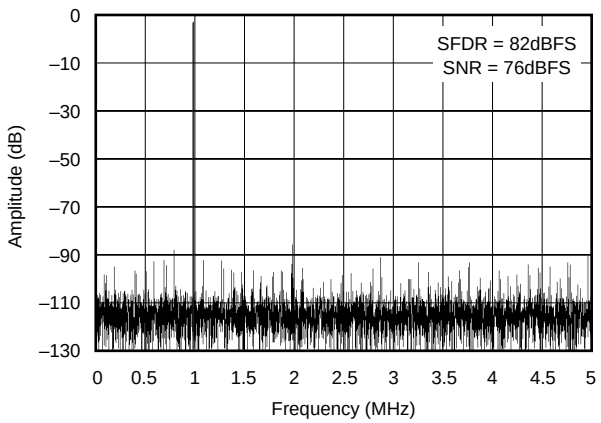
SPECTRAL PERFORMANCE
(2Vp-p, Differential, f_{IN} = 4.8MHz)



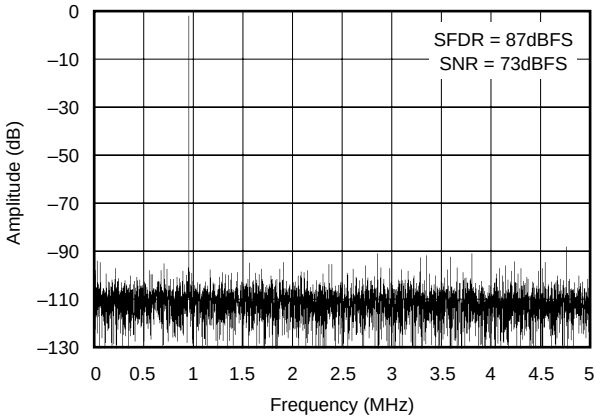
SPECTRAL PERFORMANCE
(2Vp-p, Single-Ended, f_{IN} = 4.8MHz)



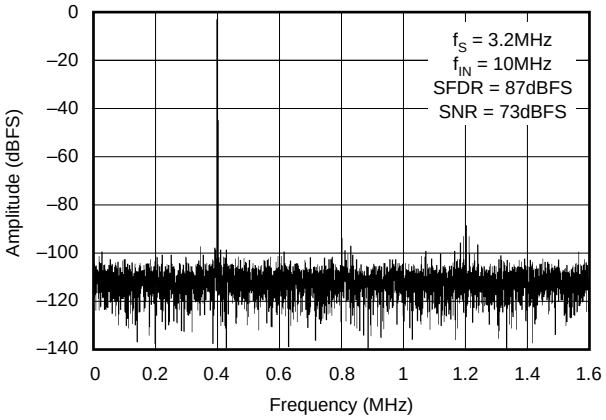
SPECTRAL PERFORMANCE
(4Vp-p, Differential, f_{IN} = 1MHz)



SPECTRAL PERFORMANCE
(2Vp-p, Single-Ended, f_{IN} = 1MHz)



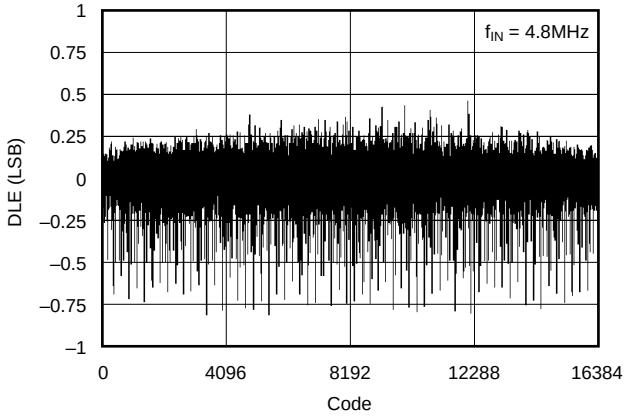
UNDERSAMPLING
(Differential, 4Vp-p)



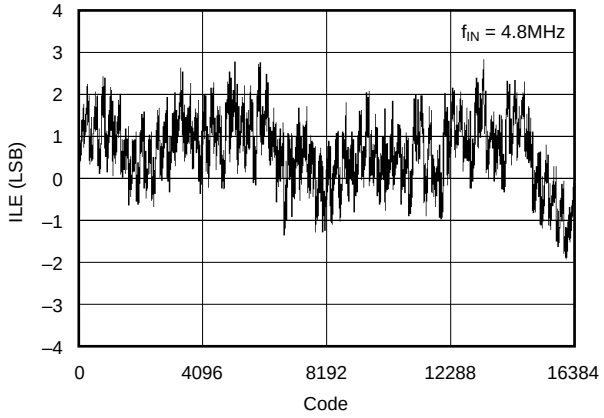
TYPICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, specified input range = 1.5V to 3.5V, differential internal reference input and sampling rate = 10MSPS after calibration, V_{REF} = 2V, –1dB input, unless otherwise specified.

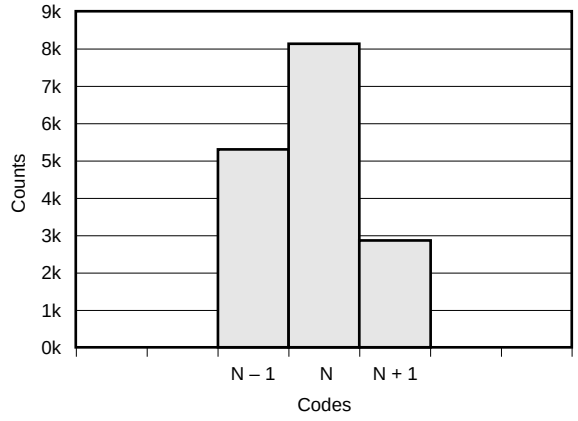
DIFFERENTIAL LINEARITY ERROR



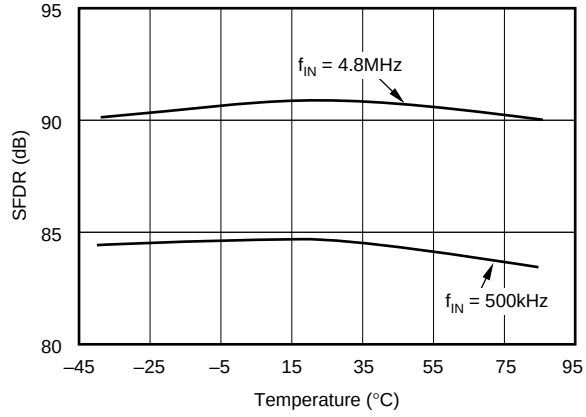
INTEGRAL LINEARITY ERROR



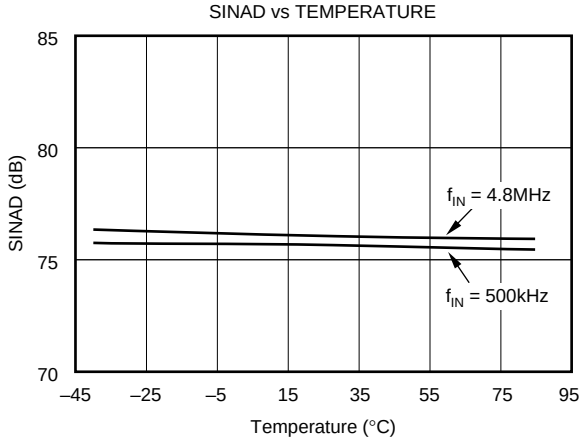
OUTPUT NOISE HISTOGRAM
(4Vp-p)



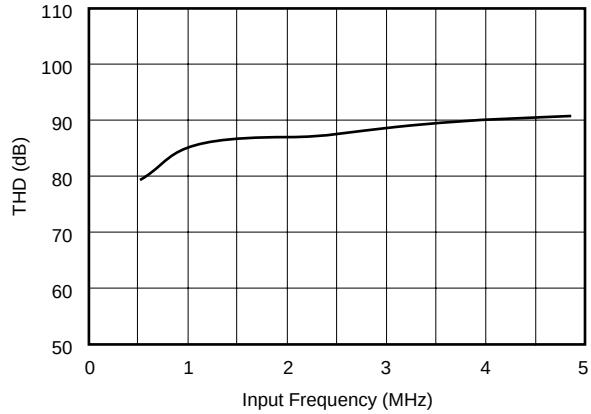
SFDR vs TEMPERATURE



SINAD vs TEMPERATURE



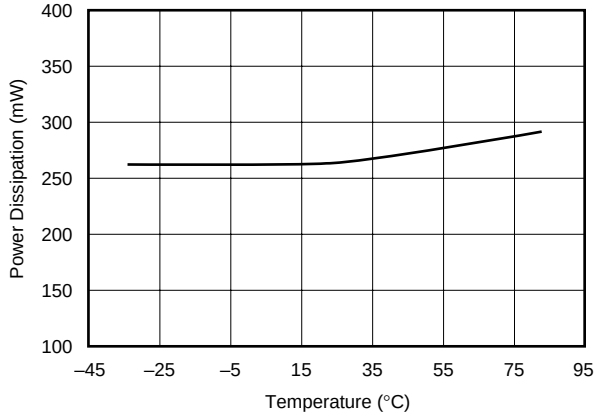
THD vs INPUT FREQUENCY



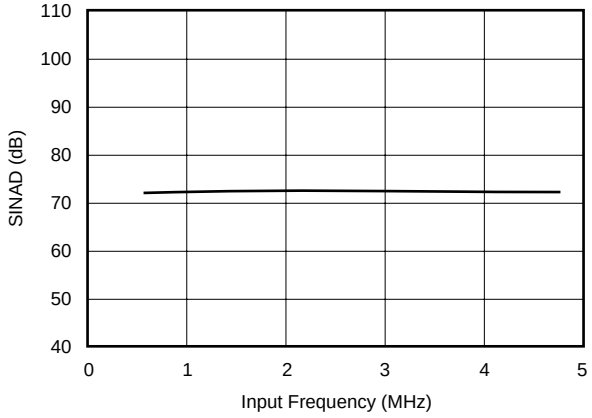
TYPICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, specified input range = 1.5V to 3.5V, differential internal reference input and sampling rate = 10MSPS after calibration, V_{REF} = 2V, –1dB input, unless otherwise specified.

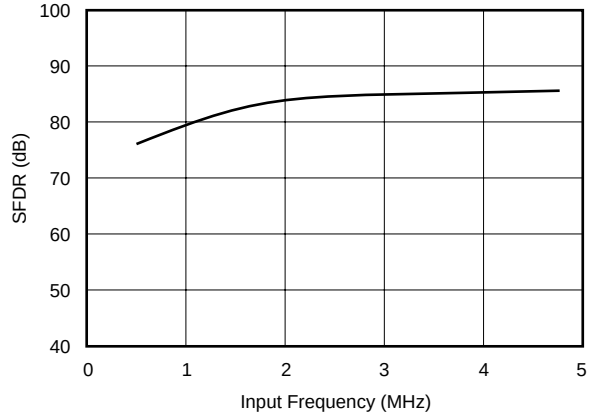
POWER DISSIPATION vs TEMPERATURE



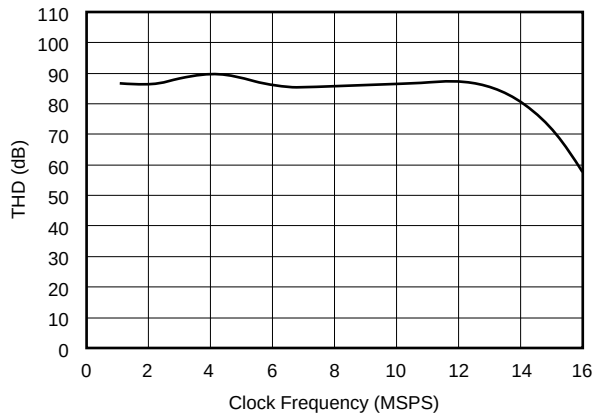
SINAD vs INPUT FREQUENCY



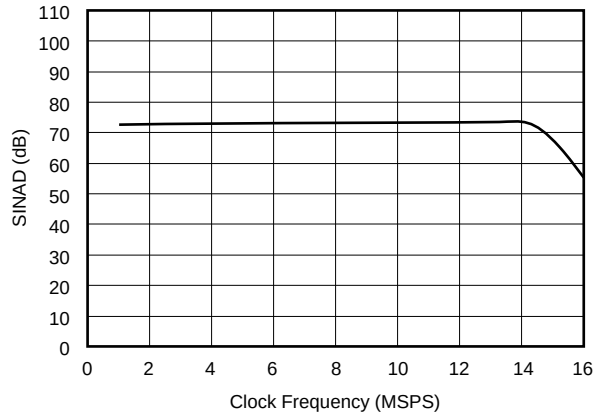
SFDR vs INPUT FREQUENCY



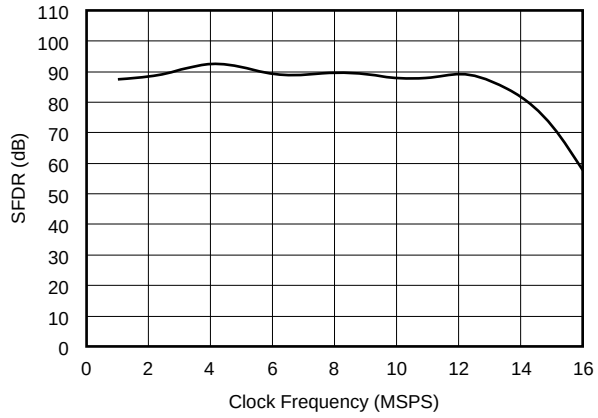
THD vs CLOCK FREQUENCY



SINAD vs CLOCK FREQUENCY

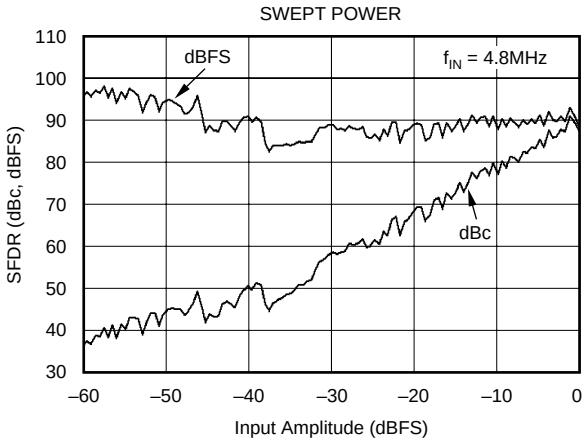


SFDR vs CLOCK FREQUENCY



TYPICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, specified input range = 1.5V to 3.5V, differential internal reference input and sampling rate = 10MSPS after calibration, V_{REF} = 2V, –1dB input, unless otherwise specified.



APPLICATION INFORMATION

DRIVING THE ANALOG INPUT

The ADS850 allows its analog inputs to be driven either single-ended or differentially. The focus of the following discussion is on the single-ended configuration.

CALIBRATION PROCEDURE

The calibration procedure (CAL) is started by a positive pulse, with a minimum width of 2 clock cycles. Once calibration is initiated, the clock must operate continuously and the power supplies and references must remain stable. The calibration registers are reset on the rising edge of the CAL signal. The actual calibration procedure begins at the falling edge of the CAL signal. Calibration is completed at the end of 32,775 cycles at 10MSPS, CAL = 3.28ms (see Timing Diagram 3 on page 5). During calibration, the CAL_BUSY signal stays HIGH and the digital output pins of the ADC are forced to zero. Also, during calibration, the inputs (IN and $\overline{IN}$) are disabled. When the calibration procedure is complete, the CAL_BUSY goes LOW. Valid data appears at the output seven cycles later or after a total of 32,775 clock cycles. If there are any changes to the clock or the temperature changes more than ±20°C, the ADC should be re-calibrated to maintain performance.

At power-on (see Timing Diagram 2 on page 5), the ADC calibrates itself. The power-on delay, t_S, is the time it takes for the reference voltage to settle. Once the clock starts, the power-on delay operates for 2^{21} clock cycles. Bypass capacitors should be selected to allow the reference to settle within 200ms. If the system is noisy or external references require a longer settling time, a CAL pulse may be required.

AC-COUPLED INPUT CONFIGURATION

See Figure 1 for the circuit example of the most common interface configuration for the ADS850. With the V_{REF} pin connected to the SEL pin, the full-scale input range is defined to be 2Vp-p. This signal is ac-coupled in single-ended form to the ADS850 using the low distortion voltage-feedback amplifier OPA642. As is generally necessary for single-supply components, operating the ADS850 with a full-scale input signal swing requires a level-shift of the amplifier's zero-centered analog signal to comply with the ADC's input range requirements. Using a DC blocking capacitor between the output of the driving amplifier and the converter's input, a simple level-shifting scheme can be implemented. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3V and +2V, respectively. Here, two resistor pairs of 2 • 2kΩ are used to create a common-mode voltage of approximately +2.5V to bias the inputs of the ADS850 (IN, $\overline{IN}$) to the required DC voltage.

An advantage of ac-coupling is that the driving amplifier still operates with a ground-based signal swing. This will keep the distortion performance at its optimum since the signal swing stays centered within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. Consider using the inverting gain configuration to eliminate CMR induced errors of the amplifier. The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS850 will be beneficial in almost all interface configurations. This will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor together with the 100pF capacitor establish a passive low-pass filter, limiting the bandwidth for the wideband noise, thus help improving the SNR performance.

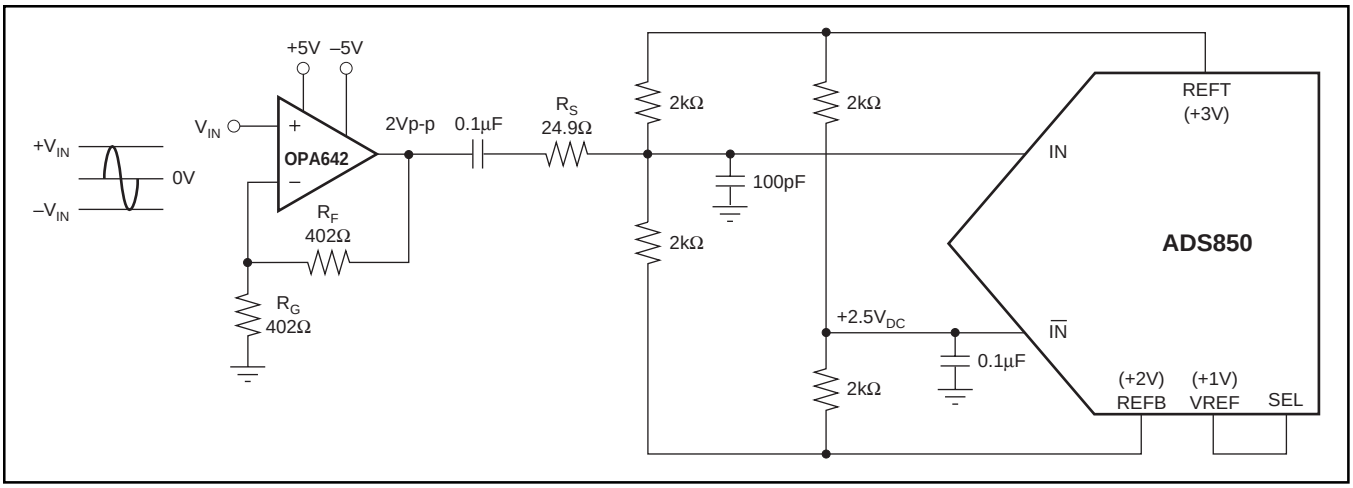


FIGURE 1. AC-Coupled Input Configuration for 2Vp-p Input Swing and Common-Mode Voltage at +2.5V Derived from Internal Top and Bottom Reference.

DC-COUPLED WITHOUT LEVEL SHIFT

In some applications the analog input signal may already be biased at a level which complies with the selected input range and reference level of the ADS850. In this case, it is only necessary to provide an adequately low source impedance to the selected input, IN or $\overline{IN}$. Always consider wideband op amps since their output impedance will stay low over a wide range of frequencies. For those applications requiring the driving amplifier to provide a signal amplification, with a gain ≥ 3, consider using the decompensated voltage feedback op amp OPA686.

DC-COUPLED WITH LEVEL SHIFT

Several applications may require that the bandwidth of the signal path include DC, in which case the signal has to be DC-coupled to the ADC. In order to accomplish this, the interface circuit has to provide a DC-level shift. The circuit shown in Figure 2 employs an op amp, OPA681, to sum the ground centered input signal with a required DC offset. The ADS850 typically operates with a +2.5V common-mode voltage, which is established at the center tap of the ladder and connected to the $\overline{IN}$ input of the converter. The OPA681 operates in inverting configuration. Here resistors R_1 and R_2 set the DC-bias level for the OPA691. Because of the op amp's noise gain of +2V/V, assuming $R_F = R_{IN}$, the DC offset voltage applied to its noninverting input has to be divided down to +1.25V, resulting in a DC output voltage of +2.5V. DC voltage differences between the IN and $\overline{IN}$ inputs of the ADS850 effectively will produce an offset, which can be corrected for by adjusting the values of resistors R_1 and R_2. The bias current of the op amp may also result in an undesired offset. The selection criteria of the appropriate op amp should include the input bias current, output voltage swing, distortion and noise specification. Note that in this example the overall signal phase is inverted. To re-establish the original signal polarity, it is always possible to interchange the IN and $\overline{IN}$ connections.

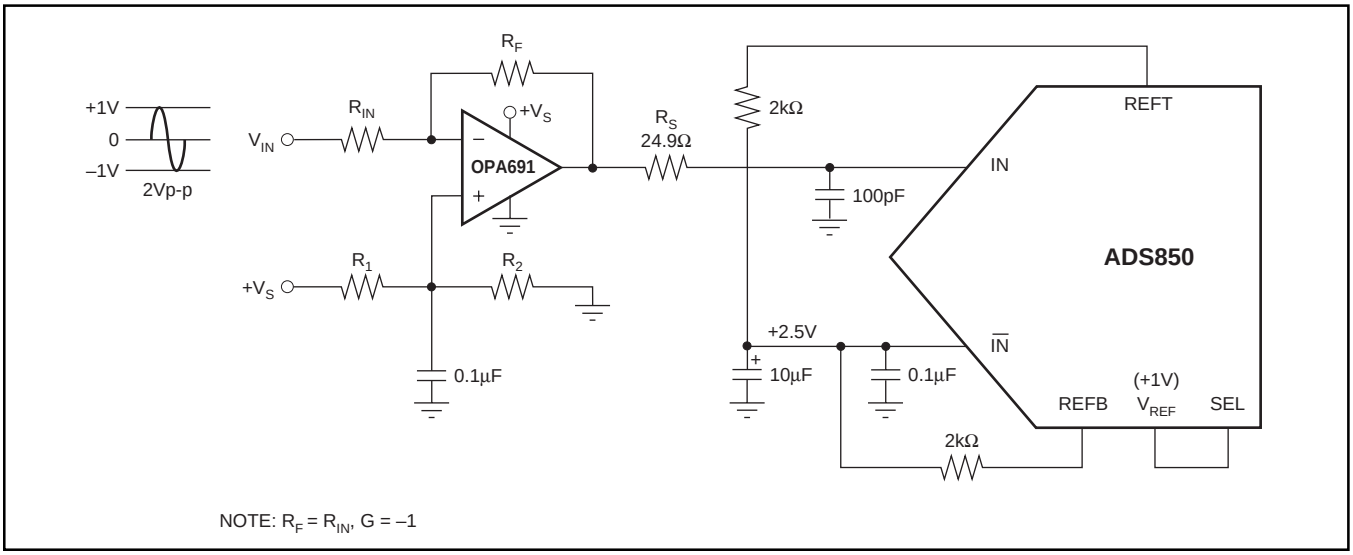


FIGURE 2. DC-Coupled, Single-Ended Input Configuration with DC-level Shift.

SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (TRANSFORMER COUPLED)

In order to select the best suited interface circuit for the ADS850, the performance requirements must be known. If an ac-coupled input is needed for a particular application, the next step is to determine the method of applying the signal; either single-ended or differentially. The differential input configuration may provide a noticeable advantage of achieving good SFDR performance based on the fact that in the differential mode, the signal swing can be reduced to half of the swing required for single-ended drive. Secondly, by driving the ADS850 differentially, the even-order harmonics will be reduced. Figure 3 shows the schematic for the suggested transformer-coupled interface circuit. The resistor across the secondary side (R_T) should be set to get an input impedance match (e.g., $R_T = n^2 \bullet R_G$).

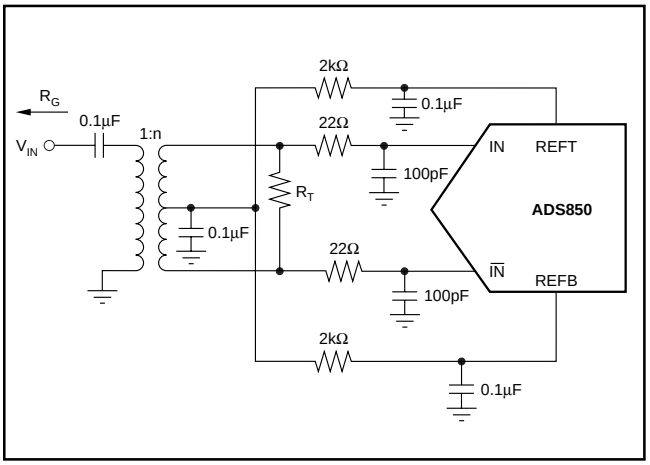


FIGURE 3. Transformer-Coupled Input.

REFERENCE OPERATION

Integrated into the ADS850 is a bandgap reference circuit including logic that provides either a +1V or +2V reference output, by simply selecting the corresponding pin-strap configuration. For more design flexibility, the internal reference can be shut off and an external reference voltage used. Table I provides an overview of the possible reference options and pin configurations.

MODE	INPUT RANGE	SEL	V_{REF}	REFB	REFT
Internal	2Vp-p	V_{REF}	SEL	NC	NC
Internal	4Vp-p	GND	NC	NC	NC
External	2V < FSR < 4V	$+V_S$	1V < FSR < 2V	NC	NC
External	(REFB – REFT) • 2	$+V_S$	GND	1.5V < REFB < 2V	2V < REFT <3.5V

TABLE I. Selected Reference Configuration Examples.

A simple model of the internal reference circuit is shown in Figure 4. The internal blocks are a 1V bandgap voltage reference, buffer, the resistive reference ladder, and the drivers for the top and bottom reference which supply the necessary current to the internal nodes. As shown, the output of the buffer appears at the V_{REF} pin. The full-scale input span of the ADS850 is determined by the voltage at V_{REF}, according to Equation 1:

$$\text{Full-Scale Input Span} = 2 \bullet V_{REF} \quad (1)$$

Note that the current drive capability of this amplifier is limited to about 1mA and should not be used to drive low loads. The programmable reference circuit is controlled by the voltage applied to the select pin (SEL). Refer to Table I for an overview.

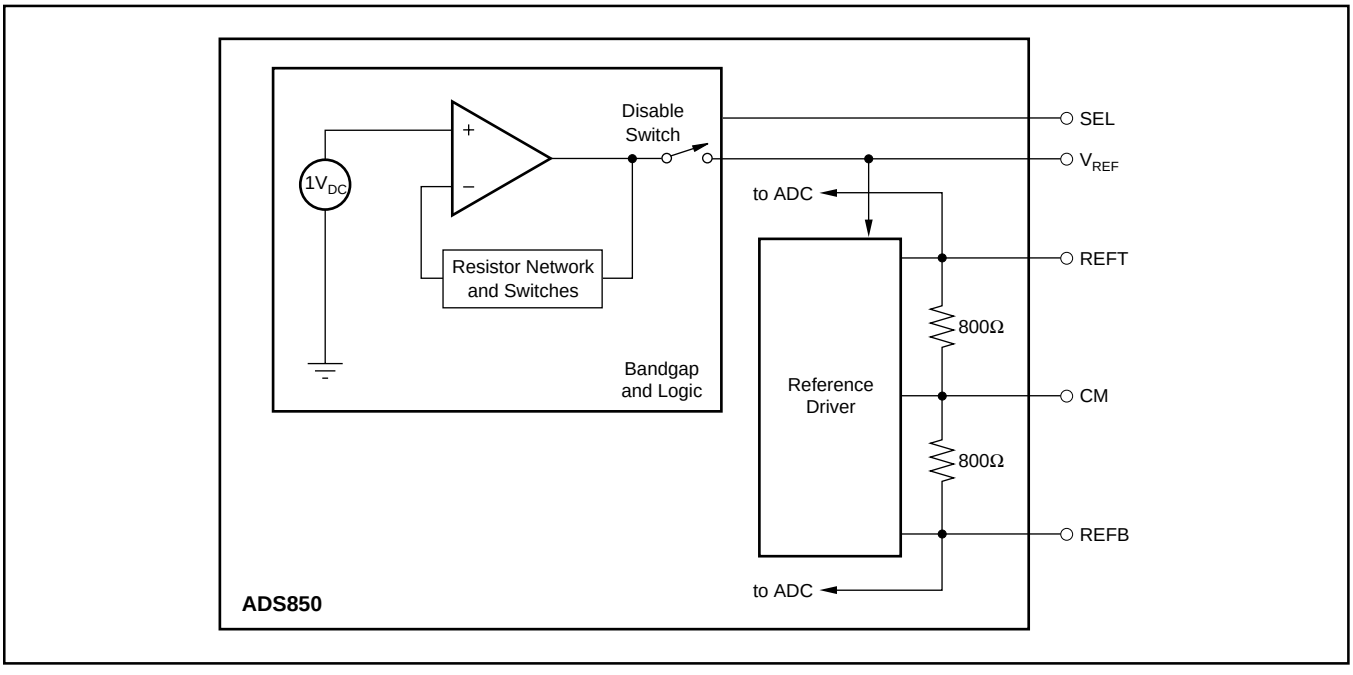


FIGURE 4. Equivalent Reference Circuit.

The top reference (REFT) and the bottom reference (REFB) are brought out mainly for external bypassing. For proper operation with all reference configurations, it is necessary to provide solid bypassing to the reference pins in order to keep the clock feedthrough to a minimum. Figure 5 shows the recommended reference decoupling configuration.

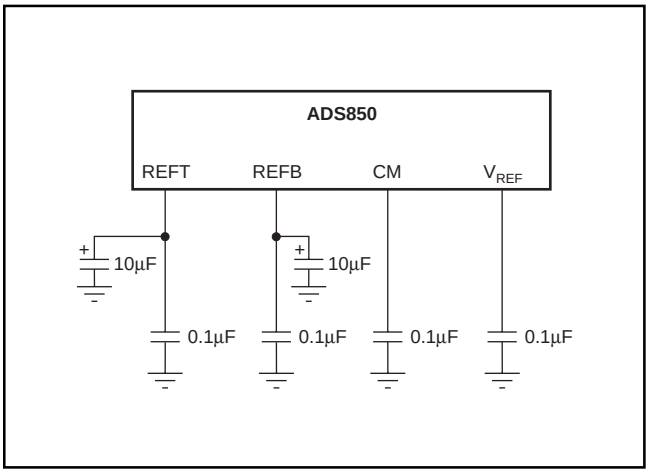


FIGURE 5. Recommended Reference Bypassing Scheme.

In addition, the Common-Mode Voltage (CMV) may be used as a reference level to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternate method of generating a common-mode voltage is given in Figure 6. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode level will appear at the midpoint. The output buffers of the top and bottom reference are designed to supply approximately 2mA of output current.

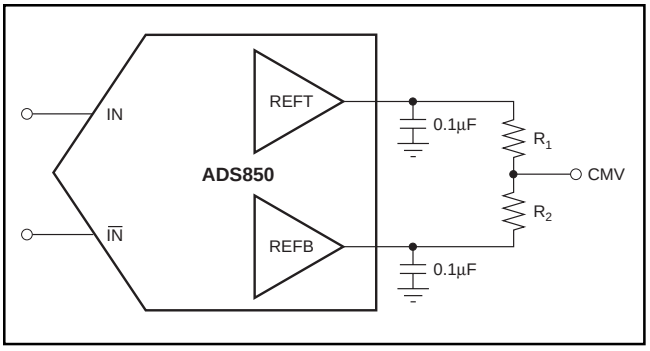


FIGURE 6. Alternative Circuit to Generate Common-Mode Voltage.

EXTERNAL REFERENCE OPERATION

Depending on the application requirements, it might be advantageous to operate the ADS850 with an external reference. This may improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy. To use the ADS850 with an external reference, the user must disable the internal reference, as shown in Figure 7. By connecting the SEL pin to $+V_S$, the internal logic will shut down the internal reference. At the same time, the output of the internal reference buffer is disconnected from the V_{REF} pin, which now must be driven with the external reference. Note that a similar bypassing scheme should be maintained as described for the internal reference operation.

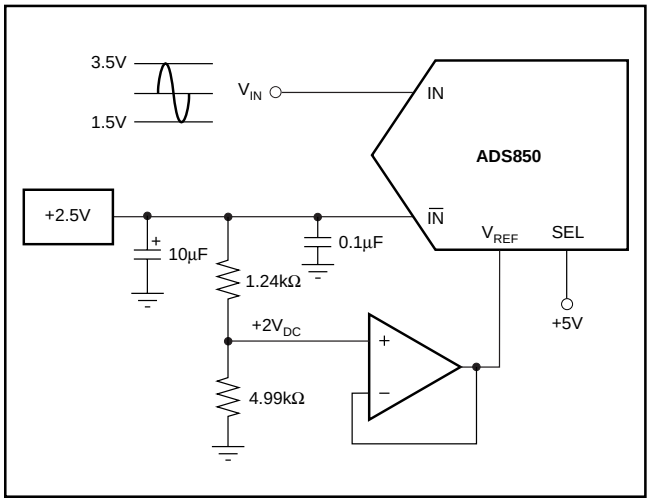


FIGURE 7. External Reference, Input Range 1.5V to 3.5V (2Vp-p), Single-Ended, with +2.5V Common-Mode Voltage.

DIGITAL INPUTS AND OUTPUTS

Over Range (OVR)

One feature of the ADS850 is its 'Over Range' digital output (OVR). This pin can be used to monitor any out-of-range condition, which occurs every time the applied analog input voltage exceeds the input range (set by V_{REF}). The OVR output is LOW when the input voltage is within the defined input range. It becomes HIGH when the input voltage is beyond the input range. This is the case when the input voltage is either below the bottom reference voltage or above the top reference voltage. OVR will remain active until the analog input returns to its normal signal range and another conversion is completed. Using the MSB and its complement in conjunction with OVR a simple clue logic can be built that detects the overrange and underrange conditions, as shown in Figure 8. It should be noted that OVR is a digital output which is updated along with the bit information corresponding to the particular sampling incidence of the analog signal. Therefore, the OVR data is subject to the same pipeline delay (latency) as the digital data.

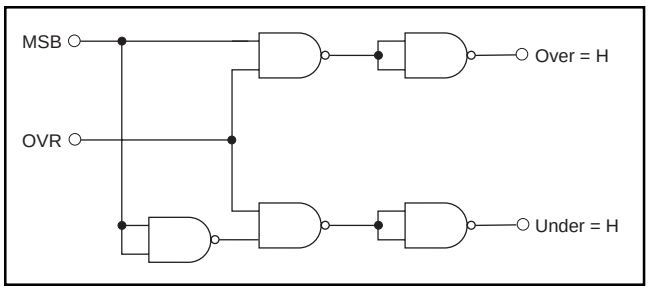


FIGURE 8. External Logic for Decoding Under- and Over-Range Condition.

CLOCK INPUT REQUIREMENTS

Clock jitter is critical to the SNR performance of high-speed, high-resolution ADCs. It leads to aperture jitter (t_A) which adds noise to the signal being converted. The ADS850 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20\log\frac{1}{2\pi f_{IN} t_A}\ \text{rms signal to rms noise}$$

Where: f_{IN} is Input Signal Frequency

t_A is rms Clock Jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have a 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less.

DIGITAL OUTPUTS

The digital outputs of the ADS850 are designed to be compatible with both high speed TTL and CMOS logic families. The driver stage for the digital outputs is supplied through a separate supply pin, VDRV, which is not connected to the analog supply pins. By adjusting the voltage on VDRV, the digital output levels will vary respectively. Therefore, it is possible to operate the ADS850 on a +5V analog supply while interfacing the digital outputs to 3V logic.

It is recommended to keep the capacitive loading on the data lines as low as possible (≤ 15pF). Larger capacitive loads demand higher charging currents as the outputs are changing. Those high current surges can feed back to the analog portion of the ADS850 and influence the performance. If necessary, external buffers or latches may be used which provide the added benefit of isolating the ADS850 from any digital noise activities on the bus coupling back high frequency noise. In addition, resistors in series with each data line may help maintain the ac performance of the ADS850. Their use depends on the capacitive loading seen by the converter. Values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances, as the output levels change from LOW to HIGH or HIGH to LOW.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high frequency designs. Multi-layer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. It is recommended that the analog and digital ground pins of the ADS850 be joined together at the IC and be connected only to the analog ground of the system.

The ADS850 has analog and digital supply pins, however, the converter should be treated as an analog component and all supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise that would otherwise be coupled into the converter and degrade the achievable performance.

Because of the pipeline architecture, the converter also generates high frequency current transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the analog supplies. In most cases, 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger size bipolar capacitor (1µF to 22µF) should be placed on the PC board in close proximity to the converter circuit.

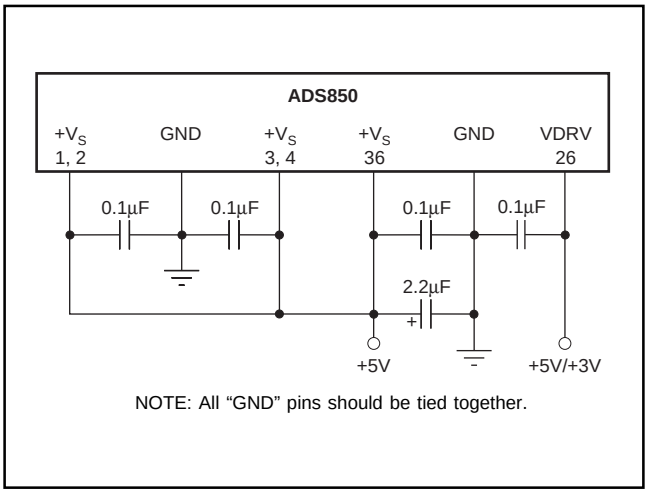


FIGURE 9. Recommended Bypassing for Analog Supply Pins.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS850Y/250	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS850Y	Samples
ADS850Y/250G4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS850Y	Samples
ADS850Y/2K	ACTIVE	TQFP	PFB	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS850Y	Samples

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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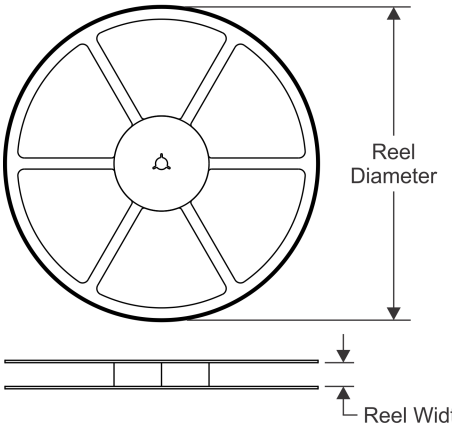
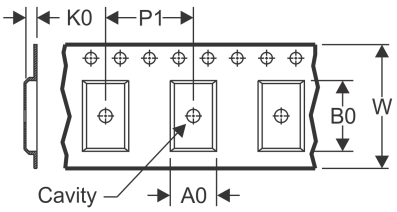
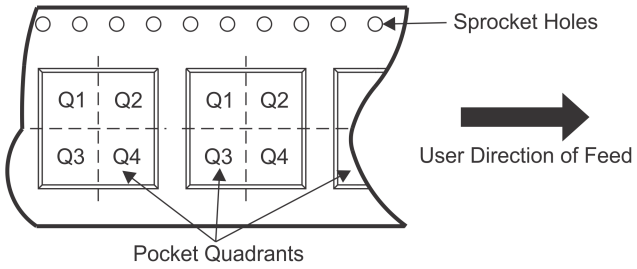


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

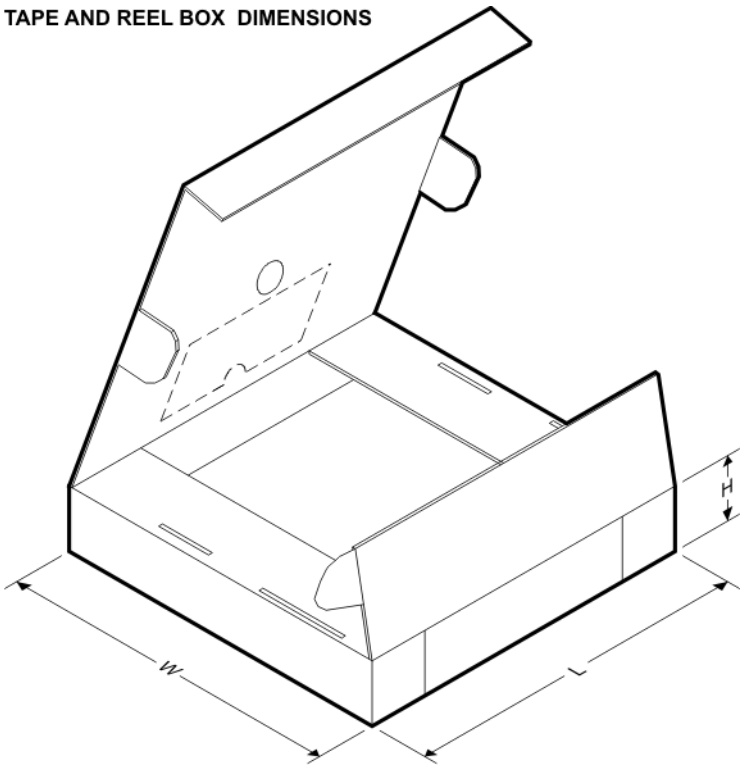
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS850Y/250	TQFP	PFB	48	250	177.8	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS850Y/250	TQFP	PFB	48	250	210.0	185.0	35.0

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