AKD4351

Evaluation board Rev.B for AK4351

General Description

AKD4351 is an evaluation board for the 18bit audio D/A converter AK4351. The AKD4351 has the interface with AKM's wave generator using ROM data and with AKM's ADC evaluation boards(AKD5392, AKD5391, AKD5352, and AKD5351). Therefore, it is easy to evaluate the AK4351. The AKD4351 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4351 --- Evaluation board of AK4351

Function

- On-board clock generator
- Compatible with the following 3 types of interface
  1) Direct interface with AKM's A/D converter, and direct interface with ROM board.
  2) Direct interface with signal generator(AKD43XX)
  3) On-board CS8412 as DIR which accepts optical input
- A BNC connector for an external clock input

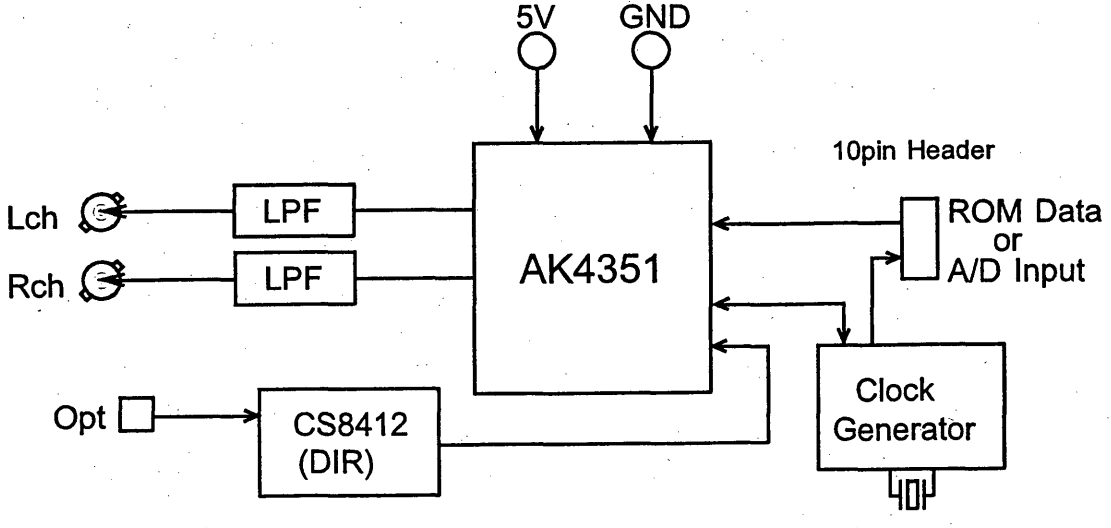
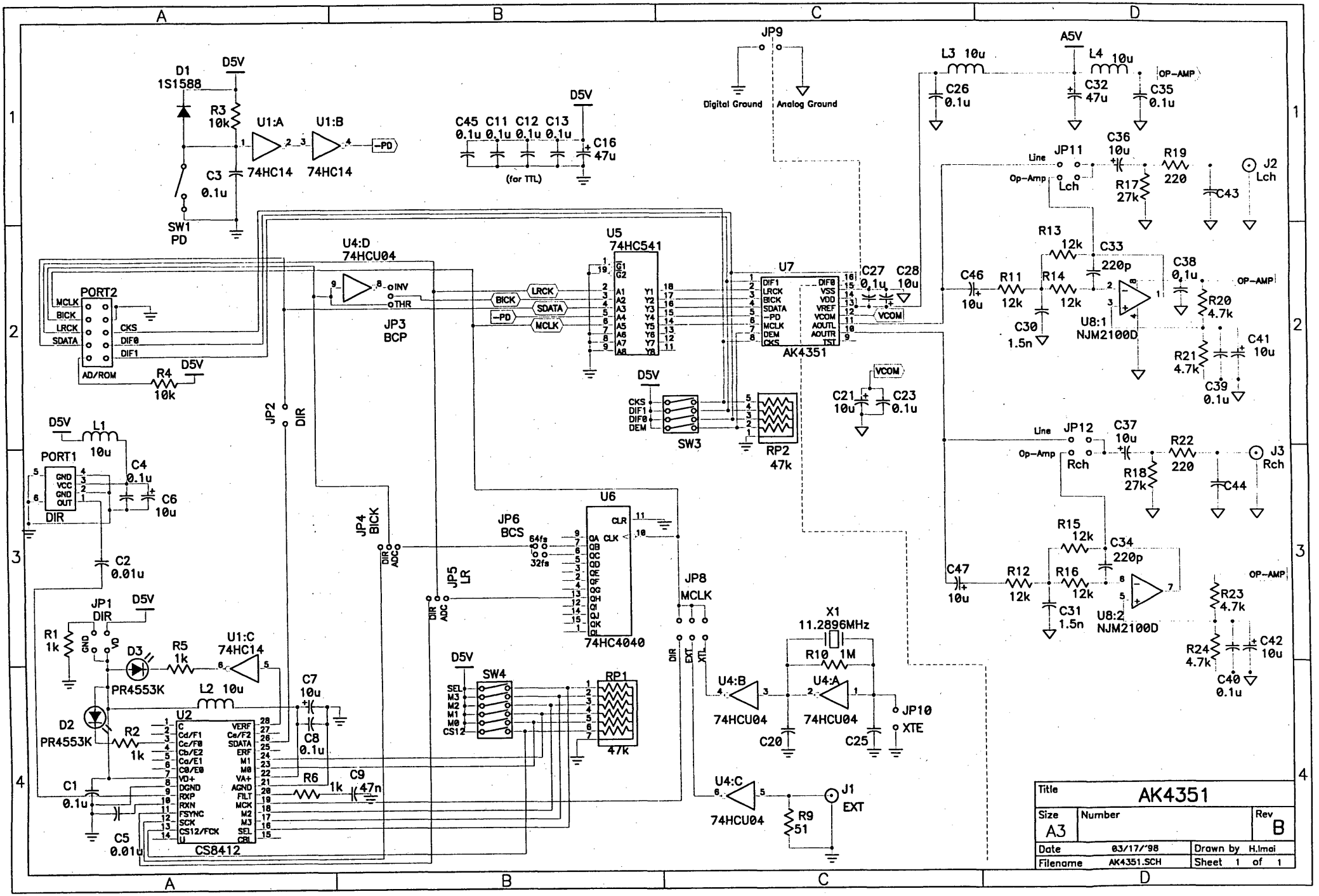


Figure 1. AKD4351 Block Diagram


JP9
Digital Ground
Analog Ground
D1
1S1588
D5V
R3
10k
U1:A
U1:B
74HC14
74HC14
-PD
C3
0.1u
SW1
PD
C45 C11 C12 C13
0.1u 0.1u 0.1u 0.1u
C16
47u
(for TTL)
L3 10u
A5V
L4 10u
OP-AMP
C26
0.1u
C32
47u
C35
0.1u
C36
10u
JP11
Line
Op-Amp
Lch
R19
220
R17
27k
C43
J2
Lch
R13
12k
C33
220p
C38
0.1u
C46
10u
R11
12k
R14
12k
C30
1.5n
U8:1
NJM2100D
R20
4.7k
R21
4.7k
C41
10u
C39
0.1u
U4:D
74HCU04
JP3
BCP
U5
74HC541
U7
AK4351
C27
0.1u
C28
10u
VCOM
C21
10u
C23
0.1u
PORT2
MCLK
BICK
LRCK
SDATA
CKS
DIF0
DIF1
AD/ROM
R4
10k
D5V
SW3
RP2
47k
JP2
DIR
L1
10u
PORT1
GND
VCC
GND
OUT
DIR
C4
0.1u
C6
10u
C2
0.01u
JP4
BICK
JP5
LR
JP6
BCS
64fs
32fs
U6
74HC4040
JP8
MCLK
JP1
DIR
R1
1k
D3
PR4553K
R5
1k
U1:C
74HC14
L2 10u
C7
10u
C8
0.1u
D2
PR4553K
R2
1k
U2
CS8412
C1
0.1u
C5
0.01u
R6
1k
C9
47n
SW4
RP1
47k
X1
11.2896MHz
R10 1M
U4:B
U4:A
74HCU04
74HCU04
C20
C25
JP10
XTE
U4:C
74HCU04
R9
51
J1
EXT
Line
Op-Amp
Rch
JP12
C37
10u
R22
220
R18
27k
C44
J3
Rch
R15
12k
C34
220p
C47
10u
R12
12k
R16
12k
C31
1.5n
U8:2
NJM2100D
R23
4.7k
R24
4.7k
C42
10u
C40
0.1u
Title
AK4351
Size
A3
Number
Rev
B
Date
03/17/'98
Drawn by
H.Imai
Filename
AK4351.SCH
Sheet 1 of 1

■ Analog Output

Analog signals are output through BNC connectors on the board and the output level are typically 3.4Vpp (@ VREFH-VREFL=5.0V). Please set JP11/JP12 "Line".

※ C46 and C47 has been removed.

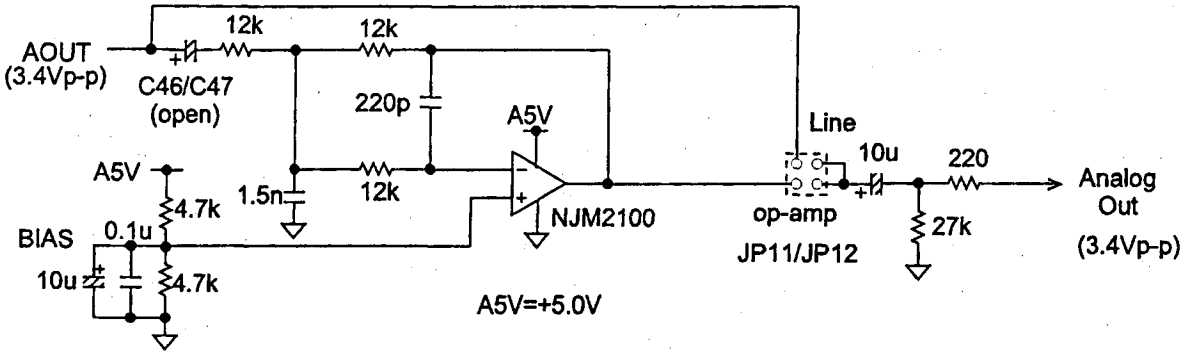


Fig.2 on-board analog filter

■ Grounding and Power Supply Decoupling

To minimize the effect of digital noise, the AKD4351 should be decoupled. VDD is supplied from analog power supply of the system. Decoupling capacitors should be connected to AK4351 as near as possible. Especially the capacitor between VREF and VSS should be connected nearest.

■ Operation Sequence

① Set up the power supply lines.
D5V=A5V= 5.0V,
AGND=DGND=0V.
Each supply line should be distributed from the power supply unit.

② Set up the evaluation modes and jumper pins.
(See the next item)

③ Set up the DIP-SW.
(See the next item.)

④ Power on.

⑤ Reset the AK4351 by SW1.

(The AK4351 is reset by SW1: PD = "L" during operarion.)

■ Set-up of the evaluation modes and jumper pins

1. Evaluation modes

Applicable evaluation modes

① DIR (Optical Link) ・・・・・・・(default)
② Using ROM data(AK43XX).
③ Using AKM's evaluation board for ADC
④ Feeding all signals from external

① DIR (Optical Link)

PORT1 is used. All clock are supplied from CS8412 (DIR). DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT2.

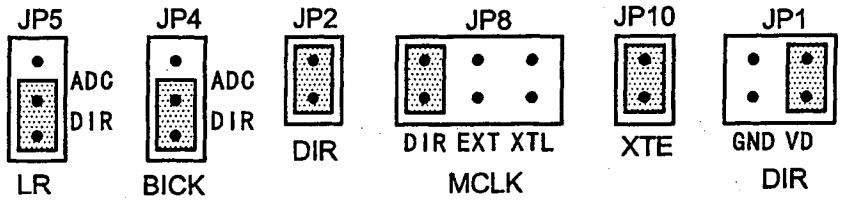


Fig.3 DIR

② Using ROM data(AK43XX).

Connect the AK43XX with PORT2.
AKD4351 sends MCLK to AKD43XX, and receives LRCK,BICK and SDATA.
※ In case of using external master clock through a BNC connector, set JP8(MCLK) EXT and short JP10(XTE).

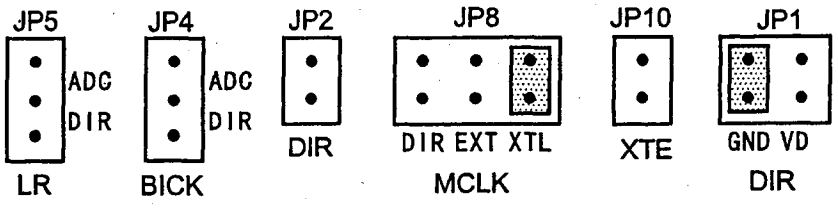


Fig.4 ROM data

③ Using AKM's evaluation board for ADC

To evaluate AK4351 with analog input, The AKM's evaluation board for ADC can be used.
MCLK, BICK and LRCK are supplied from clock generator on the AKD4351, and analog signal is A/D converted and send to AKD4351 through PORT2.
※ In case of using external master clock through a BNC connector, sets JP7(MCLK) EXT and shorts JP10(XTE).

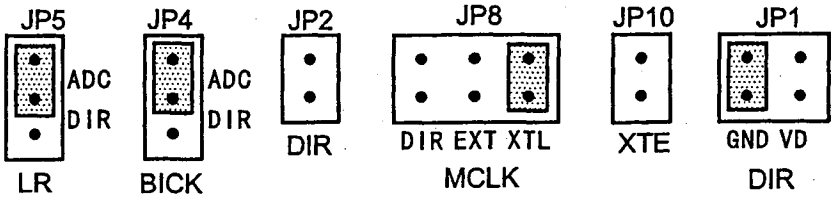


Fig.5 A/D data

④ Feeding all signals from external

Under the following set-up, all external signals could be fed through PORT2.

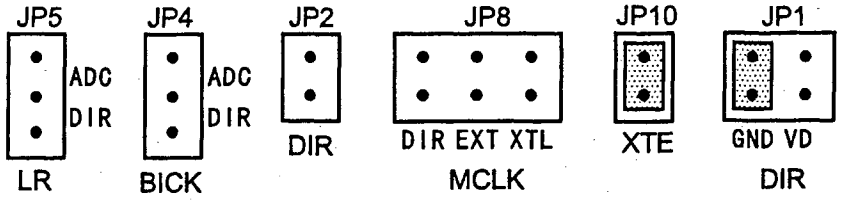


Fig.6 External signal

2. BICK frequency (JP6)

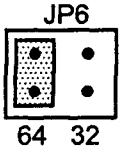


Fig.7

When BICK is fed from 74HC4040 on board, its frequency is selected with JP6.

64 : BICK = 64fs (Fig.7) ・・・・・・・・・ (default)

32 : BICK = 32fs

3. MCLK frequency (SW3-1)

Following the MCLK frequency, set up the SW3-1(CKS)

MCLK = 256fs : CKS = OFF ・・・・・・・・・ (default)

MCLK = 384fs : CKS = ON

※ In case of mode ① and ③, set SW3-1 OFF(256fs).

4. De-emphasis filter (SW3-4)

Set the De-emphasis filter of AK4351 with SW3-4(DEM). ・・・・・・・・・ (default = OFF)

5. Serial data format (SW3-2,3)

Set serial data format of AK4351 with SW3-2,3(DIF0,1).

※ In case of mode ①, adjust the data format between DIR and AK4351 with SW4.

Table 1 Serial data format of AK4351

DIF1	DIF0	Mode	BICK
0	0	16bit LSB justified	≧ 32fs
0	1	18bit LSB justified	≧ 36fs
1	0	18bit MSB justified	≧ 36fs
1	1	I ² S (IIS)	≧ 32fs or ≧ 36fs

・・・・ (default)

6. CS8412(DIR) Set-up (SW4, JP3)

Set the data format of CS8412(DIR) with SW4 and JP3. This format must be fitted to AK4351, which is set with DIF0 and DIF1.
(For more detailed configurations, please refer to the CS8412 data-sheet.)

Table 2-1 (SW4)

No.	pin name	ON	OFF	
1	SEL	normally ON		※ 1
2	M 3	see Table 2-2		
3	M 2			
4	M 1			
5	M 0			
6	CS12	Rch	Lch	※ 2

Table 2-2 CS8412 data format

M 3	M 2	M 1	M 0	mode	JP3 ※ 3	
0	0	0	0	0: 18bit MSB justified	INV	
0	0	1	0	2: I ² S	THR	・・・・・・・・・ (default)
0	1	0	1	5: 16bit LSB justified	THR	
0	1	1	0	6: 18bit LSB justified	THR	1:ON, 0:OFF

※ 1 When "ON", LED shows the pre-emphasis status.
(LED turns on when the data is pre-emphasized.)
※ 2 Selects the channel whose set up of CS8412.
※ 3 JP3 fits the BICK phase of CS8412 to AK4351s.

■ Switch list

[SW1] Reset switsh for AK4351. The reset state is "L".
[SW2] Soft-mute switch for AK4351. AK4351 is soft-muted while SW2 is pushed.
[SW3] Set-up switch of CKS,DEM,DIF1,DIF0.
[SW4] Set-up switch of CS8412.

[D1] "Pre-emphasis"-monitor. LED turns on when the data is pre-emphasized.
[D2] "VERF pin"-monitor for the CS8412.
LED turns on when some error has occurred to CS8412.

■ Other functions

[JP3] THR : The phase of BICK is not changed. (through)
INV : The phase of BICK is inverted.

[JP9] AGND and DGND are connected together by this jumper.

AK4351 measurement example

Measutement conditions :

DVDD=AVDD=5.0V, fs=44.1kHz, MCLK=256fs, BICK=64fs, DIR,
Resolution = 18bit,

1. Measurement unit = ROHDE&SCHWARZ UPD04

		units	external filters
THD+N(0dB)	-89.0	dBr	20kHzLPF
DR(-60dB)	96.0	dBr	20kHzLPF + A-weight
S/N	96.0	dBr	20kHzLPF + A-weight

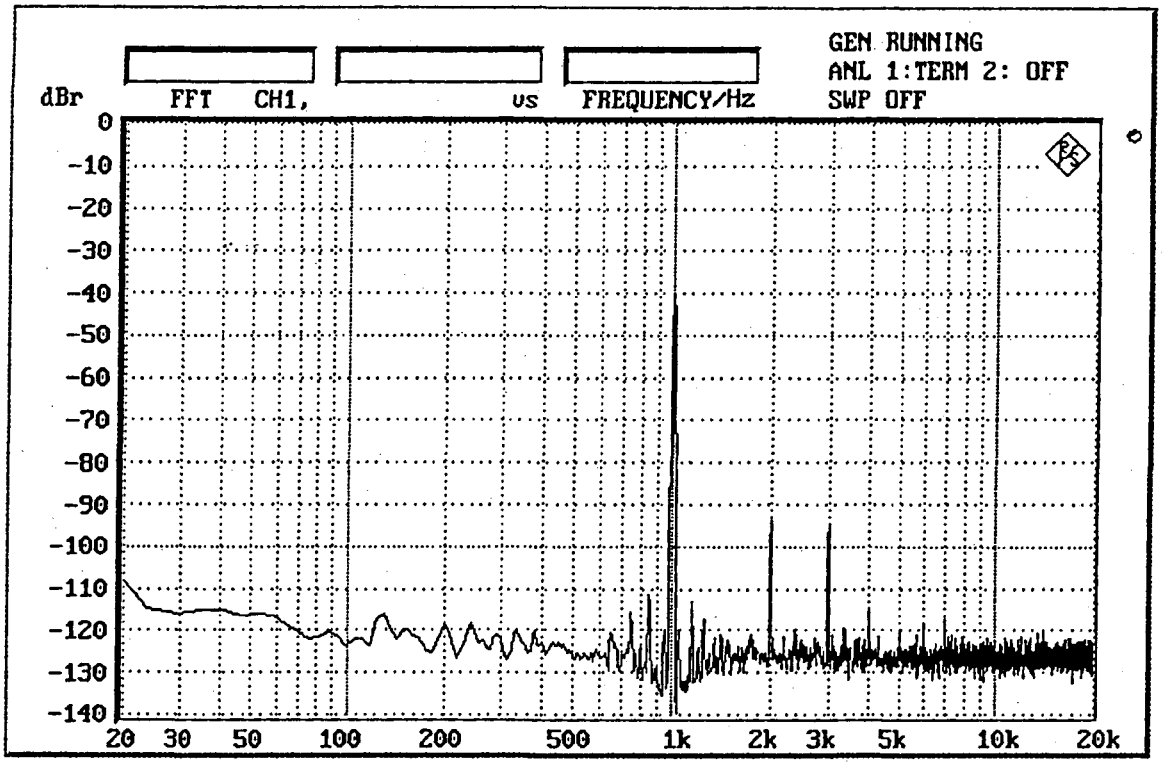


Fig.1 FFT plot (1kHz, 0dB, Notch=30dB)

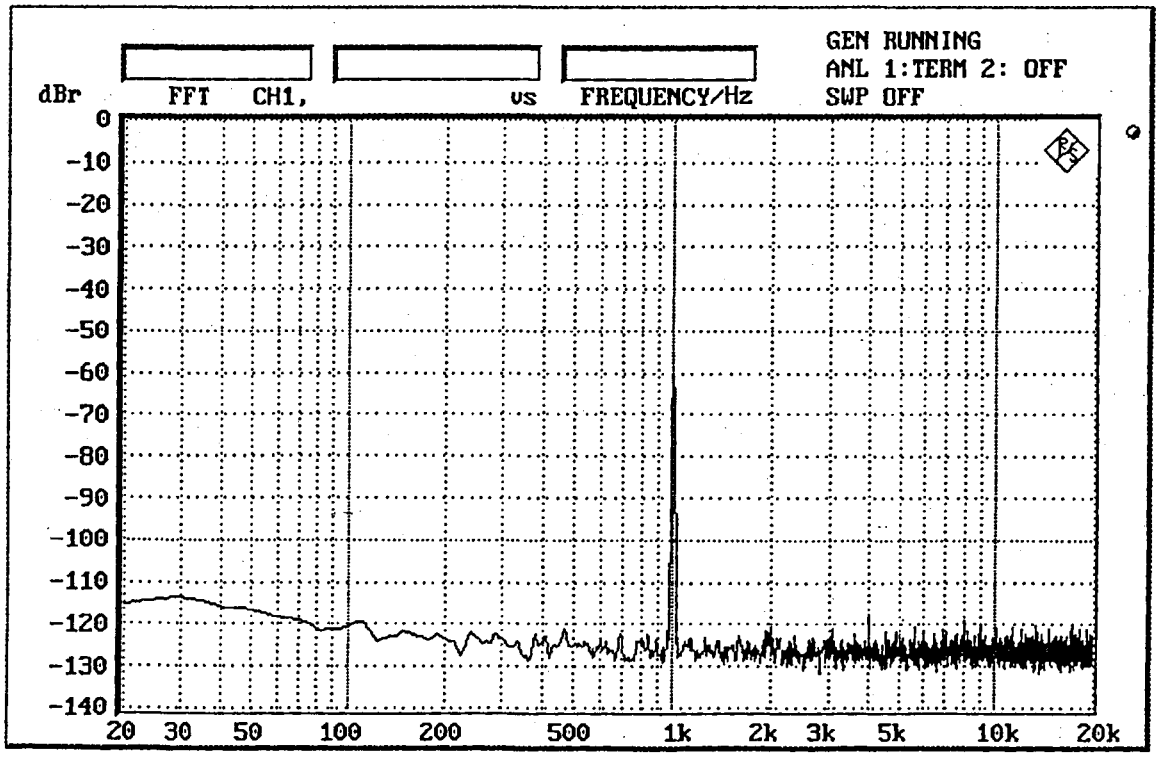


Fig.2 FFT plot (1kHz, -60dB)

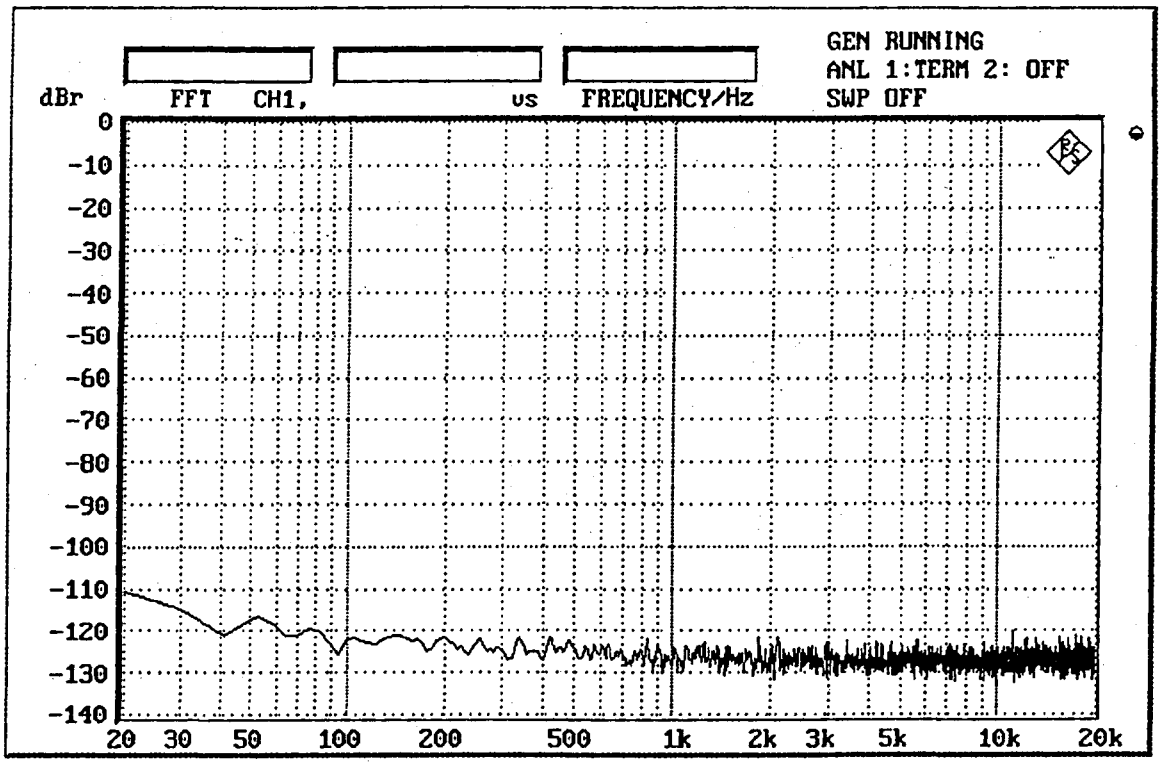


Fig.3 FFT plot (noise floor)

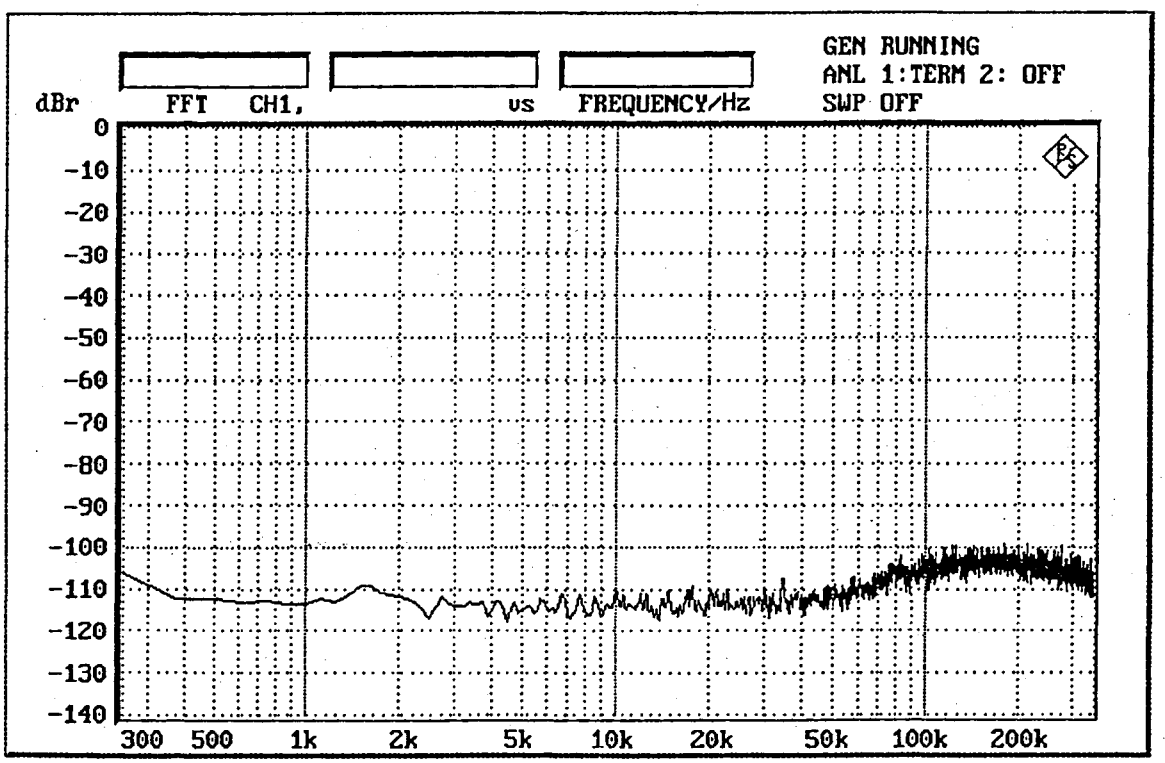


Fig.4 FFT plot (noise floor ~300kHz)

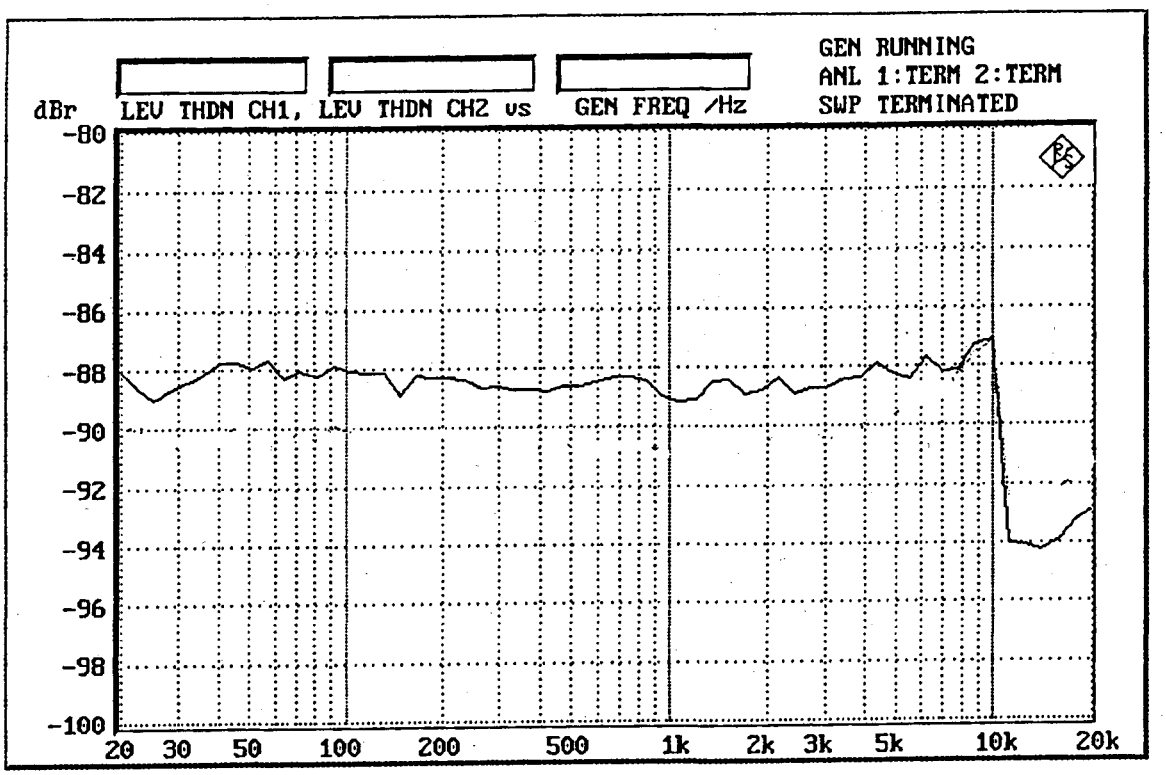


Fig.5 THD+N vs. Input frequency

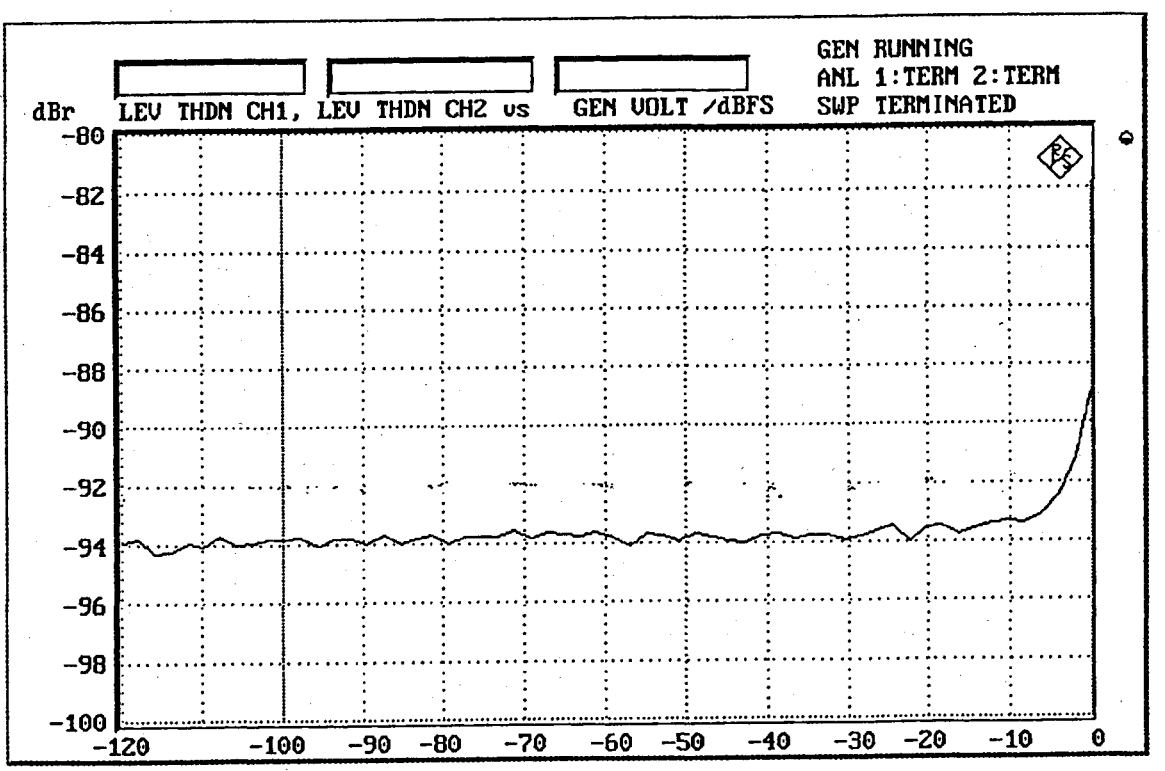


Fig.6 THD+N vs. Input level

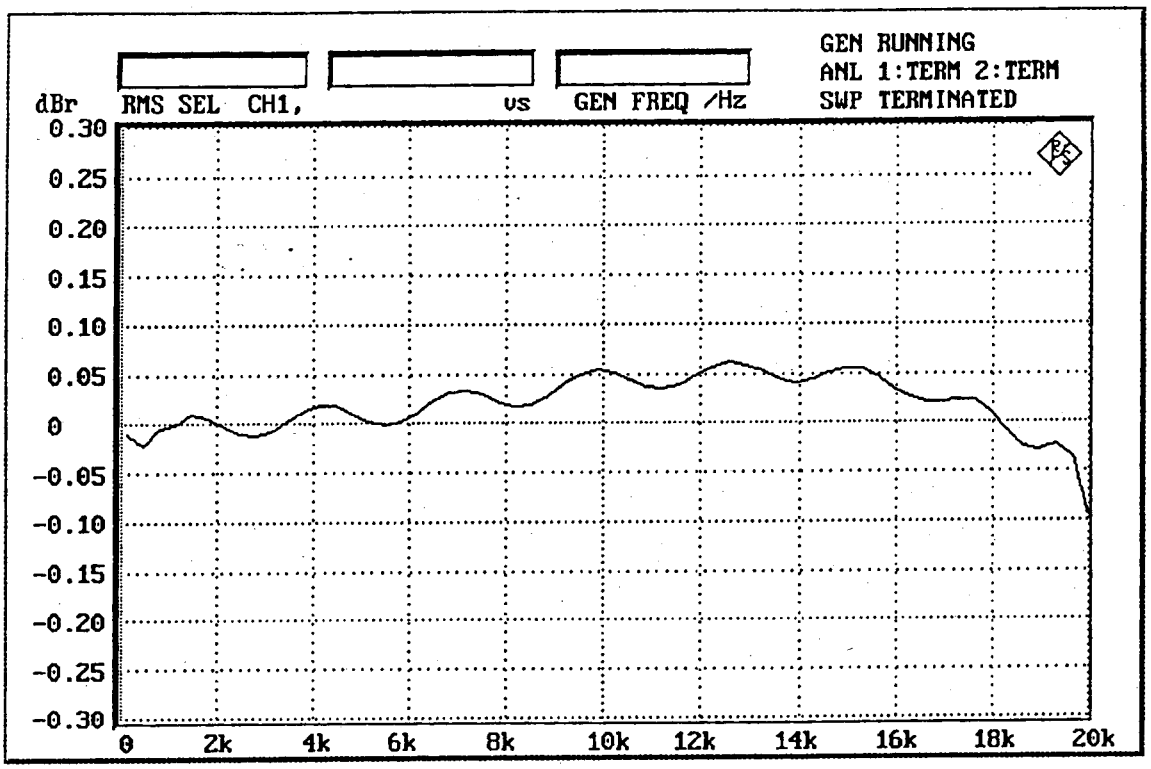


Fig.7 Frequency response

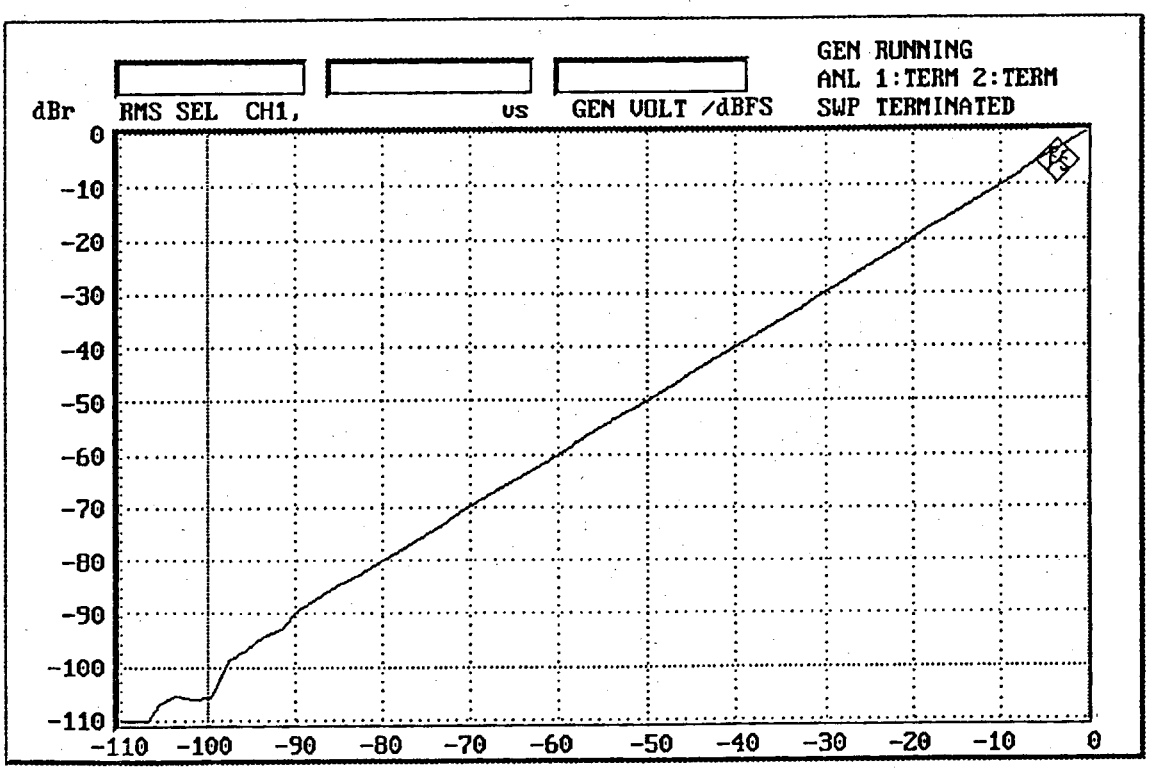


Fig.8 Linearity

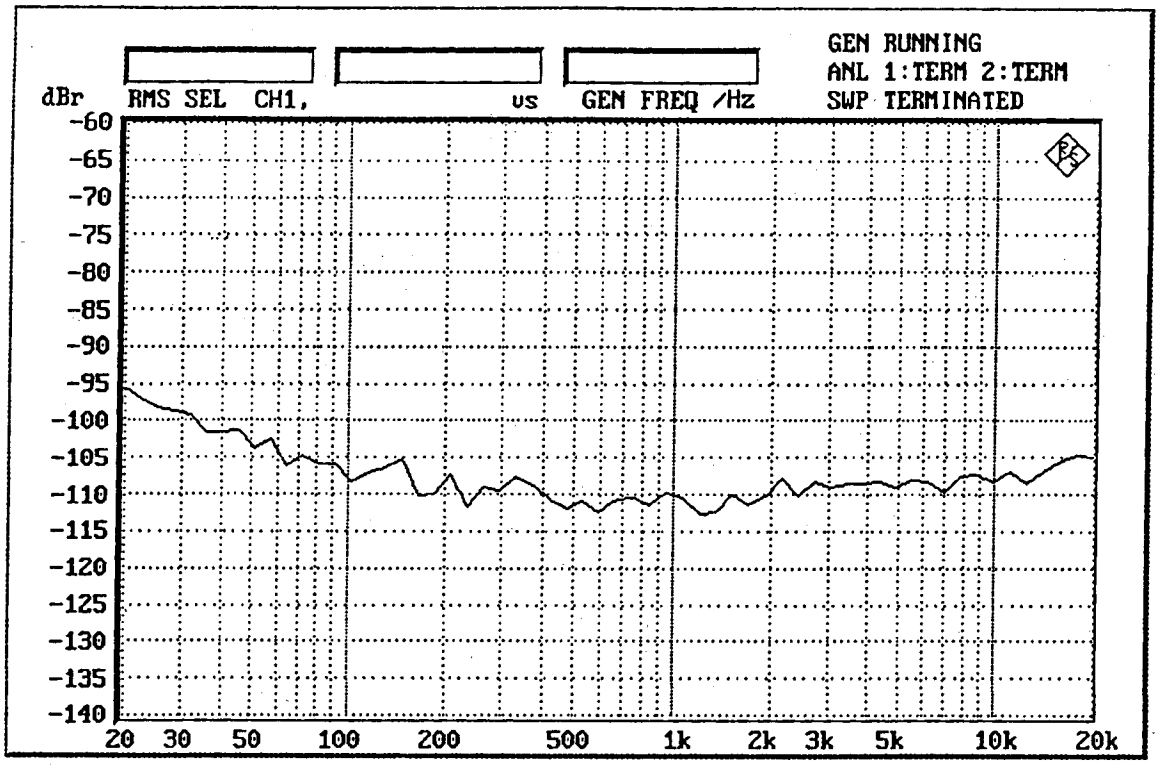
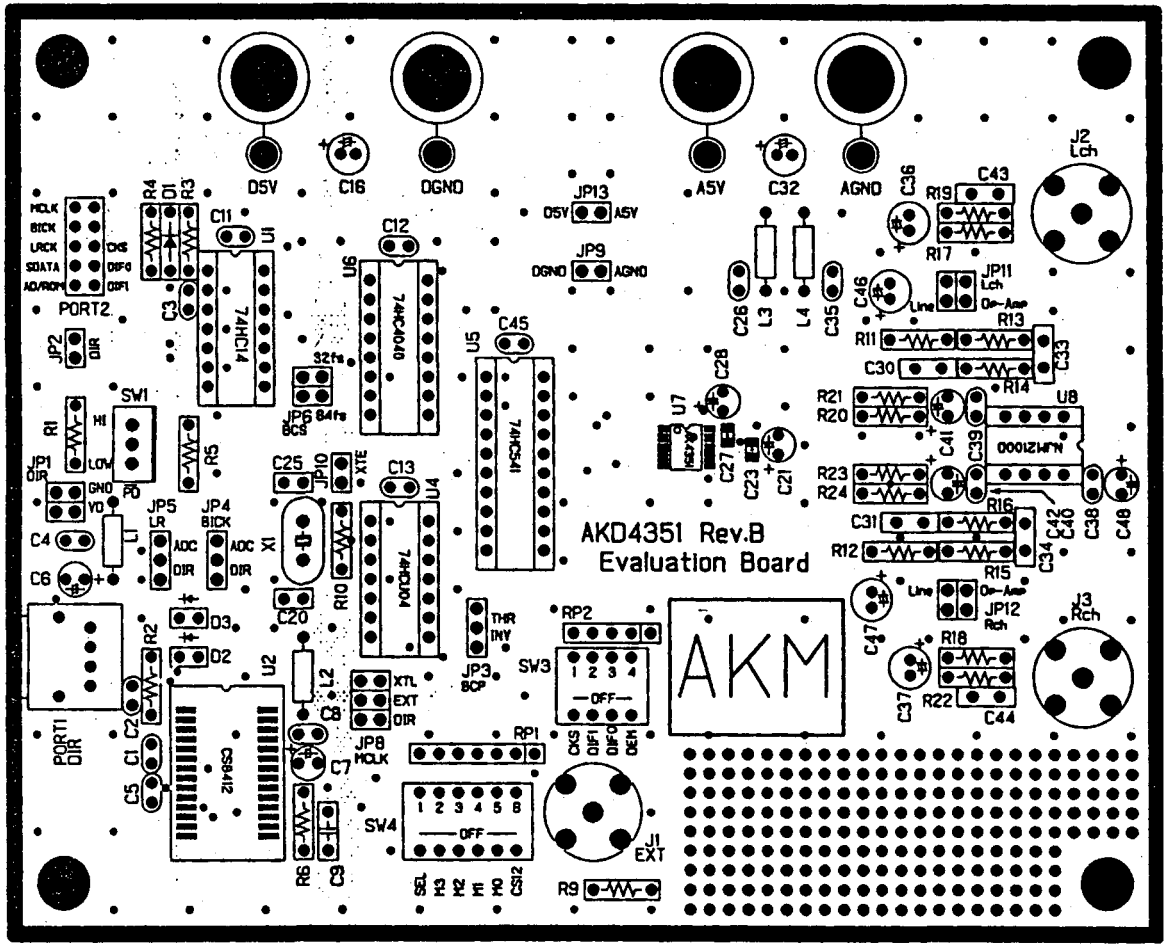
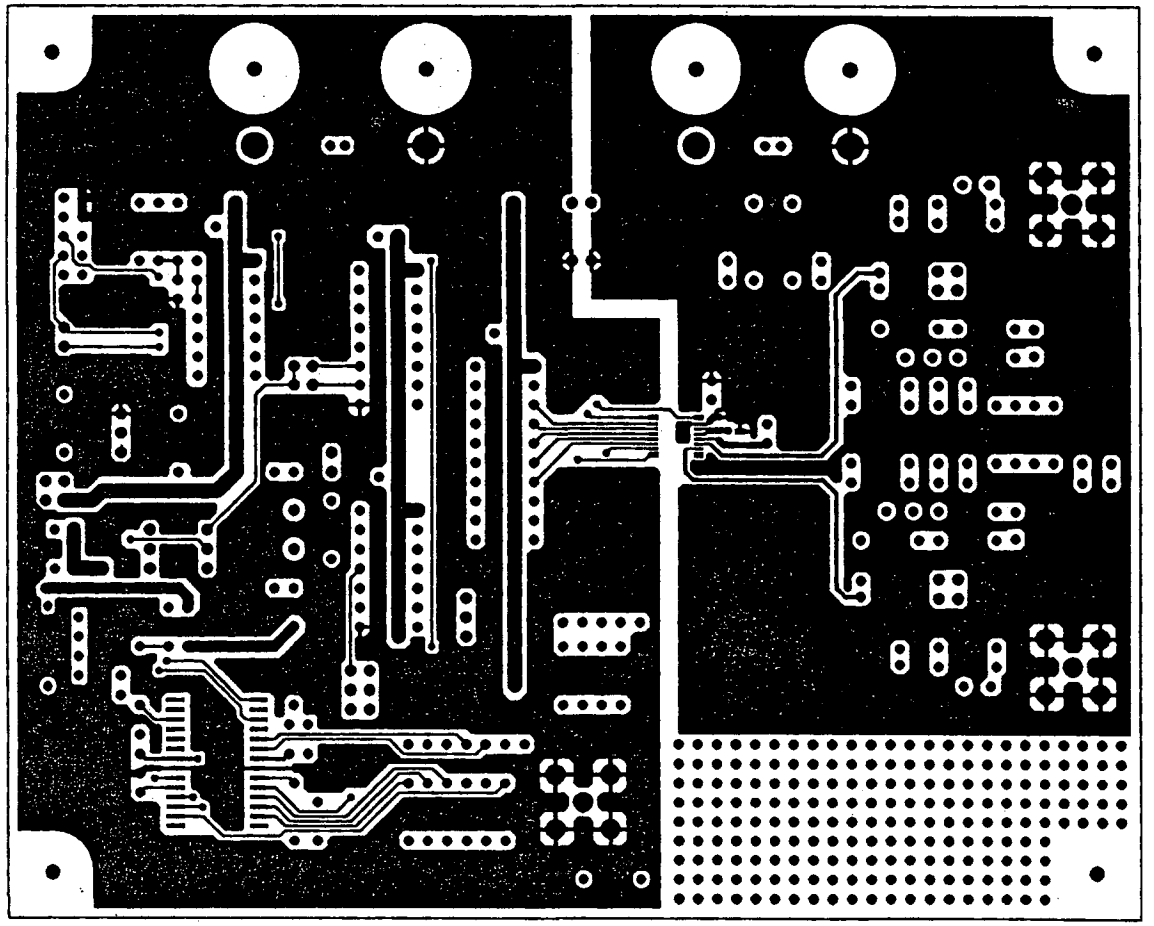


Fig.9 Crosstalk



AKD4351 Rev.B L1 SR SILK



AKD4351 Rev.B L1

AKD4351 Rev.B LZ

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