

# TC74VHCV573FT, TC74VHCV573FK

## Octal Schmitt D-Type Latch with 3-State Output

The TC74VHCV573 is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

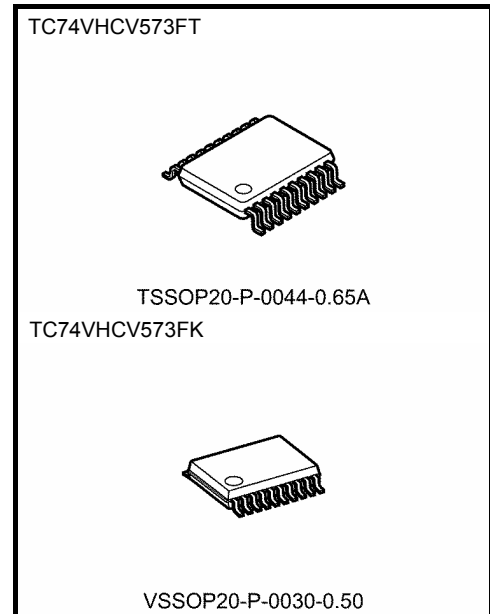
Input pin have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCV573 is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output <sup>(Note)</sup> pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state.

### Features

- High speed:  $t_{pd} = 5.0$  ns (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 2$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- Wide operating voltage range:  $V_{CC} (opr) = 1.8$  V to 5.5 V
- Output current:  $|I_{OH}|/I_{OL} = 16$  mA (min) ( $V_{CC} = 4.5$  V)
- Available in TSSOP and VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 573 type

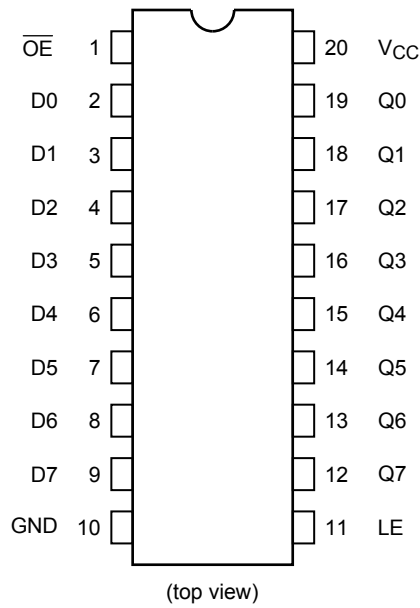


### Weight

TSSOP20-P-0044-0.65A	: 0.08 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Start of commercial production  
2010-01

## Pin Assignment



## Truth Table

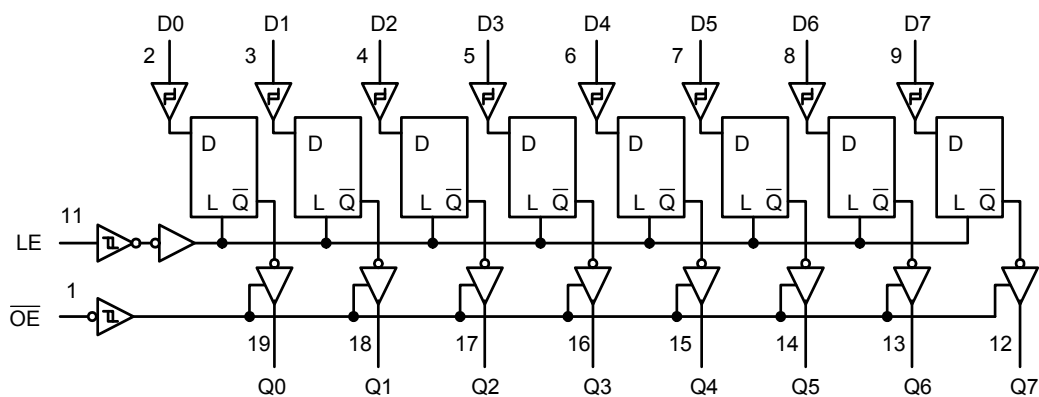
Inputs			Output
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	$I_{IK}$	-50	mA
Output diode current	$I_{OK}$	$\pm 50$ (Note 4)	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
Power dissipation	$P_D$	180	mW
DC $V_{CC}$ /ground current	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	1.8 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to 5.5 (Note 2)	V
		0 to $V_{CC}$ (Note 3)	
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 20 ( $V_{CC} = 3.3 \pm 0.3V$ )	ms/V
		0 to 1 ( $V_{CC} = 5 \pm 0.5V$ )	

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2: Output in off-state

Note 3: High or low state.

**Electrical Characteristics**

**DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Positive threshold voltage	V <sub>P</sub>	—		1.8	—	—	1.65	—	1.65	V
				2.3	—	—	1.85	—	1.85	
				3.0	—	—	2.20	—	2.20	
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V <sub>N</sub>	—		1.8	0.15	—	—	0.15	—	V
				2.3	0.45	—	—	0.45	—	
				3.0	0.90	—	—	0.90	—	
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage	V <sub>H</sub>	—		1.8	0.15	—	1.05	0.15	1.05	V
				2.3	0.20	—	1.10	0.20	1.10	
				3.0	0.30	—	1.20	0.30	1.20	
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	1.8	1.7	1.8	—	1.7	—	V
			I <sub>OH</sub> = -8 mA	3.0	2.9	3.0	—	2.9	—	
			I <sub>OH</sub> = -16 mA	4.5	4.4	4.5	—	4.4	—	
			I <sub>OH</sub> = -16 mA	3.0	2.58	—	—	2.48	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	1.8	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 8 mA	3.0	—	—	0.1	—	0.1	
			I <sub>OL</sub> = 16 mA	4.5	—	—	0.1	—	0.1	
			I <sub>OL</sub> = 16 mA	3.0	—	—	0.36	—	0.44	
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 5.5V	1.8 to 5.5	—	—	±0.5	—	±5.0	μA	
Power-off leakage current	I <sub>OFF</sub>	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V	0	—	—	0.5	—	5.0	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	2.0	—	20.0	μA	

## Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (LE)	$t_w$ (H)	—	2.5 ± 0.2	—	6.5	6.5	ns
			3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	$t_s$	—	2.5 ± 0.2	—	5.0	5.0	ns
			3.3 ± 0.3	—	3.5	3.5	
			5.0 ± 0.5	—	3.5	3.5	
Minimum hold time	$t_h$	—	2.5 ± 0.2	—	2.0	2.0	ns
			3.3 ± 0.3	—	1.5	1.5	
			5.0 ± 0.5	—	1.5	1.5	

## AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit			
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max		Min	Max	
Propagation delay time (LE-Q)	$t_{pLH}$ $t_{pHL}$	—	2.5 ± 0.2	15	—	8.9	16.2	1.0	19.0	ns	
				50	—	11.8	19.1	1.0	23.0		
			3.3 ± 0.3	15	—	6.6	11.9	1.0	14.0		ns
				50	—	8.8	15.4	1.0	17.5		
			5.0 ± 0.5	15	—	5.0	7.7	1.0	9.0		ns
				50	—	6.6	9.7	1.0	11.0		
Propagation delay time (D-Q)	$t_{pLH}$ $t_{pHL}$	—	2.5 ± 0.2	15	—	10.4	15.8	1.0	18.0	ns	
				50	—	13.2	20.7	1.0	23.5		
			3.3 ± 0.3	15	—	7.5	11.0	1.0	13.0		ns
				50	—	9.5	14.5	1.0	16.5		
			5.0 ± 0.5	15	—	5.4	6.8	1.0	8.0		ns
				50	—	7.0	8.8	1.0	10.0		
3-state output enable time	$t_{pZL}$ $t_{pZH}$	R <sub>L</sub> = 1 kΩ	2.5 ± 0.2	15	—	7.6	16.2	1.0	19.0	ns	
				50	—	10.7	19.0	1.0	22.0		
			3.3 ± 0.3	15	—	5.7	11.5	1.0	13.5		ns
				50	—	8.1	15.0	1.0	17.0		
			5.0 ± 0.5	15	—	4.2	7.7	1.0	9.0		ns
				50	—	6.1	9.7	1.0	11.0		
3-state output disable time	$t_{pLZ}$ $t_{pHZ}$	R <sub>L</sub> = 1 kΩ	2.5 ± 0.2	50	—	13.6	17.3	1.0	19.0	ns	
			3.3 ± 0.3	50	—	10.5	14.5	1.0	16.5		
			5.0 ± 0.5	50	—	8.2	9.7	1.0	11.0		
Output to output skew	$t_{osLH}$ $t_{osHL}$	(Note 1)	2.5 ± 0.2	50	—	—	2.0	—	2.0	ns	
			3.3 ± 0.3	50	—	—	1.5	—	1.5		
			5.0 ± 0.5	50	—	—	1.0	—	1.0		
Input capacitance	C <sub>IN</sub>	—	—	—	4	10	—	10	pF		
Output capacitance	C <sub>OUT</sub>	—	—	—	6	—	—	—	pF		
Power dissipation capacitance	C <sub>PD</sub>	—	(Note 2)	—	25	—	—	—	pF		

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C<sub>PD</sub> when n pcs. of latch operate can be gained by the following equation:

$$C_{PD} \text{ (total)} = 13 + 12 \cdot n$$

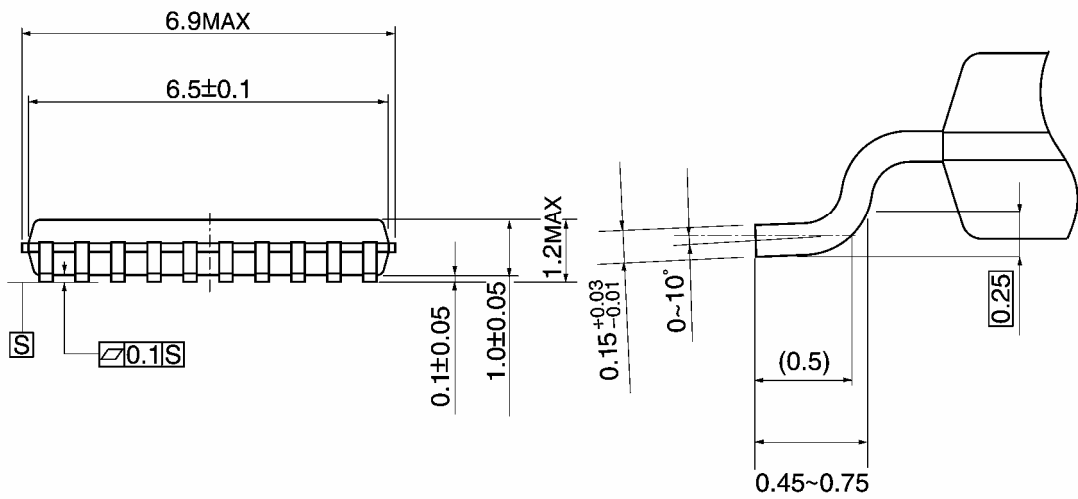
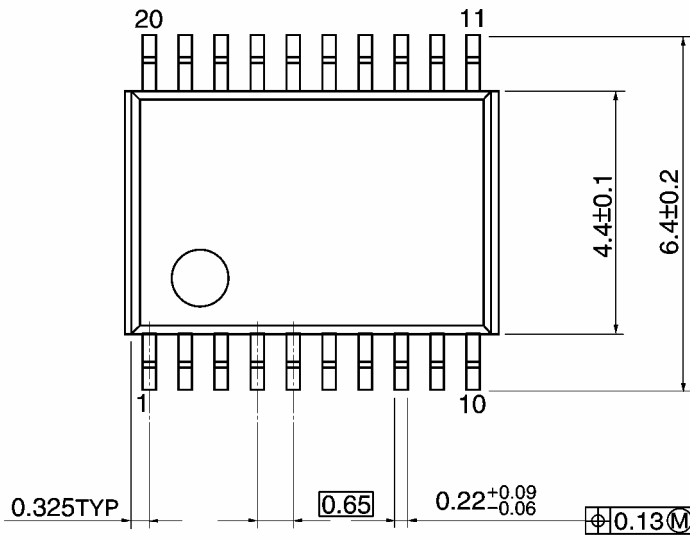
## Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Max	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	3.3	0.4	—	V
			5.0	0.8	—	
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	3.3	-0.1	—	V
			5.0	-0.4	—	
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

**Package Dimensions**

TSSOP20-P-0044-0.65A

Unit: mm



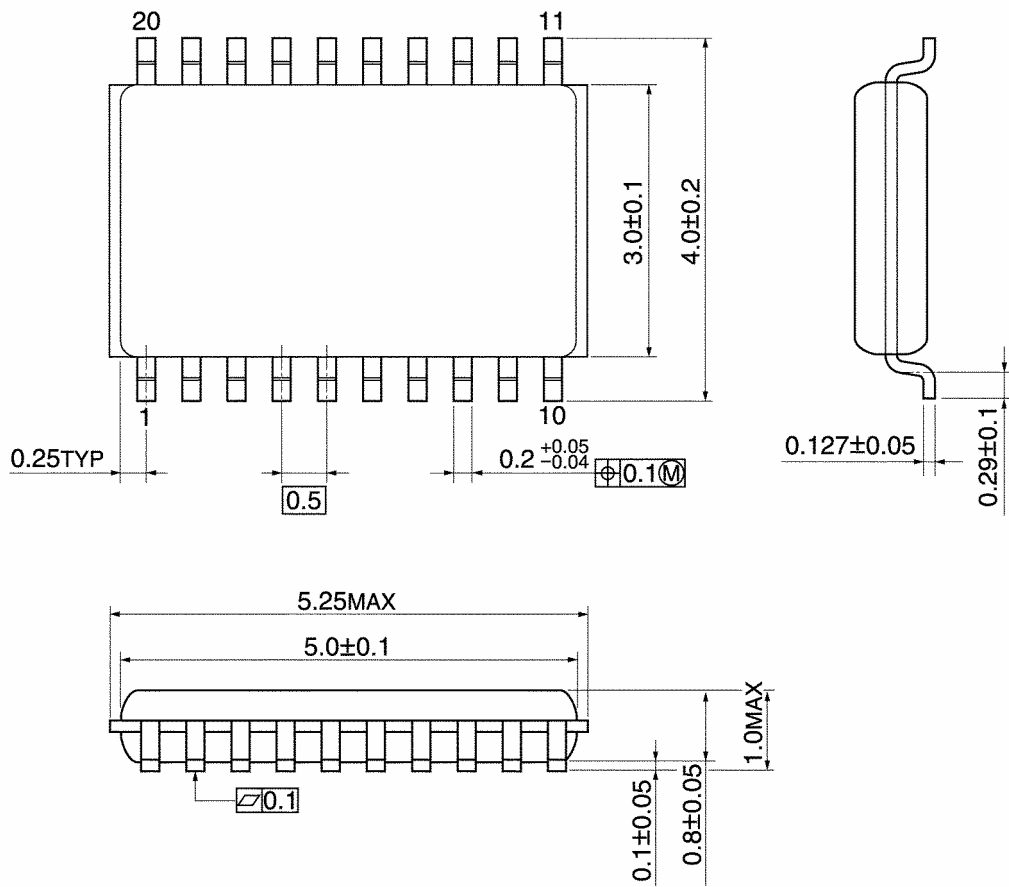
Weight: 0.08 g (typ.)



**Package Dimensions**

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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