Standard Products
UT64BS1X433 Matrix-A™ 64-Channel 1:4 Bus Switch
Preliminary Data Sheet
November 12, 2014
www.aeroflex.com/busswitch

FEATURES

❑ Interfaces to standard processor memory busses

❑ Single-chip interface to industry-standard asynchronous SRAM and PROM memory devices

❑ Eliminates need for additional logic or FPGA

❑ I/O channels functional to 3.3V

❑ R_{ON} 5 Ohms typical

❑ Flat R_{ON} characteristics over channel voltage

❑ Propagation delay 187ps through switch

❑ Transmission gate technology allows for true bi-directional operation

❑ Bus holders maintain output states on all 64 channels when de-selected

❑ Logic power 1mW/MHz

❑ Independent 5-bit address decoding to select 1 of 32 devices

❑ Temperature range -55°C to 125°C

❑ Operational environment:

  - Intrinsic total-dose: up to 300 krad(Si)

  - SEL Immune: $\leq$100 MeV-cm^2/mg @ 125°C

❑ Packaging options:

  - 400-pin Ceramic Land Grid, Column Grid and Ball Grid Array packages; 1mm pitch

❑ Standard Microcircuit Drawing 5962-TBD

  - QML Q and V (pending)

APPLICATIONS

  - Microprocessor interfaces that require large amounts of memory

  - High-speed applications or systems with large bus capacitance

  - Cost-sensitive applications that require bus isolation without an expensive FPGA

INTRODUCTION

The UT64BS1X433 Matrix-A™ is a 64-Channel, 1:4 Bus Switch, that provides bus isolation for up to four banks of 64 I/O connections. By providing bus isolation, the UT64BS1X433 can significantly reduce the amount of load capacitance seen by a host processor and memory devices. The reduction in both load capacitance and delay time significantly increase speed and performance compared with a discrete logic or FPGA memory interface solution.

The UT64BS1X433 operates from a single 3.3V supply. The bus channels can pass any voltage between V_{SS} and V_{DD}, allowing the switching of signals using other standards, such as LVCMOS 1.8V.

The UT64BS1X433 has two modes of operation. In mode 0, the device uses five address and one chip select line to electrically connect the input bank to one of four output banks and generate 1 of 32 chip select outputs. In mode 1, the device uses eight address and two chip select lines to independently control two pairs of two banks with each bank pair controlled by one of the two chip selects. Mode 1 allows the device to interface two different types of memory having different address bus configurations e.g. two PROM banks and two SRAM banks. The input and output banks connect via analog channels that have an R_{ON} that is nominally 5 Ohms over the entire input voltage range. The flat R_{ON} eliminates the need to add external series resistors for source impedance termination.

The UT64BS1X433 also provides logic to control up to eight discrete devices per bank by providing eight individual chip selects that are decoded using address lines ASEL[2:0] and BSEL[2:0]. In a fully utilized configuration, the UT64BS1X433 can select up to 32 discrete devices and provide bus isolation to each bank of eight devices. This makes the device ideally suited for use with mutli-chip module memory devices, such as the Aeroflex UT8R1/2/4M39 40/80/160Mbit family of SRAM devices. Each UT64BS1X433 can interface up to four of the Aeroflex 160Mb SRAM MCM devices with any Aeroflex LEON processor without the need for additional logic.

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INTRODUCTION

The UT64BS1X433 64-Channel 1:4 Bus Switch is built on a 0.35μm Triple-Well CMOS process. The device incorporates control logic that electrically connects input bank A to the output banks B0-B3, depending upon the selected channel. The control logic also decodes the address pins to provide chip-select outputs to up to 32 discrete memory devices. To ensure that important memory control lines e.g. $\overline{RD}$ and $\overline{WR}$ are consistently driven, regardless of the switching logic, the Matrix-A provides two 2-to-4 fanout buffers. Typical applications will connect the processor or memory controller's $\overline{RD}$ and $\overline{WR}$ output signals to XIN and YIN on the Matrix-A, and tie the corresponding XOUTn and YOUTn to the $\overline{RD}$ and $\overline{WR}$ memory inputs on each bank.
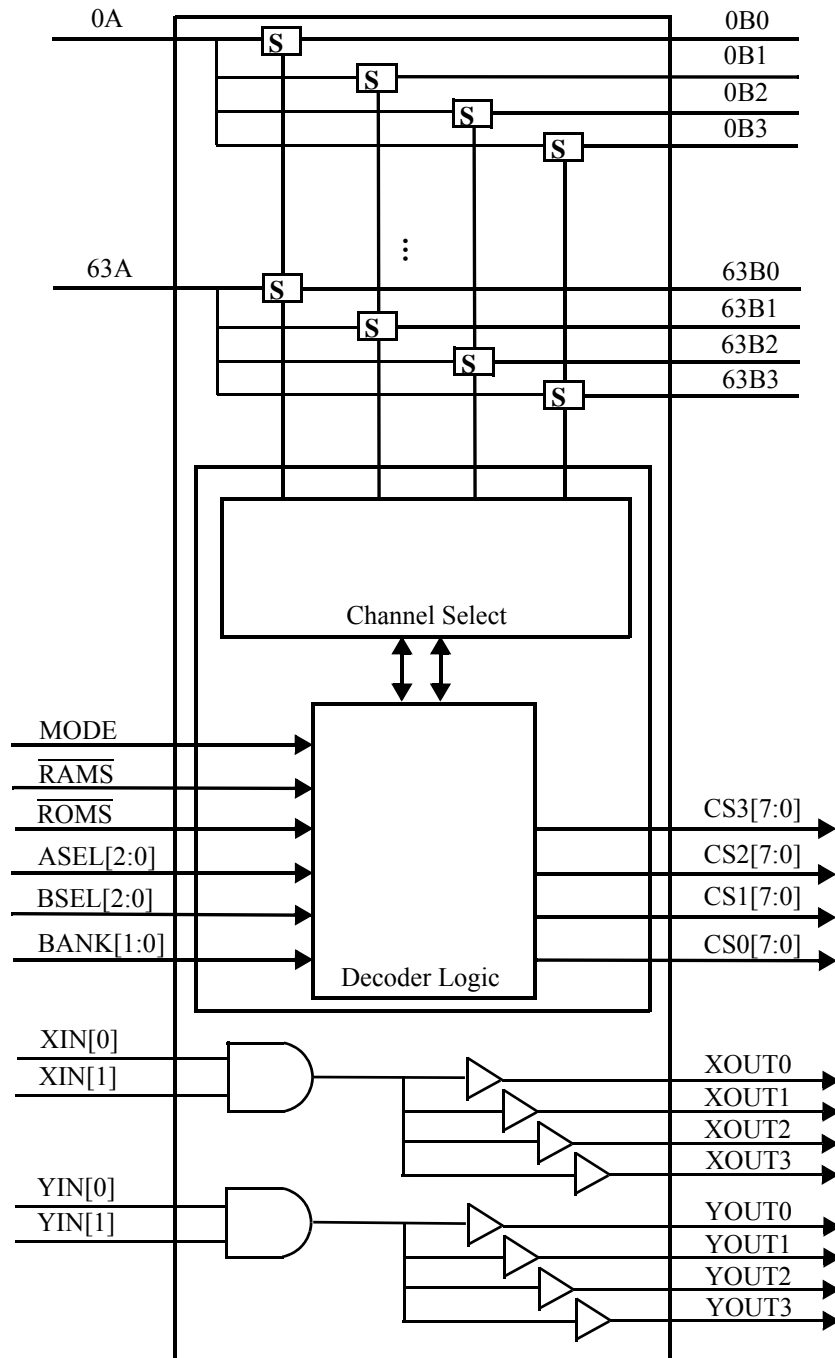
Figure 1. UT64BS1X433 Functional Block Diagram

Functional Tables

Table 1. Truth Table for Digital Inputs and Channels										
Inputs							Channel Outputs			
MODE	$\overline{\text{ROMS}}$	$\overline{\text{RAMS}}$	BSEL[2:0]	BANK[1]	BANK[0]	ASEL[2:0]	[63:0]B3	[63:0]B2	[63:0]B1	[63:0]B0
X	1	1	XXXb	X	X	XXXb	Z	Z	Z	Z
0	0	1	XXXb	X	X	XXXb	Z	Z	Z	Z
MODE 0										
0	X	0	XXXb	0	0	000b	Z	Z	Z	IN->OUT
						⋮				
0	X	0	XXXb	0	0	111b	Z	Z	Z	IN->OUT
0	X	0	XXXb	0	1	000b	Z	Z	IN->OUT	Z
						⋮				
0	X	0	XXXb	0	1	111b	Z	Z	IN->OUT	Z
0	X	0	XXXb	1	0	000b	Z	IN->OUT	Z	Z
						⋮				
0	X	0	XXXb	1	0	111b	Z	IN->OUT	Z	Z
0	X	0	XXXb	1	1	000b	IN->OUT	Z	Z	Z
						⋮				
0	X	0	XXXb	1	1	111b	IN->OUT	Z	Z	Z
MODE 1										
1	0	X	000b	X	0	XXXb	Z	Z	Z	IN->OUT
			⋮							
1	0	X	111b	X	0	XXXb	Z	Z	Z	IN->OUT
1	0	X	000b	X	1	XXXb	Z	Z	IN->OUT	Z
			⋮							
1	0	X	111b	X	1	XXXb	Z	Z	IN->OUT	Z
1	1	0	XXXb	0	X	000b	Z	IN->OUT	Z	Z
						⋮				
1	1	0	XXXb	0	X	111b	Z	IN->OUT	Z	Z
1	1	0	XXXb	1	X	000b	IN->OUT	Z	Z	Z
						⋮				
1	1	0	XXXb	1	X	111b	IN->OUT	Z	Z	Z

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Table 2: Truth Table for Digital Inputs and Digital Outputs										
Inputs							**Digital Outputs**			
MODE	**$\overline{ROMS}$**	**$\overline{RAMS}$**	**BSEL[2:0]**	**BANK[1]**	**BANK[0]**	**ASEL[2:0]**	**CS3[7:0]**	**CS2[7:0]**	**CS1[7:0]**	**CS0[7:0]**
X	1	1	XXXb	X	X	XXXb	11111111b	11111111b	11111111b	11111111b
0	0	1	XXXb	X	X	XXXb	11111111b	11111111b	11111111b	11111111b
MODE 0										
0	X	0	XXXb	0	0	000b	11111111b	11111111b	11111111b	11111110b
						⋮				
0	X	0	XXXb	0	0	111b	11111111b	11111111b	11111111b	01111111b
0	X	0	XXXb	0	1	000b	11111111b	11111111b	11111110b	11111111b
						⋮				
0	X	0	XXXb	0	1	111b	11111111b	11111111b	01111111b	11111111b
0	X	0	XXXb	1	0	000b	11111111b	11111110b	11111111b	11111111b
						⋮				
0	X	0	XXXb	1	0	111b	11111111b	01111111b	11111111b	11111111b
0	X	0	XXXb	1	1	000b	11111110b	11111111b	11111111b	11111111b
						⋮				
0	X	0	XXXb	1	1	111b	01111111b	11111111b	11111111b	11111111b
MODE 1										
1	0	X	000b	X	0	XXXb	11111111b	11111111b	11111111b	11111110b
			⋮							
1	0	X	111b	X	0	XXXb	11111111b	11111111b	11111111b	01111111b
1	0	X	000b	X	1	XXXb	11111111b	11111111b	11111110b	11111111b
			⋮							
1	0	X	111b	X	1	XXXb	11111111b	11111111b	01111111b	11111111b
1	1	0	XXXb	0	X	000b	11111111b	11111110b	11111111b	11111111b
						⋮				
1	1	0	XXXb	0	X	111b	11111111b	01111111b	11111111b	11111111b
1	1	0	XXXb	1	X	000b	11111110b	11111111b	11111111b	11111111b
						⋮				
1	1	0	XXXb	1	X	111b	01111111b	11111111b	11111111b	11111111b

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PIN IDENTIFICATION and DESCRIPTION
Logic Pins

Pin Name	Direction	Pin Number	Description
MODE	I	M11	Mode select 0: Banks 0-3 are selected with BANK[1:0] and bank 0-3 chip selects are selected with ASEL[2:0]. 1: Banks 0-1 are selected with BANK[0] and bank 0-1 chip selects are selected with BSEL[2:0]. Banks 2-3 are selected with BANK[1] and bank 2-3 chip selects are selected with ASEL[2:0].
$\overline{\text{RAMS}}$	I	M10	Enables banks 0-3 in mode 0 and banks 2-3 in mode 1.
$\overline{\text{ROMS}}$	I	N10	Enables banks 0-1 in mode 1. Don't care in mode 0.
ASEL[0]	I	P9	Bit 0 to select chip selects for banks 0-3 in mode 0 and for banks 2-3 in mode 1.
ASEL[1]	I	P10	Bit 1 to select chip selects for banks 0-3 in mode 0 and for banks 2-3 in mode 1.
ASEL[2]	I	R10	Bit 2 to select chip selects for banks 0-3 in mode 0 and for banks 2-3 in mode 1.
BSEL[0]	I	U7	Bit 0 to select chip selects for banks 0-1 in mode 1.
BSEL[1]	I	N9	Bit 1 to select chip selects for banks 0-1 in mode 1.
BSEL[2]	I	M9	Bit 2 to select chip selects for banks 0-1 in mode 1.
BANK[0]	I	U6	Bit 0 to select banks 0-3 in mode 0 and banks 0-1 in mode 1.
BANK[1]	I	U8	Bit 1 to select banks 0-3 in mode 0 and banks 2-3 in mode 1.
$\overline{\text{CS0[0]}}$	O	W5	Bank 0 chip select 0. Asserted when xSEL[2:0] = 000b.
$\overline{\text{CS0[1]}}$	O	Y6	Bank 0 chip select 1. Asserted when xSEL[2:0] = 001b.
$\overline{\text{CS0[2]}}$	O	V9	Bank 0 chip select 2. Asserted when xSEL[2:0] = 010b.
$\overline{\text{CS0[3]}}$	O	Y4	Bank 0 chip select 3. Asserted when xSEL[2:0] = 011b.
$\overline{\text{CS0[4]}}$	O	W9	Bank 0 chip select 4. Asserted when xSEL[2:0] = 100b.
$\overline{\text{CS0[5]}}$	O	P8	Bank 0 chip select 5. Asserted when xSEL[2:0] = 101b.
$\overline{\text{CS0[6]}}$	O	R9	Bank 0 chip select 6. Asserted when xSEL[2:0] = 110b.
$\overline{\text{CS0[7]}}$	O	U10	Bank 0 chip select 7. Asserted when xSEL[2:0] = 111b.
$\overline{\text{CS1[0]}}$	O	W6	Bank 0 chip select 0. Asserted when xSEL[2:0] = 000b.
$\overline{\text{CS1[1]}}$	O	V7	Bank 1 chip select 1. Asserted when xSEL[2:0] = 001b.
$\overline{\text{CS1[2]}}$	O	W8	Bank 1 chip select 2. Asserted when xSEL[2:0] = 010b.
$\overline{\text{CS1[3]}}$	O	W4	Bank 1 chip select 3. Asserted when xSEL[2:0] = 011b.
$\overline{\text{CS1[4]}}$	O	Y10	Bank 1 chip select 4. Asserted when xSEL[2:0] = 100b.
$\overline{\text{CS1[5]}}$	O	R7	Bank 1 chip select 5. Asserted when xSEL[2:0] = 101b.

Pin Name	Direction	Pin Number	Description
$\overline{CS1[6]}$	O	T9	Bank 1 chip select 6. Asserted when xSEL[2:0] = 110b.
$\overline{CS1[7]}$	O	V10	Bank 1 chip select 7. Asserted when xSEL[2:0] = 111b.
$\overline{CS2[0]}$	O	Y5	Bank 2 chip select 0. Asserted when xSEL[2:0] = 000b.
$\overline{CS2[1]}$	O	V8	Bank 2 chip select 1. Asserted when xSEL[2:0] = 001b.
$\overline{CS2[2]}$	O	Y3	Bank 2 chip select 2. Asserted when xSEL[2:0] = 010b.
$\overline{CS2[3]}$	O	V3	Bank 2 chip select 3. Asserted when xSEL[2:0] = 011b.
$\overline{CS2[4]}$	O	Y9	Bank 2 chip select 4. Asserted when xSEL[2:0] = 100b.
$\overline{CS2[5]}$	O	R8	Bank 2 chip select 5. Asserted when xSEL[2:0] = 101b.
$\overline{CS2[6]}$	O	U9	Bank 2 chip select 6. Asserted when xSEL[2:0] = 110b.
$\overline{CS2[7]}$	O	T6	Bank 2 chip select 7. Asserted when xSEL[2:0] = 111b.
$\overline{CS3[0]}$	O	Y7	Bank 3 chip select 0. Asserted when xSEL[2:0] = 000b.
$\overline{CS3[1]}$	O	W7	Bank 3 chip select 1. Asserted when xSEL[2:0] = 001b.
$\overline{CS3[2]}$	O	W3	Bank 3 chip select 2. Asserted when xSEL[2:0] = 010b.
$\overline{CS3[3]}$	O	W10	Bank 3 chip select 3. Asserted when xSEL[2:0] = 011b.
$\overline{CS3[4]}$	O	Y8	Bank 3 chip select 4. Asserted when xSEL[2:0] = 100b.
$\overline{CS3[5]}$	O	T8	Bank 3 chip select 5. Asserted when xSEL[2:0] = 101b.
$\overline{CS3[6]}$	O	T10	Bank 3 chip select 6. Asserted when xSEL[2:0] = 110b.
$\overline{CS3[7]}$	O	T7	Bank 3 chip select 7. Asserted when xSEL[2:0] = 111b.
XIN[0]	I	T14	Buffered input X[0]
XIN[1]	I	R6	Buffered input X[1]
YIN[0]	I	N11	Buffered input Y[0]
YIN[1]	I	V6	Buffered input Y[1]
XOUT[0]	O	U14	Bit 0 of buffered output X
XOUT[1]	O	T15	Bit 1 of buffered output X
XOUT[2]	O	P12	Bit 2 of buffered output X
XOUT[3]	O	U13	Bit 3 of buffered output X
YOUT[0]	O	N12	Bit 0 of buffered output Y
YOUT[1]	O	P11	Bit 1 of buffered output Y
YOUT[2]	O	M12	Bit 2 of buffered output Y
YOUT[3]	O	R11	Bit 3 of buffered output Y

Channel Pins

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
0A	U3	0B0	R03	0B1	U4	0B2	T3	0B3	T4
1A	T1	1B0	T2	1B1	R2	1B2	P1	1B3	R1
2A	P2	2B0	P3	2B1	N3	2B2	M3	2B3	N2
3A	U1	3B0	W2	3B1	V2	3B2	U2	3B3	V1
4A	L1	4B0	L2	4B1	M2	4B2	M1	4B3	N1
5A	N6	5B0	N7	5B1	P6	5B2	N5	5B3	N8
6A	L5	6B0	M5	6B1	M4	6B2	L4	6B3	L3
7A	R4	7B0	R5	7B1	P5	7B2	N4	7B3	P4
8A	M7	8B0	M8	8B1	M6	8B2	L7	8B3	L6
9A	L9	9B0	L10	9B1	L8	9B2	K8	9B3	K9
10A	J8	10B0	K7	10B1	J7	10B2	K6	10B3	J9
11A	H4	11B0	G4	11B1	F5	11B2	F6	11B3	G5
12A	K5	12B0	K4	12B1	K3	12B2	J5	12B3	J4
13A	H6	13B0	H5	13B1	J6	13B2	H7	13B3	G6
14A	J2	14B0	J1	14B1	H1	14B2	K1	14B3	K2
15A	D2	15B0	C1	15B1	D1	15B2	C3	15B3	C2
16A	H3	16B0	J3	16B1	H2	16B2	G2	16B3	G3
17A	F1	17B0	G1	17B1	E1	17B2	E2	17B3	F2
18A	F4	18B0	E3	18B1	E4	18B2	F3	18B3	D3
19A	C4	19B0	C6	19B1	D4	19B2	C5	19B3	D5
20A	A5	20B0	B5	20B1	B6	20B2	A7	20B3	A6
21A	B7	21B0	C7	21B1	C8	21B2	C9	21B3	B8
22A	A4	22B0	B2	22B1	B3	22B2	B4	22B3	A3
23A	A10	23B0	B10	23B1	B9	23B2	A9	23B3	A8
24A	F8	24B0	G8	24B1	F7	24B2	E8	24B3	F9
25A	E10	25B0	E9	25B1	D9	25B2	D10	25B3	C10
26A	D6	26B0	E6	26B1	E7	26B2	D8	26B3	D7
27A	G9	27B0	H9	27B1	H8	27B2	G10	27B3	F10
28A	H10	28B0	J10	28B1	K11	28B2	J11	28B3	H11
29A	G11	29B0	F11	29B1	G12	29B2	H12	29B3	F12
30A	E14	30B0	D13	30B1	D14	30B2	D15	30B3	E15
31A	E11	31B0	D11	31B1	C11	31B2	E12	31B3	D12

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Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
32A	E13	32B0	H13	32B1	F13	32B2	G13	32B3	F14
33A	B12	33B0	A12	33B1	A13	33B2	A11	33B3	B11
34A	B17	34B0	A18	34B1	A17	34B2	B19	34B3	B18
35A	C13	35B0	C12	35B1	B13	35B2	B14	35B3	C14
36A	A14	36B0	A15	36B1	A16	36B2	B16	36B3	B15
37A	D17	37B0	C16	37B1	D16	37B2	C15	37B3	C17
38A	F17	38B0	D18	38B1	F18	38B2	E17	38B3	E18
39A	F20	39B0	F19	39B1	E19	39B2	E20	39B3	G20
40A	H18	40B0	G18	40B1	G19	40B2	H19	40B3	J18
41A	D19	41B0	C19	41B1	C18	41B2	D20	41B3	C20
42A	J19	42B0	K19	42B1	K20	42B2	H20	42B3	J20
43A	H15	43B0	G15	43B1	H14	43B2	J15	43B3	H16
44A	K16	44B0	J17	44B1	J16	44B2	K18	44B3	K17
45A	H17	45B0	G16	45B1	F15	45B2	F16	45B3	G17
46A	J13	46B0	J12	46B1	K15	46B2	J14	46B3	K14
47A	L12	47B0	K12	47B1	K13	47B2	L13	47B3	L11
48A	M14	48B0	L15	48B1	L14	48B2	M15	48B3	M13
49A	R17	49B0	P17	49B1	N17	49B2	P16	49B3	R16
50A	L16	50B0	L18	50B1	L17	50B2	M17	50B3	M16
51A	N15	51B0	N13	51B1	N16	51B2	P15	51B3	N14
52A	L20	52B0	N20	52B1	M20	52B2	M19	52B3	L19
53A	U20	53B0	V20	53B1	U19	53B2	V19	53B3	W19
54A	P19	54B0	N19	54B1	M18	54B2	N18	54B3	P18
55A	T20	55B0	R20	55B1	P20	55B2	R19	55B3	T19
56A	U18	56B0	T17	56B1	T18	56B2	U17	56B3	R18
57A	U15	57B0	V17	57B1	V15	57B2	U16	57B3	V16
58A	Y14	58B0	W15	58B1	W16	58B2	Y16	58B3	Y15
59A	V13	59B0	V14	59B1	W14	59B2	W13	59B3	V12
60A	W17	60B0	W18	60B1	V18	60B2	Y17	60B3	Y18
61A	W12	61B0	W11	61B1	Y11	61B2	Y13	61B3	Y12
62A	T13	62B0	R14	62B1	P13	62B2	R13	62B3	R12
63A	T11	63B0	U12	63B1	T12	63B2	V11	63B3	U11

Power and Ground Pins

Pin Name	Pin Number	Description
V_{DD}	A2, A20, B1, E5, G14, P7, T16, W20, Y1, Y19	Power Supply
V_{SS}	A1, A19, B20, E16, G7, P14, T5, U5, W1, Y2, Y20, R15	Ground
NC	K10, V4, V5	No Connect

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	DESCRIPTION	VALUE	UNITS
V_{DD}	Supply voltage[2]	-0.3 to 4.8	V
V_{IO}	Input voltage any logic pin[2]	V_{SS}-0.3 to V_{DD}+0.3	V
V_{CH}	Input voltage any bussed pin[2]	V_{SS}-0.3 to V_{DD}+0.3	V
I_{IO}	Maximum dc I/O current any logic pin	-10 to 10	mA
P_D	Maximum power dissipation permitted @ T_C=125C[3]	5	W
T_J	Junction temperature	150	°C
θ_{JC}	Thermal resistance, junction to case	5	°C/W
T_{STG}	Storage temperature	-65 to 150	°C
ESD	ESD protection (human body model) Class 2	2000	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

2. All voltages are referenced to V_{SS}

3. Power dissipation capability depends on package characteristics and use environment.

RECOMMENDED OPERATING CONDITIONS

36-00-03-001   Aeroflex Microelectronics Solutions - HiRel

(Referenced to V_{SS})

SYMBOL	DESCRIPTION	CONDITIONS	VALUE	UNITS
V_{DD}	Supply voltage		3.0 to 3.6	V
V_{IN}	Input voltage any pin		0 to V_{DD}	V
T_C	Case operating temperature		-55 to 125	°C
t_R	Rise time, logic inputs	Transition from V_{IL} to V_{IH}	5	ns
t_F	Fall time, logic inputs	Transition from V_{IH} to V_{IL}	5	ns
I_{CH}	DC Continuous channel current		-60 to 60	mA

OPERATIONAL ENVIRONMENT

OPERATIONAL ENVIRONMENT		
PARAMETER	LIMIT	UNITS
TID	3.0E5	Rad(Si)
Single Event Latchup ImmunE (SEL)	≤100	MeV-cm^2/mg

POWER SUPPLY OPERATING CHARACTERISTICS (Pre and Post-Radiation)*
(V_{DD} = 3.3V $\pm$ 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

SYMBOL	DESCRIPTION	CONDITIONS		MIN	MAX	UNITS
I_{DD}	Active supply current	V_{DD}=3.6V The following pins are toggling once per period at *f*=18.67MHz: $\overline{RAMS}$, ASEL[1], BSEL[1]. BANK[0] at *f*=1.17MHz.		--	1.5	mA/ MHz
I_{DDS}	Standby supply current	V_{DD}=3.6V $\overline{ROMS}$=V_{DD}, $\overline{RAMS}$=V_{DD}	-55°C and +25°C	--	20	uA
			+125°C	--	250	uA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

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DC CHARACTERISTICS FOR LOGIC SIGNALS (Pre and Post-Radiation)*

(V_{DD} = 3.3V $\pm$ 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
V_{IH}	High-level input voltage	V_{DD} = 3.6V	2.0	--	V
V_{IL}	Low-level input voltage	V_{DD} = 3.0V	--	0.8	V
I_{IN}	Input leakage current	$V_{IN}=V_{DD}$, V_{DD} = 3.6V	--	1	uA
		$V_{IN}=V_{SS}$, V_{DD} = 3.6V	-1	--	
V_{OH}[1]	High-level output voltage	I_{OH}=-100uA, V_{DD} = 3.0V	V_{DD}-0.2	--	V
		I_{OH}=-24mA, V_{DD} = 3.0V	2.2	--	
V_{OL}[1]	Low-level output voltage	I_{OL}=100uA, V_{DD} = 3.0V	--	0.2	V
		I_{OL}=24mA, V_{DD} = 3.0V		0.6	
V_{BBM}[2]	Break before make voltage	Any two CS$m[n]$ signals R_L=50Ω, C_L=50pF	2.0	--	V
C_{IN}[3]	Input capacitance	V_{DD}=0V f=1MHz	--	TBD	pF
C_{OUT}[3]	Output capacitance	V_{DD}=0V f=1MHz	--	TBD	pF

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Output pins should not be shorted to V_{DD} when driven low nor to V_{SS} when driven high.

2. Guaranteed by design.

3. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.

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DC CHARACTERISTICS FOR BUSSED SIGNALS (Pre and Post-Radiation)*

(V_{DD} = 3.3V $\pm$ 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
C_{ON}[1]	Switch ON capacitance	Output is open f=1MHz, $0.1V_{DD} \leq V_I \leq 0.9V_{DD}$	--	17	pF
C_{OFF1}[1]	Switch OFF capacitance at input mA	Output is open f=1MHz	--	11	pF
C_{OFF2}[1]	Switch OFF capacitance at output mBn	Input is open f=1MHz	--	5	pF
R_{ON}[2]	Switch ON resistance	V_O=V_{SS}, V_{DD}, and V_{DD}/2 I_{IN}=40mA	--	11	Ω
$R_{ON(flat)}$[2]	Switch ON resistance flatness	V_O=V_{SS}, V_{DD}, and V_{DD}/2 I_{IN}=-40mA	--	5	Ω
I_{OFF}	Switch OFF leakage current	V_I=V_{SS} and V_O=V_{DD}, or V_I=V_{DD} and V_O=V_{SS}	-2	2	uA
I_{BHHL}[3]	Bus holder switch current high to low	Output is off	-500	-150	uA
I_{BHLH}[3]	Bus holder switch current low to high	Output is off	150	500	uA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed by design.

2. Guaranteed by device characterization.

3. Guaranteed by functional test only.

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AC CHARACTERISTICS (Pre and Post-Radiation)*

$(V_{DD} = 3.3V \pm 0.3V; V_{SS} \leq V_{IN} \leq V_{DD};$ -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered
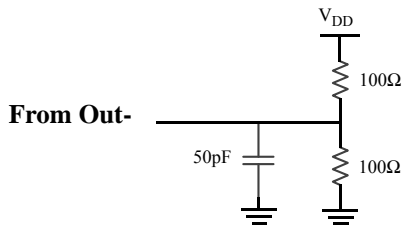
SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
$t_{P,BUS}$[1]	Bussed signals propagation delay	From any mA input to any mBn output	--	187	ps
t_{ON1}	Bussed signals ON time	From BANK to any mBn output; $\overline{ROMS}$ and $\overline{RAMS}$ static R_L=50Ω, C_L=50pF	1.7	6.2	ns
t_{OFF1}	Bussed signals OFF time	From BANK to any mBn output; $\overline{ROMS}$ and $\overline{RAMS}$ static R_L=50Ω, C_L=50pF	1.7	5.7	ns
t_{ON2}	Bussed signals ON time	From $\overline{ROMS}$ or $\overline{RAMS}$ to any mBn output; BANK static R_L=50Ω, C_L=50pF	1.7	6.2	ns
t_{OFF2}	Bussed signals OFF time	From $\overline{ROMS}$ or $\overline{RAMS}$ to any mBn output; BANK static R_L=50Ω, C_L=50pF	1.7	5.7	ns
t_{PLH1}	Logic output low-to-high delay	From ASEL, BSEL, or BANK to any $\overline{CS}$; $\overline{ROMS}$ and $\overline{RAMS}$ static R_L=50Ω, C_L=50pF	2.0	7.5	ns
t_{PHL1}	Logic output high-to-low delay	From ASEL, BSEL, or BANK to any $\overline{CS}$; $\overline{ROMS}$ and $\overline{RAMS}$ static R_L=50Ω, C_L=50pF	2.0	7.5	ns
t_{PLH2}	Logic output low-to-high delay	From $\overline{ROMS}$ or $\overline{RAMS}$ to any $\overline{CS}$; ASEL, BSEL, and BANK static R_L=50Ω, C_L=50pF	2.0	7.5	ns
t_{PHL2}	Logic output high-to-low delay	From $\overline{ROMS}$ or $\overline{RAMS}$ to any $\overline{CS}$; ASEL, BSEL, and BANK static R_L=50Ω, C_L=50pF	2.0	7.5	ns
t_{PLH3}	Buffered output low-to-high delay	From XIN to any XOUT or YIN to any YOUT R_L=50Ω, C_L=50pF	1.0	4.0	ns
t_{PHL3}	Buffered output high-to-low delay	From XIN to any XOUT or YIN to any YOUT R_L=50Ω, C_L=50pF	1.0	4.0	ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Not tested. The propagation delay through the channel is based upon the RC time constant of the maximum channel resistance and switch ON capacitance; 11Ω and 17pF.

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PARAMETER MEASUREMENT INFORMATION

Figure 2. Load Circuit

Figure 5. Logic and Buffered Output Delay

Notes:
1. The bus input is driven to V_{DD} or V_{SS} through a
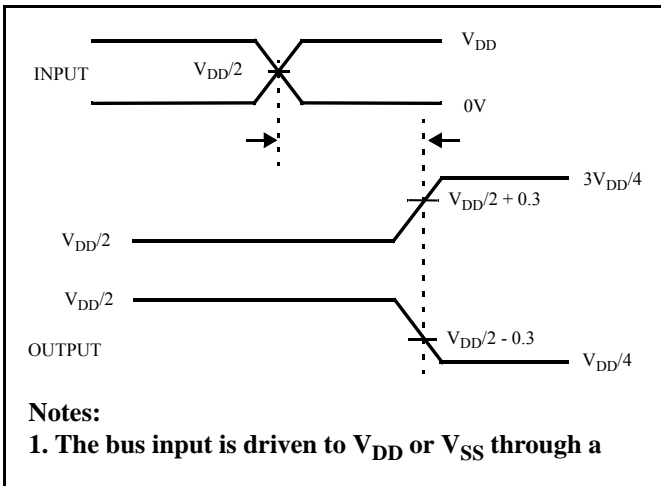
Figure 3. Bussed Signals Turn-on Time

Notes:
1. The bus input is driven to V_{DD} or V_{SS} through a
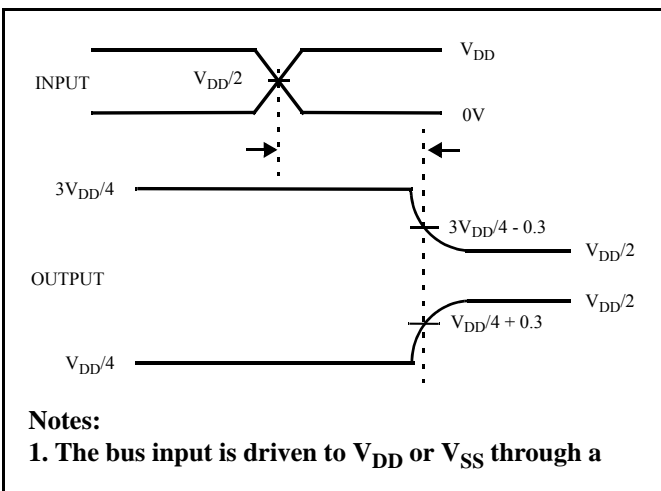
Figure 4. Bussed Signals Turn-off Time

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PACKAGING
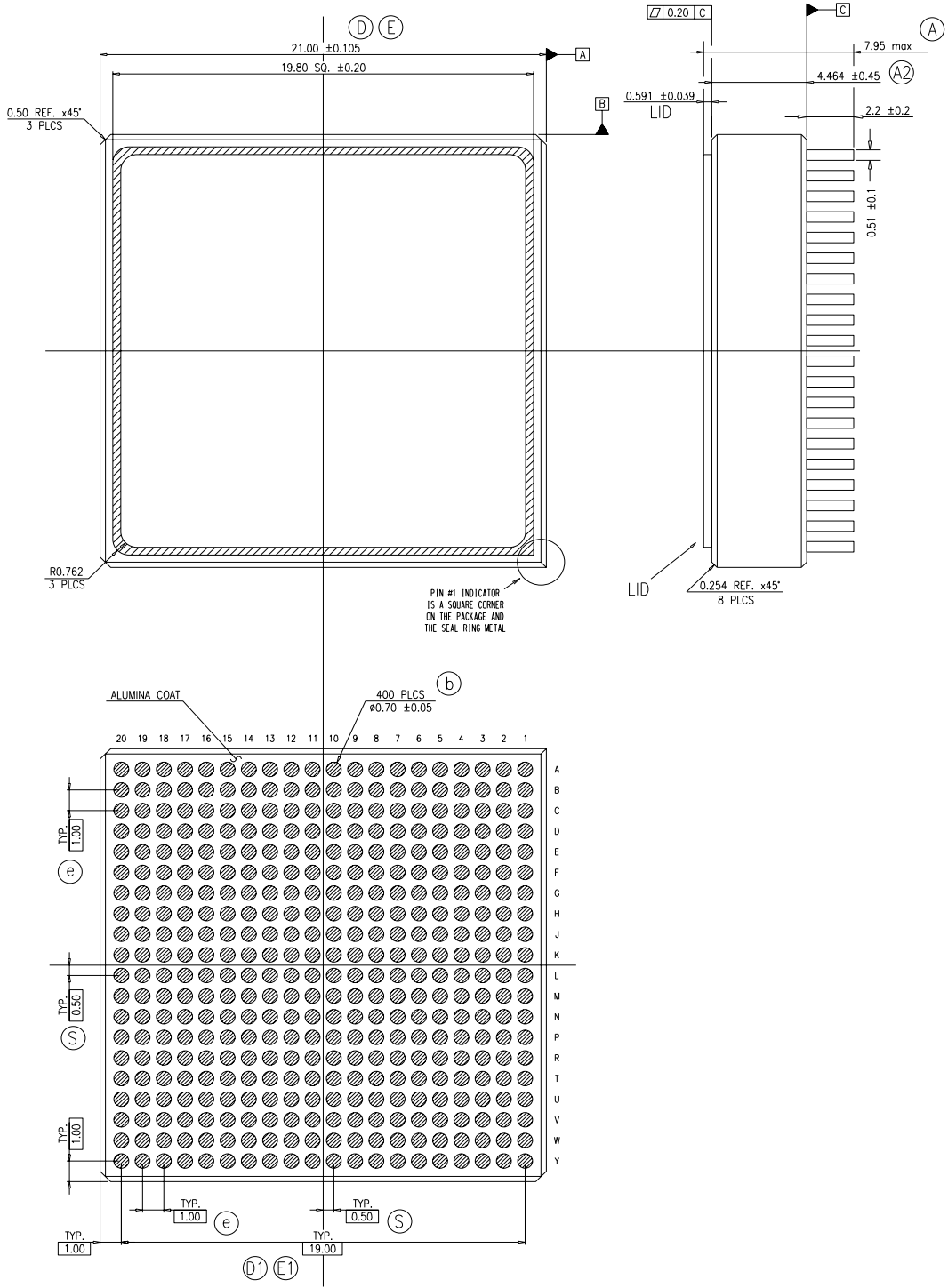
Figure 6. 400-pin Ceramic Land Grid Array Package (Case Outline Z)
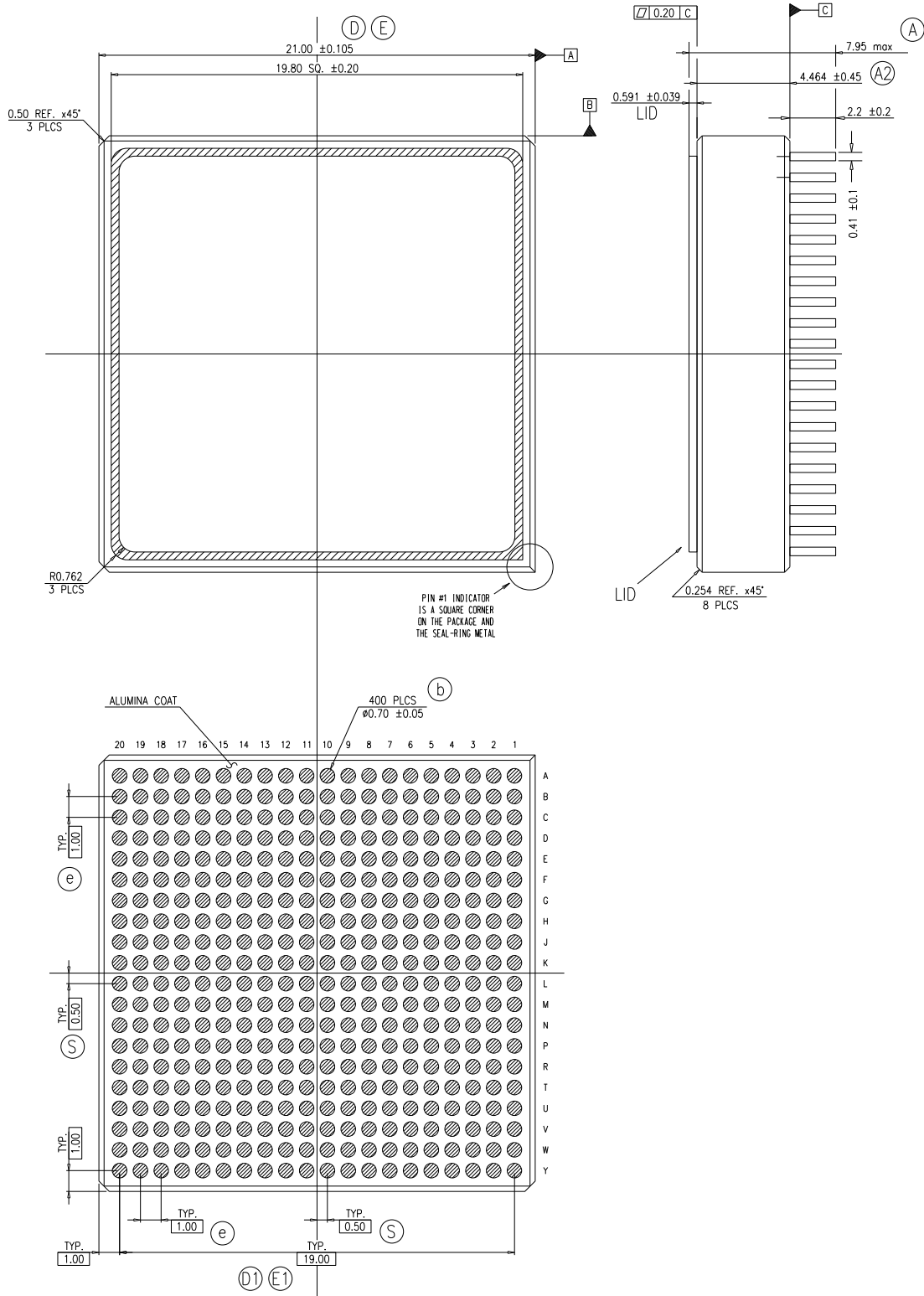
Figure 7. 400-pin Ceramic Column Grid Array Package (Case Outline S)

NOTES:
1. LID IS CONNECTED TO VSS.
2. UNITS ARE IN MILLIMETERS.

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Figure 8. 400-pin Ceramic Ball Grid Array Package (Case Outline C)

NOTES:
1. LID IS CONNECTED TO VSS.
2. UNITS ARE IN MILLIMETERS.

ORDERING INFORMATION

UT64BS1X433 Matrix-A

UT ********* - * * *

Lead Finish:
(A) = Hot Solder Dipped
(C) = Gold

Screening Level: **(NOTE 1 & 2)**
(P) = Prototype flow (Temperature Range: 25°C only)
(E) = HiRel flow (Temperature Range: -55°C to +125°C)

Case Outline:
(Z) = 400-Ceramic Land Grid Array
(S) = 400-Ceramic Column Grid Array
(C) = 400-Ceramic Ball Grid Array

Device Type:
(64BS1X433) = Matrix-A 64-Channel 1:4 Bus Switch
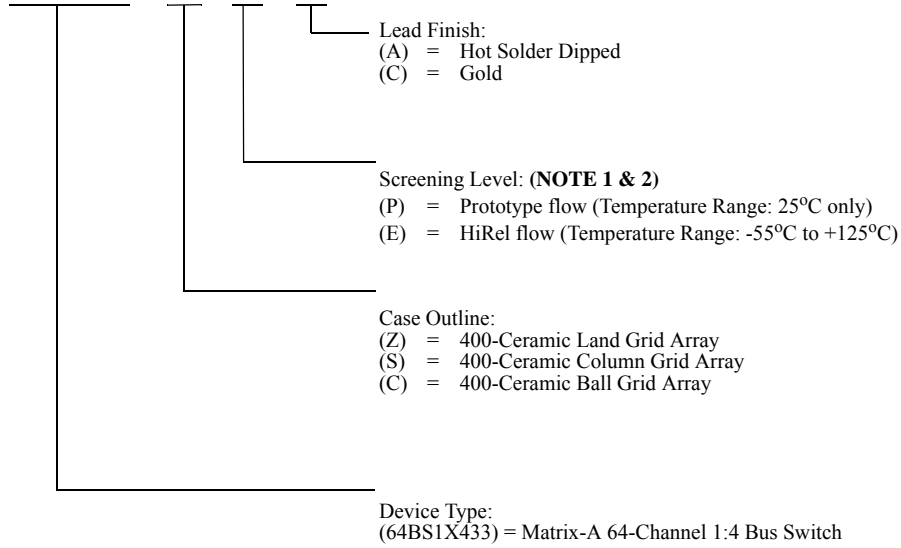
Notes:

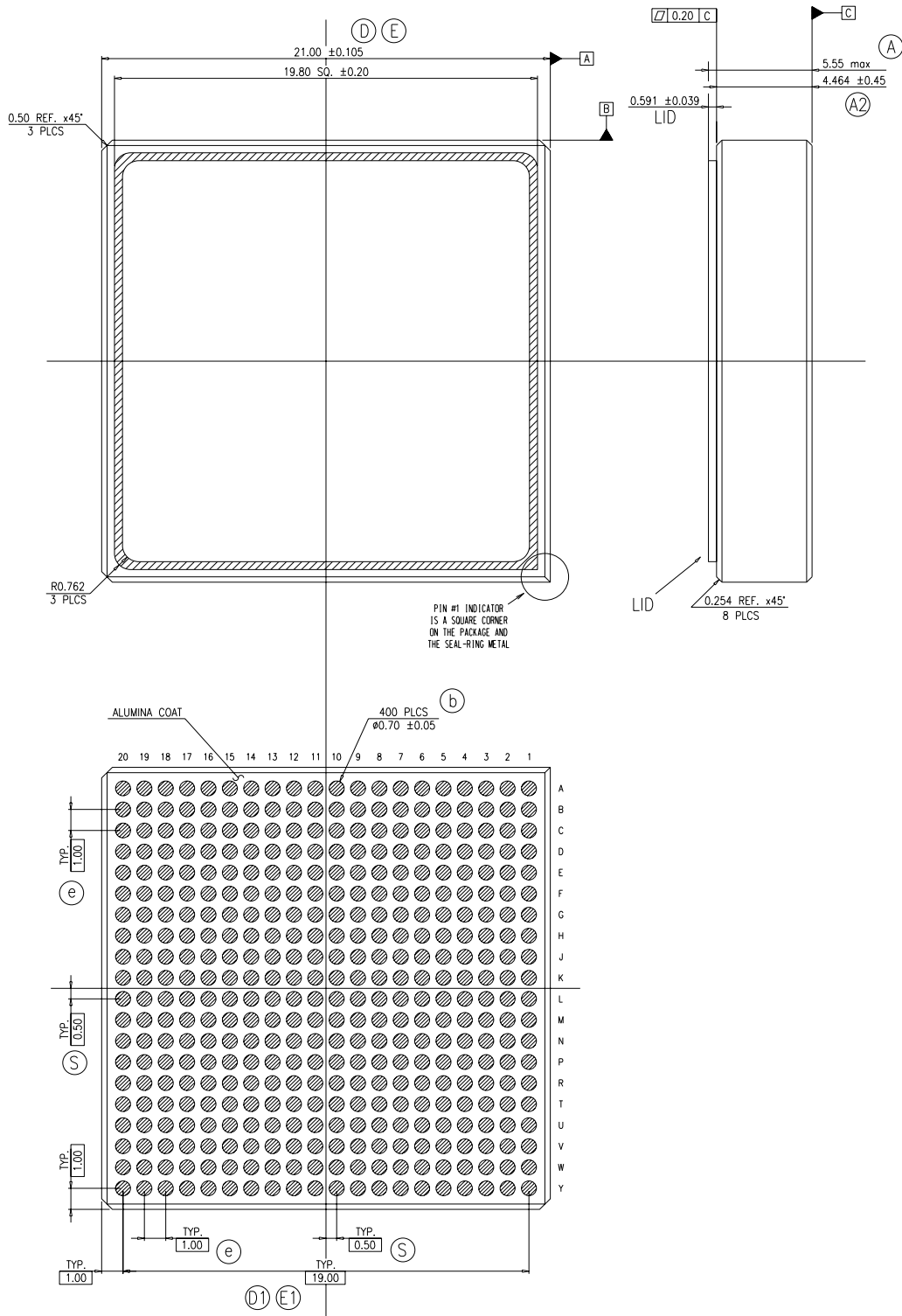1. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Radiation is neither tested nor guaranteed.

2. HiRel Flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

Package Option	Associated Lead Finish
(Z) 400-CLGA	(C) Gold
(S) 400-CCGA	(A) Hot Solder Dipped
(C) 400-CBGA	(A) Hot Solder Dipped

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UT64BS1X433 Matrix-A: SMD

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5962  -  XXXXX  **   *   *   *
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Lead Finish: (**NOTE 1**)
(C) = Gold

Case Outline: (**NOTE 2**)
(X) = 400-Ceramic Land Grid Array Package

Screening Level:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = UT64BS1X433 (Temperature range: -55°C to +125°C)

Drawing Number:
TBD

Total Dose:
(R) = 1E5 rad(Si)
(F) = 3E5 rad(Si)

Federal Stock Class Number: No Options
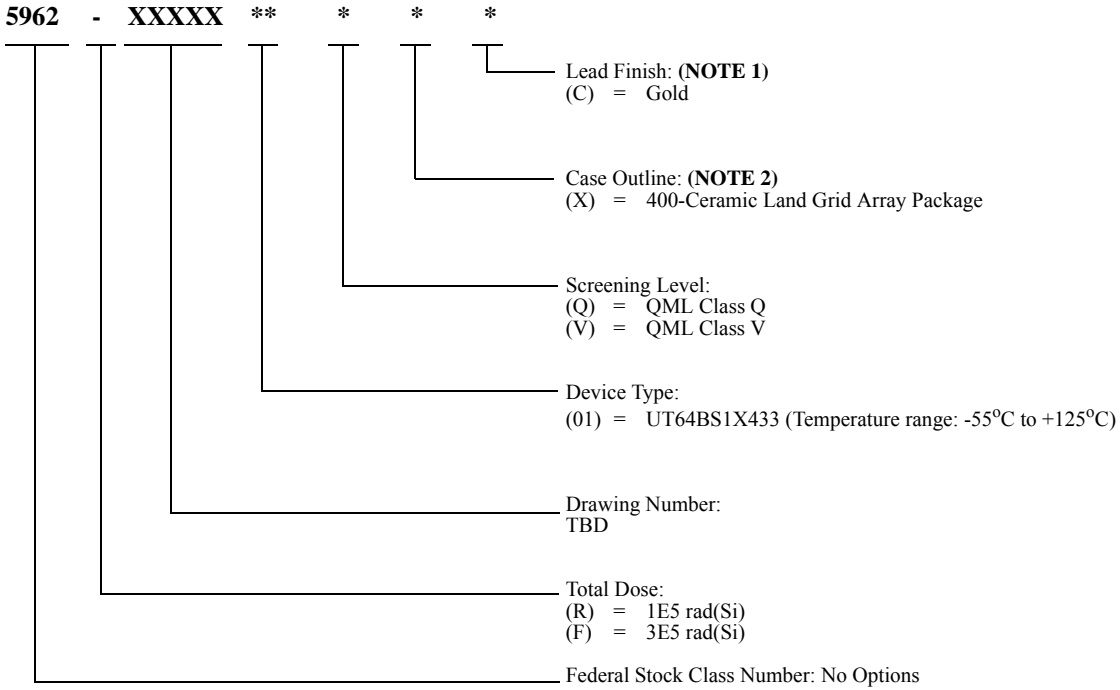
Notes:

1. Lead finish is "C" (gold) only.
2. Aeroflex offers Column Attachment as an additional service for the Ceramic Column Grid Array (Case outline "S"). If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.

Aeroflex Microelectronics Solutions - HiRel

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

www.aeroflex.com   info-ams@aeroflex.com

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