VERY LOW POWER CLOCK FOR 2011 NETBOOKS

9VRS4338D

General Description

The 9VRS4338D is a main clock for Intel Netbooks, conforming to the CK-NET specification. It is driven with a 14.31818MHz crystal and generates a variety of clocks, including an LCD clock. An SMBus interface allows full control of the device.

Recommended Application

CK-NET

Output Features

- 2 - 0.8V push-pull differential CPU pairs
- 3 - 0.8V push-pull differential SRC pairs
- 1 - 0.8V push-pull differential SATA/SRC pair
- 1 - 0.8V push-pull differential DOT96/SRC pair
- 1 - 0.8V push-pull differential LCD100 pair
- 1 - 0.8V push-pull differential CPU_ITP/SRC pair
- 3 - PCI (33MHz), 1 free-running
- 1 - 25MHz _PCI (33MHz)
- 1 - USB_48MHz
- 1 - REF, 14.318MHz

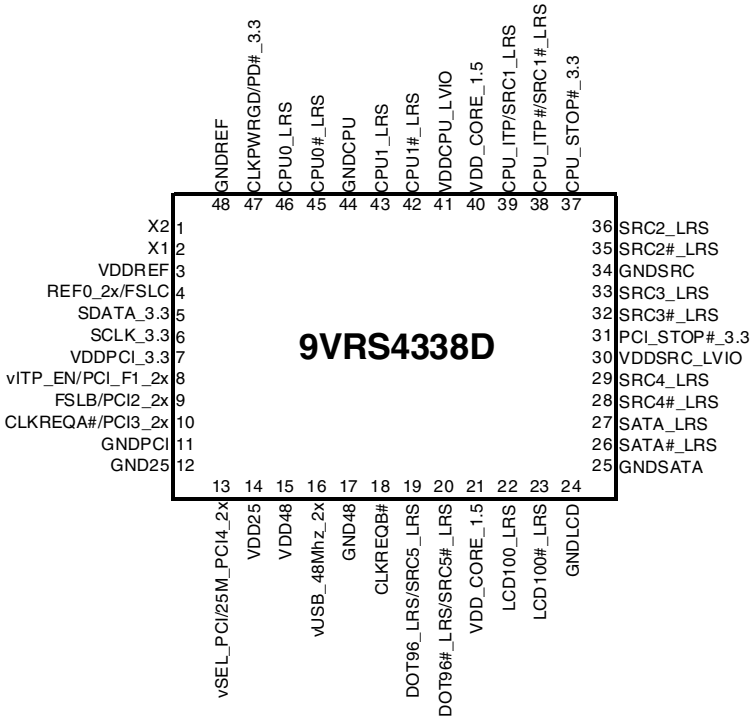
Features/Benefits

- 25M output can run in power down; Supports Wake_On_LAN
- Selectable spread % on CPU, SRC, PCI; Supports margining
- External 14.318MHz crystal; Supports tight ppm
- CLKREQ# pins; Support SRC power management
- Low power differential clock outputs; reduced power and board space
- Integrated 33 ohm series resistors on all differential outputs; reduced board space

Key Specifications

- CPU cycle-to-cycle jitter <85ps
- SRC/SATA cycle-to-cycle jitter <85ps
- SRC(1:4) are PCIe Gen2 compliant
- SRC5 is PCIe Gen1 compliant
- ±100ppm frequency accuracy on all clocks except 25M
- ±30ppm frequency accuracy on 25M

Pin Configuration



48-pin MLF, 6x6 mm, 0.4mm pitch

v prefix indicates internal 120KOhm pull down resistor

^ prefix indicates internal 120KOhm pull up resistor

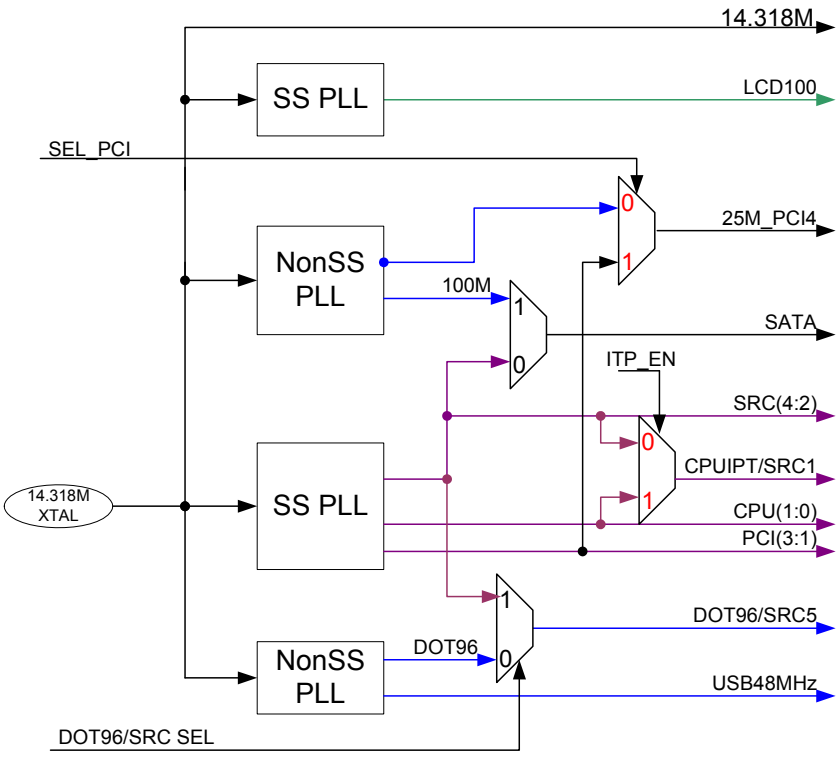
Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	X2	OUT	Crystal output, Nominally 14.318MHz
2	X1	IN	Crystal input, Nominally 14.318MHz.
3	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
4	REF0_2x/FSLC	I/O	2x strength 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
5	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
6	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
7	VDDPCI_3.3	PWR	Power supply for PCI clocks, nominal 3.3V
8	vITP_EN/PCI_F1_2x	I/O	ITP Enable Latched Input/Free Running PCI clock output. ITP_Enable Selects the functionality of the CPU_ITP/SRC output as follows: 1 = CPU_ITP output 0 = SRC output
9	FSLB/PCI2_2x	I/O	3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. / 3.3V PCI clock output.
10	CLKREQA#/PCI3_2x	I/O	Active low realtime input pin to enable SRC Outputs / PCI clock output. (pin function is programmable through SMBus). See CLKREQ# Control Table and SRC Power Management Table for details.
11	GNDPCI	PWR	Ground pin for the PCI outputs
12	GND25	PWR	Ground pin for the 25MHz outputs
13	vSEL_PCI/25M_PCI4_2x	I/O	SEL_PCI 3.3V latched input to select pin functionality for 25M_PCICLK3 output/25M or PCI clock output. This pin has an internal 120Kohm pulldown resistor. Latch functionality is as follows: 0 = 25MHz output 1 = 33.3MHz PCICLK
14	VDD25	PWR	Power pin for the 25MHz output.3.3V
15	VDD48	PWR	Power pin for the 48MHz output.3.3V
16	vUSB_48Mhz_2x	OUT	3.3V 48MHz USB clock output. This pin has an internal 120Kohm pull down resistor.
17	GND48	PWR	Ground pin for the 48MHz outputs
18	CLKREQB#	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = controlled outputs are enabled 1 = controlled outputs are Low/Low
19	DOT96_LRS/SRC5_LRS	OUT	True clock of push-pull DOT96 or SRC clock with integrated series resistor. No 50 ohm pull down needed. Default is DOT96. After powerup, this pin function may be changed to SRC via SMBus.
20	DOT96#_LRS/SRC5#_LRS	OUT	Complementary clock of push-pull DOT96 or SRC clock with integrated series resistor. No 50 ohm pull down needed. Default is DOT96. After powerup, this pin function may be changed to SRC via SMBus.
21	VDD_CORE_1.5	PWR	Power for PLL core components requiring 1.5V
22	LCD100_LRS	OUT	True clock of differential push-pull LCD100 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
23	LCD100#_LRS	OUT	Complementary clock of differential push-pull LCD100 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
24	GNDLCD	PWR	Ground pin for LCD clock output

Pin Descriptions (cont.)

25	GNDSATA	PWR	Ground pin for the SATA outputs
26	SATA#_LRS	OUT	Complementary clock of low power differential push-pull SATA clock pair with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
27	SATA_LRS	OUT	True clock of low power differential push-pull SATA clock pair with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
28	SRC4#_LRS	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
29	SRC4_LRS	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
30	VDDSRC_LVIO	PWR	VDD for SRC I/O. Nominally 1.05V to 1.5V from external power supply
31	PCI_STOP#_3.3	IN	Stops all stoppable PCI and SRC clocks at logic 0 level, when low. Free running PCI and SRC clocks are not effected by this input. This input is 3.3V tolerant.
32	SRC3#_LRS	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
33	SRC3_LRS	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
34	GNDSRC	PWR	Ground pin for the SRC outputs
35	SRC2#_LRS	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
36	SRC2_LRS	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
37	CPU_STOP#_3.3	IN	Stops stoppable CPU clocks when enabled. This is a 3.3V tolerant input.
38	CPU_ITP#/SRC1#_LRS	OUT	Complementary clock of low power differential CPU_ITP/SRC pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed. The pin function is determined by the latched value on ITP_EN: 0 = SRC0# 1 = CPU_ITP#
39	CPU_ITP/SRC1_LRS	OUT	True clock of low power differential CPU_ITP/SRC pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed. The pin function is determined by the latched value on ITP_EN: 0 = SRC0 1 = CPU_ITP
40	VDD_CORE_1.5	PWR	Power for PLL core components requiring 1.5V
41	VDDCPU_LVIO	PWR	VDD for CPU I/O. Nominally 1.05V to 1.5V from external power supply.
42	CPU1#_LRS	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
43	CPU1_LRS	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
44	GNDCPU	PWR	Ground pin for the CPU outputs
45	CPU0#_LRS	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
46	CPU0_LRS	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
47	CLKPWRGD/PD#_3.3	IN	This 3.3V LVTTL input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
48	GNDREF	PWR	Ground pin for the REF outputs.

Block Diagram

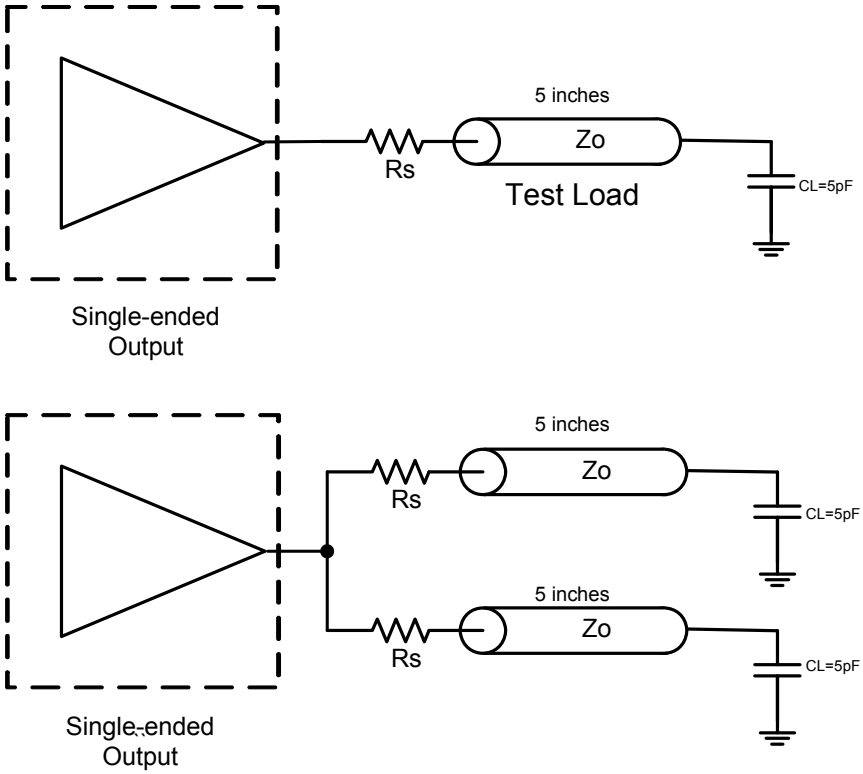


Series Resistors for Single Ended Outputs

D.C.Drive Strength	Number of Loads to Drive	Match Point for N & P Voltage / Current (mA)	Number of Loads Actually Driven.		
			1 Load Rs =	2 Loads Rs=	3 Loads Rs =
	1	0.56 / 33 (17Ω)	33Ω [39Ω]	NA	NA
	2	0.92 / 66 (14Ω)	39Ω [43Ω]	22Ω [27Ω]	NA

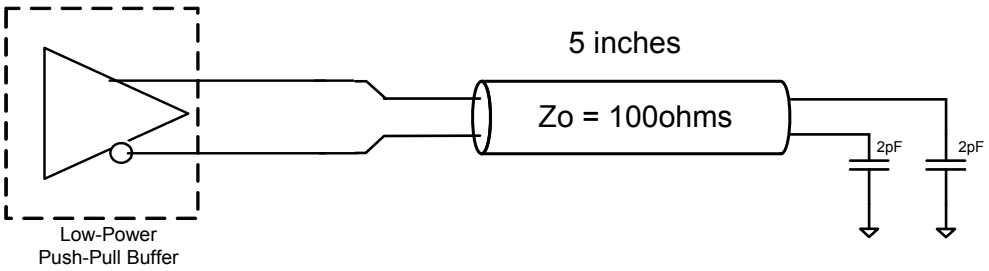
Notes:

1. Preferred drive strengths using CK505 clock sources. Transmission lines to load do not share series resistors.
2. Desktop/Mobile Platforms with Zo = 50/55 ohms use the first resistor value.
3. Systems with Zo = 60 ohms use the resistor values in brackets [ ].



The singled-ended outputs of the 9VRS4338 can drive 2 loads. If the output is driving one load, the resistor value is adjusted according to the “Series Resistors for Single-Ended Outputs Table. When driving two loads, both load traces must be equal in length.

9VRS4338 Differential Test Load



Driving LVDS inputs with the 9VRS4338

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
Cc	0.1 uF	0.1 uF	
Vcm	1.2 volts	1.2 volts	

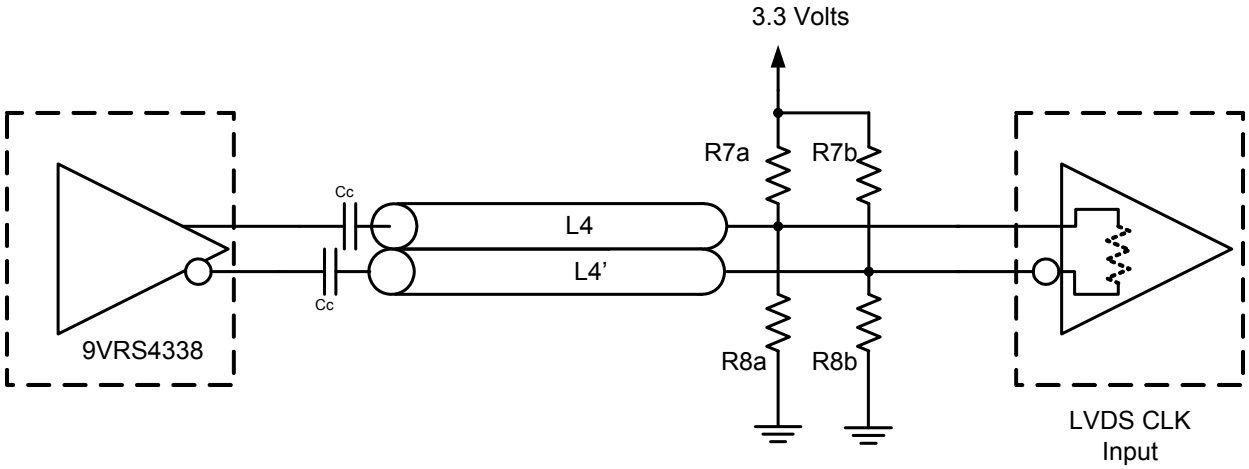


Table 1: CPU/SRC/PCI PLL Spread/Frequency Selection Table REV D

CPU/SRC/PCI Center Spread (B1b6)	SS1 (B1b5)	SS0 (B1b4)	FS_LC (B0b7)	FS_LB (B0b6)	SPREAD	CPU MHz	SRC MHz	PCI MHz
0	0	0	0	0	-0.50%	133.33	100.00	33.33
0	0	0	0	1	-0.50%	167.67	100.00	33.33
0	0	0	1	0	-0.50%	100.00	100.00	33.33
0	0	0	1	1	-0.50%	200.00	100.00	33.33
0	0	1	0	0	-0.40%	133.33	100.00	33.33
0	0	1	0	1	-0.40%	167.67	100.00	33.33
0	0	1	1	0	-0.40%	100.00	100.00	33.33
0	0	1	1	1	-0.40%	200.00	100.00	33.33
0	1	0	0	0	-0.30%	133.33	100.00	33.33
0	1	0	0	1	-0.30%	167.67	100.00	33.33
0	1	0	1	0	-0.30%	100.00	100.00	33.33
0	1	0	1	1	-0.30%	200.00	100.00	33.33
0	1	1	0	0	OFF	133.33	100.00	33.33
0	1	1	0	1	OFF	167.67	100.00	33.33
0	1	1	1	0	OFF	100.00	100.00	33.33
0	1	1	1	1	OFF	200.00	100.00	33.33
1	0	0	0	0	+/-0.25%	133.33	100.00	33.33
1	0	0	0	1	+/-0.25%	167.67	100.00	33.33
1	0	0	1	0	+/-0.25%	100.00	100.00	33.33
1	0	0	1	1	+/-0.25%	200.00	100.00	33.33
1	0	1	0	0	+/-0.20%	133.33	100.00	33.33
1	0	1	0	1	+/-0.20%	167.67	100.00	33.33
1	0	1	1	0	+/-0.20%	100.00	100.00	33.33
1	0	1	1	1	+/-0.20%	200.00	100.00	33.33
1	1	0	0	0	+/-0.15%	133.33	100.00	33.33
1	1	0	0	1	+/-0.15%	167.67	100.00	33.33
1	1	0	1	0	+/-0.15%	100.00	100.00	33.33
1	1	0	1	1	+/-0.15%	200.00	100.00	33.33
1	1	1	0	0	OFF	133.33	100.00	33.33
1	1	1	0	1	OFF	167.67	100.00	33.33
1	1	1	1	0	OFF	100.00	100.00	33.33
1	1	1	1	1	OFF	200.00	100.00	33.33

Note: Changing default spread amounts or type will impact SRC clocks, too. The default -0.5% downspread is recommended for SRC.

Table 2: LCD Spread Selection Table Rev B/C/D

FS2 (B1b3)	FS1 (B1b2)	FS0 (B1b1)	LCD Center Spread (B1b0)	SPREAD %	LCD100 MHz
0	0	0	0	OFF	Reserved
0	0	1	0	OFF	100.00
0	1	0	0	-0.50%	100.00
0	1	1	0	-1.0%	100.00
1	0	0	0	-1.5%	100.00
1	0	1	0	-2.0%	100.00
1	**1**	**0**	**0**	**-2.50%**	**100.00**
1	1	1	0	OFF	Reserved
0	0	0	1	OFF	Reserved
0	0	1	1	OFF	100.00
0	1	0	1	+/-0.25%	100.00
0	1	1	1	+/-0.5%	100.00
1	0	0	1	+/-0.75%	100.00
1	0	1	1	+/-1.0%	100.00
1	1	0	1	+/-1.25%	100.00
1	1	1	1	OFF	Reserved

CPU Power Management Table

CLKPWRGD/PD#_3.3	SMBus Register OE	CPU_STOP#	CPU (0, 1, ITP)	
			True O/P	Comp. O/P
1	Enable	**1**	Running	Running
1	Enable	**0**	High	Low
0	X	X	Low/20K	Low
X	**Disable**	X	Low/20K	Low

DOT96 and SATA Power Management Table

CLKPWRGD/PD#_3.3	SMBus Register OE	SATA		DOT96	
		True O/P	Comp. O/P	True O/P	Comp. O/P
1	Enable	Running	Running	Running	Running
0	Enable	Low/20K	Low	Low/20K	Low
X	**Disable**	Low/20K	Low	Low/20K	Low

SRC Power Management Table

CLKPWRGD/PD#_3.3	SMBus Register OE	CLKREQx#	SRC controlled by CLKREQx#		SRC not controlled by CLKREQx#	
			True O/P	Comp. O/P	True O/P	Comp. O/P
1	Enable	0	Running	Running	Running	Running
1	Enable	1	Low/20K	Low	Running	Running
0	Enable	X	Low/20K	Low	Low/20K	Low
X	**Disable**	X	Low/20K	Low	Low/20K	Low

SIngle-ended Management Table

CLKPWRGD/PD#_3.3	SMBus Register OE	PCI_STOP#	PCI_F1, PCI2, 25M_PCI4 = PCI4		CLKREQA#/PCI3 = PCI3		25M_PCI4 = 25MHz		REF	USB_48
			Free-run	Stoppable	Free-run	Stoppable	WLAN Enabled	WLAN Disabled		
1	Enable	**1**	Running	Running	Running	Running	Running	Running	Running	Running
1	Enable	**0**	Running	Low	Running	Low	Running	Running	Running	Running
0	Enable	X	**Hi-Z**	**Hi-Z**	**Low**	**Low**	Running	**Hi-Z**	**Hi-Z**	**Hi-Z**
X	**Disable**	X	**Hi-Z**	**Hi-Z**	**Hi-Z**	**Hi-Z**	**Hi-Z**	**Hi-Z**	**Hi-Z**	**Hi-Z**

CLKREQ# Control Table

CLKREQ#	SRC controlled
A	SRC1, 2
B	SRC3, 4

NOTE: SMBus selects configuration

General SMBus Serial Interface Information for 9VRS4338D

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D3_{(H)}$	$D2_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select, PD Config and SATA Source Select Register

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	FSLC	Freq Select Bit 1	R	See Table 1: CPU PLL Frequency Selection Table		Latch
Bit 6	FSLB	Freq Select Bit 0	R			Latch
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	SATA_SEL	Selects SATA=SRC or Non-SS	RW	Follows SRC	SATA PLL (NonSS)	0
Bit 0	PD Config	Forces "cold" start during PD	RW	Reset and Relatch	Normal PD# mode	1

SMBus Table: CPU, LCD SS and DOT96/SRC5 Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	DOT96/SRC5 SEL	Selects DOT96 or SRC5	RW	DOT96	SRC5	0
Bit 6	CPU/SRC/PCI Center SS En	Enables Center Spread for	RW	Down Spread	Center Spread	0
Bit 5	CPU/SRC/PCI SS1	CPU/SRC/PCI SS Mag. MSB	RW	See Table 1 for Details. Default is -0.5% down spread when spread is enabled		0
Bit 4	CPU/SRC/PCI SS0	CPU/SRC/PCI SS Mag. LSB	RW			0
Bit 3	LCD SS2	LCD SS Magnitude MSB	RW	See Table 2 for Details.		1
Bit 2	LCD SS1	LCD SS Magnitude	RW			1
Bit 1	LCD SS0	LCD SS Magnitude LSB	RW			0
Bit 0	LCD Center SS En	Enables Center Spread for LCD	RW	Down Spread	Center Spread	0

SMBus Table: Output Enable Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	REF0 OE	Output Enable	RW	Disable	Enable	1
Bit 6	USB_48MHz OE	Output Enable	RW	Disable	Enable	1
Bit 5	Reserved					1
Bit 4	25M_PCI4 OE	Output Enable	RW	Disable	Enable	1
Bit 3	PCI3 OE	Output Enable	RW	Disable	Enable	1
Bit 2	PCI2 OE	Output Enable	RW	Disable	Enable	1
Bit 1	PCI_F1 OE	Output Enable	RW	Disable	Enable	1
Bit 0	Reserved					1

SMBus Table: Output Enable Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					1
Bit 4	Reserved					1
Bit 3	Reserved					1
Bit 2	LCD CLK OE	Output Enable	RW	Disable	Enable	1
Bit 1	SRC4 OE	Output Enable	RW	Disable	Enable	1
Bit 0	SATA OE	Output Enable	RW	Disable	Enable	1

SMBus Table: Output Enable and SS Enable Control Register

Byte 4	Name	Control Function		0	1	Default
Bit 7	SRC3 OE	Output Enable	RW	Disable	Enable	1
Bit 6	SRC2 OE	Output Enable	RW	Disable	Enable	1
Bit 5	CPU_ITP/SRC1 OE	Output Enable	RW	Disable	Enable	1
Bit 4	DOT96/SRC5 OE	Output Enable	RW	Disable	Enable	1
Bit 3	CPU1 OE	Output Enable	RW	Disable	Enable	1
Bit 2	CPU0 OE	Output Enable	RW	Disable	Enable	1
Bit 1	CPU/SRC PLL SS EN	Output Enable	RW	SS OFF	SS ON @ -0.5%	1
Bit 0	Reserved					1

SMBus Table: CLKREQ_A# and CLKREQB# Mapping

Byte 5	Name	Control Function		0	1	Default
Bit 7	CLKREQ_A# EN	Pin 10 Configuration	RW	Pin 10 = PCI3	Pin 10 = CLKREQ	0
Bit 6	CLKREQ_A# MAP	MAP CLKREQ_A# to SRC	RW	SRC1 Controlled	SRC2 Controlled	0
Bit 5	Reserved					0
Bit 4	CLKREQ_B# MAP	MAP CLKREQ_B# to SRC	RW	SRC3 Controlled	SRC4 Controlled	0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: SRC STOP Control Register

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	SRC STOP EN	SRC stop with PCI_STOP		Free-running	SRC Stoppable	0

SMBus Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	D rev = 0010		0
Bit 6	RID2		R			0
Bit 5	RID1		R			1
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = ICS/IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Reserved

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Byte Count Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is 0A = 10 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			1
Bit 0	BC0		RW			0

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9VRS4338D. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDD	Supply Voltage			3.9	V	1,4
Maximum Supply Voltage	VDD_CORE_1.5	Supply Voltage			1.9	V	1,4
Maximum Supply Voltage	VDD_LVIO	Supply Voltage			1.9	V	1,4
Maximum Input Voltage	V_{IH}	3.3V Inputs, including SMBus			3.9	V	1,2,4
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5			V	1,4
Storage Temperature	Ts	-	-65		150	°C	4
Case Temperature	Tcase	-			115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	3,4

AC Electrical Characteristics–CPU, SRC, SATA, DOT96MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	tSLR	Differential Measurement	2.5	3.2	4	V/ns	1,2
Falling Edge Slew Rate	tFLR	Differential Measurement	2.5	3.1	4	V/ns	1,2
Slew Rate Variation	tSLVAR	Single-ended Measurement		12.4	20	%	1
Maximum Output Voltage	VHIGH	Includes overshoot		869	1150	mV	1
Minimum Output Voltage	VLOW	Includes undershoot	-300			mV	1
Differential Voltage Swing	VSWING	Differential Measurement	300			mV	1
Crossing Point Voltage	VXABS	Single-ended Measurement	300	364	550	mV	1,3,4
Crossing Point Variation	VXABSVAR	Single-ended Measurement		32	140	mV	1,3,5
Duty Cycle	DCYC	Differential Measurement	45	49.8	55	%	1
CPU Jitter - Cycle to Cycle	CPUJC2C	Differential Measurement		46.1	85	ps	1
SRC Jitter - Cycle to Cycle	SRCJC2C	Differential Measurement		45.9	85	ps	1
SATA Jitter - Cycle to Cycle	SATAJC2C	Differential Measurement		52.1	85	ps	1
DOT Jitter - Cycle to Cycle	DOTJC2C	Differential Measurement		110.7	250	ps	1
CPU[1:0] Skew	CPU10SKEW	Differential Measurement		32	100	ps	1,6
CPU[2_ITP:0] Skew	CPU20SKEW	Differential Measurement		53	150	ps	1,6
SRC(2:4) Skew	SRC24SKEW	Differential Measurement		53	250	ps	1
SRC(1:5) Skew	SRC15SKEW	Differential Measurement		142	500	ps	1

Notes:

Notes: T_A = 0 - 85°C; V_{DD} = 3.3 V +/-5%; C_L=2pF, Rs=0Ω (unless specified otherwise)

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] Slew rate emastured through V_swing voltage range centered about differential zero

[4] Vcross is defined at the voltage where Clock = Clock#.

[5] Only applies to the differential rising edge (Clock rising, Clock# falling.)

[6] CPU group skew is nominally 0ps.

Electrical Characteristics - Phase Jitter

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1 REFCLK phase jitter		29	86	ps	1,2,3
	$t_{jphPCIe2Lo}$	PCIe Gen 2 REFCLK phase jitter Lo-band content		1.1	3	ps (RMS)	1,2,4
	$t_{jphPCIe2Hi}$	PCIe Gen 2 REFCLK phase jitter Hi-band content		1.9	3.1	ps (RMS)	1,2,4

Notes on Phase Jitter:

[1] See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

[2] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1^{-12}

[3] Applies to all SRC outputs.

[4] Applies to SRC(1:4) outputs.

Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	25	85	°C	
Supply Voltage	VDD	Supply Voltage	3.135	3.3	3.465	V	
	VDD_CORE_1.5	Supply Voltage	1.425	1.5	1.575	V	
	VDD_LVIO	Supply Voltage	0.9975	1.05	1.575	V	
Input High Voltage	V_{IHSE}	Single-ended 3.3V inputs	2		V_{DD} + 0.3	V	7
Input Low Voltage	V_{ILSE}	Single-ended 3.3V inputs	V_{SS} - 0.3		0.8	V	7
Latched Input High Voltage	V_{IH_LI}	Single-ended 3.3V Latched Inputs	2		VDD + 0.3	V	
Latched Input Low Voltage	V_{IL_LI}	Single-ended 3.3V Latched Inputs	V_{SS} - 0.3		0.8	V	
Low Threshold Latched Input-High Voltage	V_{IH_FS}	Low threshold inputs (FS(C:B))	0.7		VDD+0.3	V	
Low Threshold Latched Input-Low Voltage	V_{IL_FS}	Low threshold inputs (FS(C:B))	V_{SS} - 0.3		0.35	V	
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND	-5		5	uA	6
Input Leakage Current	I_{INRES}	Inputs with pull up or pull down resistors V_{IN} = V_{DD} , V_{IN} = GND	-200		200	uA	
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4			V	5
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA			0.4	V	5
Operating Supply Current	$I_{DDOP3.3}$	Full Active, C_L = Full load; IDD 3.3V		17.0	25	mA	
	$I_{DDOP1.5}$	Full Active, C_L = Full load; IDD 1.5V		29.5	35	mA	
	$I_{DDOP1.05}$	Full Active, C_L = Full load; IDD LVIO		31.4	35	mA	
Powerdown Current	$I_{DDPD3.3}$	Power down mode, 3.3V Rail		0.3	1	mA	9
	$I_{DDPD1.5}$	Power down mode, 1.5V Rail		0.4	1	mA	9
	$I_{DDPDLVIO}$	Power down mode, 1.05V Rail		0.0	0.01	mA	9
Wake-On-Lan Current	$I_{DDWOL3.3}$	Wake On Lan mode, 3.3V Rail		4.0	5	mA	10
	$I_{DDWOL1.5}$	Wake On Lan mode, 1.5V Rail		9.0	12	mA	10
	$I_{DDWOLLVIO}$	Wake On Lan mode, LVIO Rail		0.0	0.01	mA	10
Input Frequency	F_i	V_{DD} = 3.3 V			15	MHz	8
Pin Inductance	L_{pin}				7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	
	C_{OUT}	Output pin capacitance			6	pF	
	C_{INX}	X1 & X2 pins			6	pF	
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	
Tstop_CR_off	T_{CROFF}	Output stop after CLKREQ# deasserted	2		3	Clocks	
Trun_CR_on	T_{CRON}	Output run after CLKREQ# asserted	2		3	Clocks	
Tstop	T_{STOP}	CPU or PCI stop after CPU or PCI STOP# assertion	2		3	Clocks	
Trun	T_{RUN}	CPU or PCI run after CPU or PCI STOP# de-assertion	2		3	Clocks	
Tfall_SE	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%			10	ns	
Trise_SE	T_{RISE}				10	ns	
SMBus Voltage	V_{DD}		2.7	3.3	3.6	V	
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4			mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	
Maximum SMBus Operating Frequency	F_{SMBUS}				100	kHz	
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	31.5	33	kHz	

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1] Intentionally blank

[2] Maximum VIH is not to exceed VDD

[3] Human Body Model

[4] Operation under these conditions is neither implied, nor guaranteed.

[5] Signal is required to be monotonic in this region.

[6] Input leakage current does not include inputs with pull-up or pull-down resistors

[7] 3.3V referenced inputs are: PCI_STOP#, CPU_STOP#, ITP_EN, SCLK, SDATA, CLKPWRgD/PD#, SEL_PCI and CLKREQ# inputs if selected.

[8] For margining purposes only. Normal operation should have Fin = 14.318MHz +/-50ppm

[9] Standard powerdown with Wake on LAN disabled.

[10] Powerdown with Wake on LAN enabled

Electrical Characteristics–PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH}@MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	1.4	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	1.5	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	47.7	55	%	1
Pin to Pin Skew	t_{skew}	V_T = 1.5 V		206	250	ps	1
Intentional PCI to PCI delay	t_{skew}	V_T = 1.5 V	100	200	200	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		139	500	ps	1

Electrical Characteristics–USB48MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH}@MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	1.4	2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	1.4	2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	47.3	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		123	350	ps	1

Electrical Characteristics–25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-30	0	30	ppm	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH}@MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	0.5	1.4	2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	0.5	1.6	2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	49.3	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		170	200	ps	1

Electrical Characteristics–REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Output High Voltage	VOH	IOH = -1 mA	2.4			V	1
Output Low Voltage	VOL	IOL = 1 mA			0.4	V	1
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	29		27	mA	1
Rising Edge Slew Rate	tSLR	Measured from 0.8 to 2.0 V	1	1.5	4	V/ns	1
Falling Edge Slew Rate	tFLR	Measured from 2.0 to 0.8 V	1	1.6	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	50.1	55	%	1
Jitter, Cycle to cycle	tjcyc-cyc	VT = 1.5 V		138	1000	ps	1

Notes for PCI, USB48M, 25M and 14.318M outputs

T_A = 0 - 85°C; V_{DD} = 3.3 V +/-5%; C_L=5pF, Rs is according to Data Sheet Loading Table for 1 load (unless specified otherwise)

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

[3] The average period over any 1us period of time

Single-ended Clock Tolerances No Spread- Spec

	REF	PCI	48M	25M	
PPM tolerance	100	100	100	30	ppm
Cycle to Cycle Jitter	1000	500	350	200	ps
Spread	0.00%	0.00%	0.00%	0.00%	%

Clock Periods - Single-ended Outputs with Spread Spectrum Disabled - Spec

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
REF	14.318	68.83429		69.83429	69.84128	69.84826		70.84826	ns	1,2
PCI	33.333	29.49700		29.99700	30.00000	30.00300		30.50300	ns	1,2
48M	48.000	20.48125		20.83125	20.83333	20.83542		21.18542	ns	1,2
25M	25.000	39.79880		39.99880	40.00000	40.00120		40.20120	ns	1,2

Single-ended Clock Tolerances with Spread Spectrum Enabled - Spec

	REF	PCI	48M	25M	
PPM tolerance	100	100	100	30	ppm
Cycle to Cycle Jitter	1000	500	350	200	ps
Spread	0.00%	-0.50%	0.00%	0.00%	%

Clock Periods - Single-ended Outputs with Spread Spectrum Enabled - Spec

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
REF	14.318	N/A							ns	1,2
PCI	33.250	29.49718	29.99718	30.07218	30.07519	30.07218	30.14718	30.64718	ns	1,2
48M	48.000	N/A							ns	1,2
25M	25.000	N/A							ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.
[2] All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 14.31818MHz.

Differential Clock Tolerances

	CPU	SRC	DOT96	SATA	
PPM tolerance	100	100	100	100	ppm
Cycle to Cycle Jitter	85	85	250	85	ps
Spread	-0.50%	-0.50%	0.00%	0.00%	%

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	100.00	9.91400		9.99900	10.00000	10.00100		10.08600	ns	1,2
	133.33	7.41425		7.49925	7.50000	7.50075		7.58575	ns	1,2
	166.67	5.91440		5.99940	6.00000	6.00060		6.08560	ns	1,2
	200.00	4.91450		4.99950	5.00000	5.00050		5.08550	ns	1,2
	266.67	3.66462		3.74962	3.75000	3.75037		3.83537	ns	1,2
	333.33	2.91470		2.99970	3.00000	3.00030		3.08530	ns	1,2
	400.00	2.41475		2.49975	2.50000	2.50025		2.58525	ns	1,2
SRC	100.00	9.91400		9.99900	10.00000	10.00100		10.08600	ns	1,2
SATA	100.00	9.91400		9.99900	10.00000	10.00100		10.08600	ns	1,2
DOT96	96.00	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2

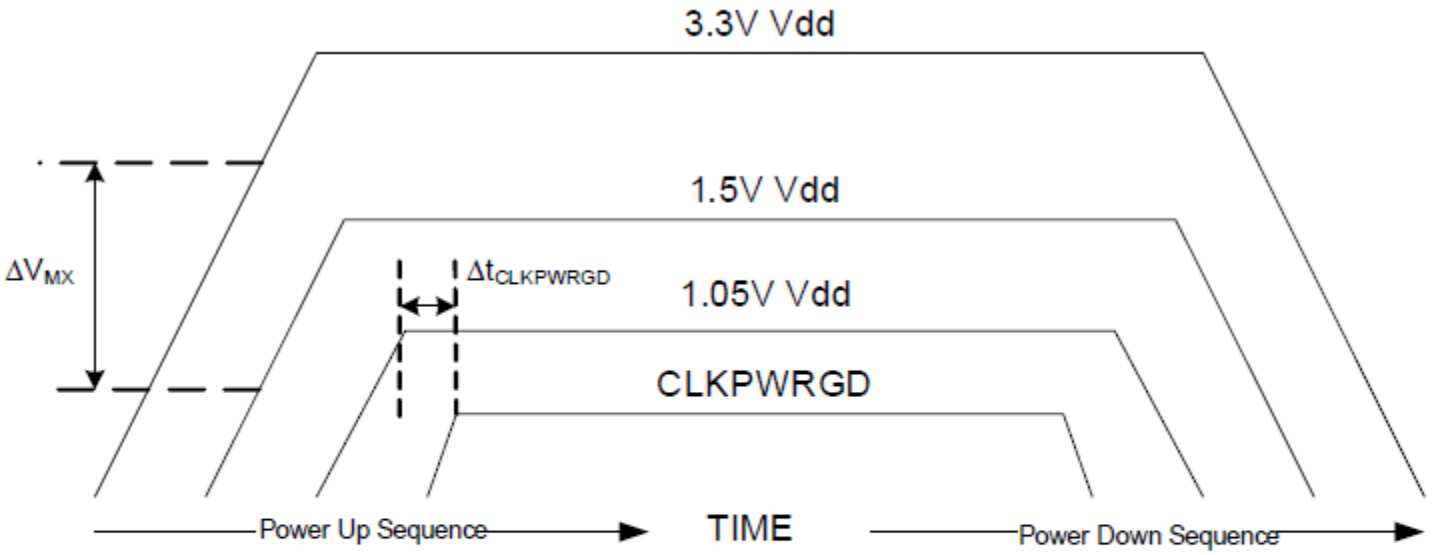
Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	99.75	9.91406	9.99906	10.02406	10.02506	10.02607	10.05107	10.13607	ns	1,2
	133.00	7.41430	7.49930	7.51805	7.51880	7.51955	7.53830	7.62330	ns	1,2
	166.25	5.91444	5.99944	6.01444	6.01504	6.01564	6.03064	6.11564	ns	1,2
	199.50	4.91453	4.99953	5.01203	5.01253	5.01303	5.02553	5.11053	ns	1,2
	266.00	3.66465	3.74965	3.75902	3.75940	3.75977	3.76915	3.85415	ns	1,2
	332.50	2.91472	2.99972	3.00722	3.00752	3.00782	3.01532	3.10032	ns	1,2
	399.00	2.41477	2.49977	2.50602	2.50627	2.50652	2.51277	2.59777	ns	1,2
SRC	99.75	9.91406	9.99906	10.02406	10.02506	10.02607	10.05107	10.13607	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 14.31818MHz.

Power-up Sequencing Requirements



Notes:

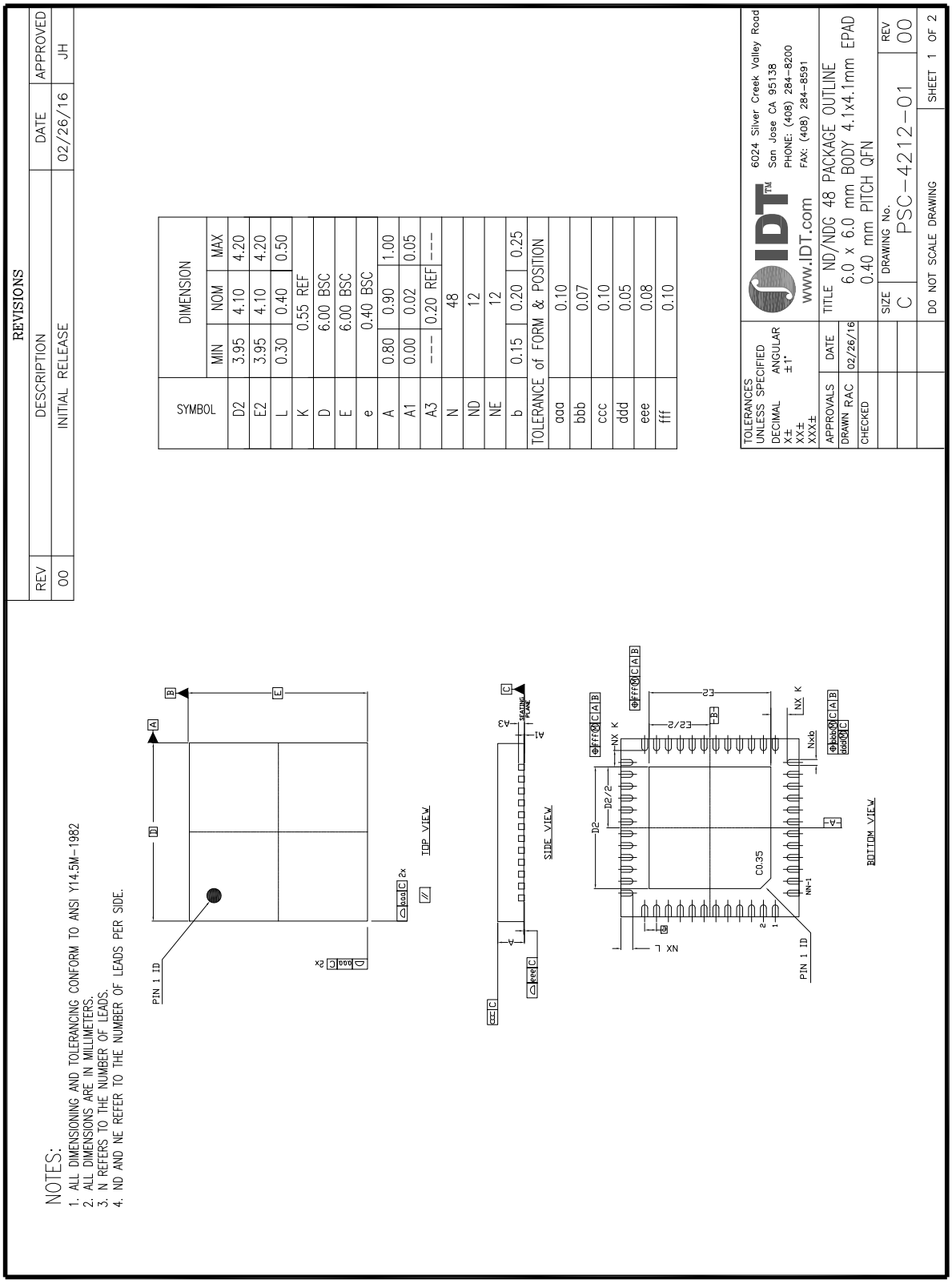
1. The maximum difference (ΔV_{MX}) between any two voltages is 0.7V if the lower power supply is powered up first.
2. There are no timing requirements between the higher and lower voltages if the higher voltages power up first.
3. The minimum time before CLKPWRGD can be set ($\Delta t_{CLKPWRGD} = 0$) is 0 sec from the last power supply that is powered up.

Marking Diagram

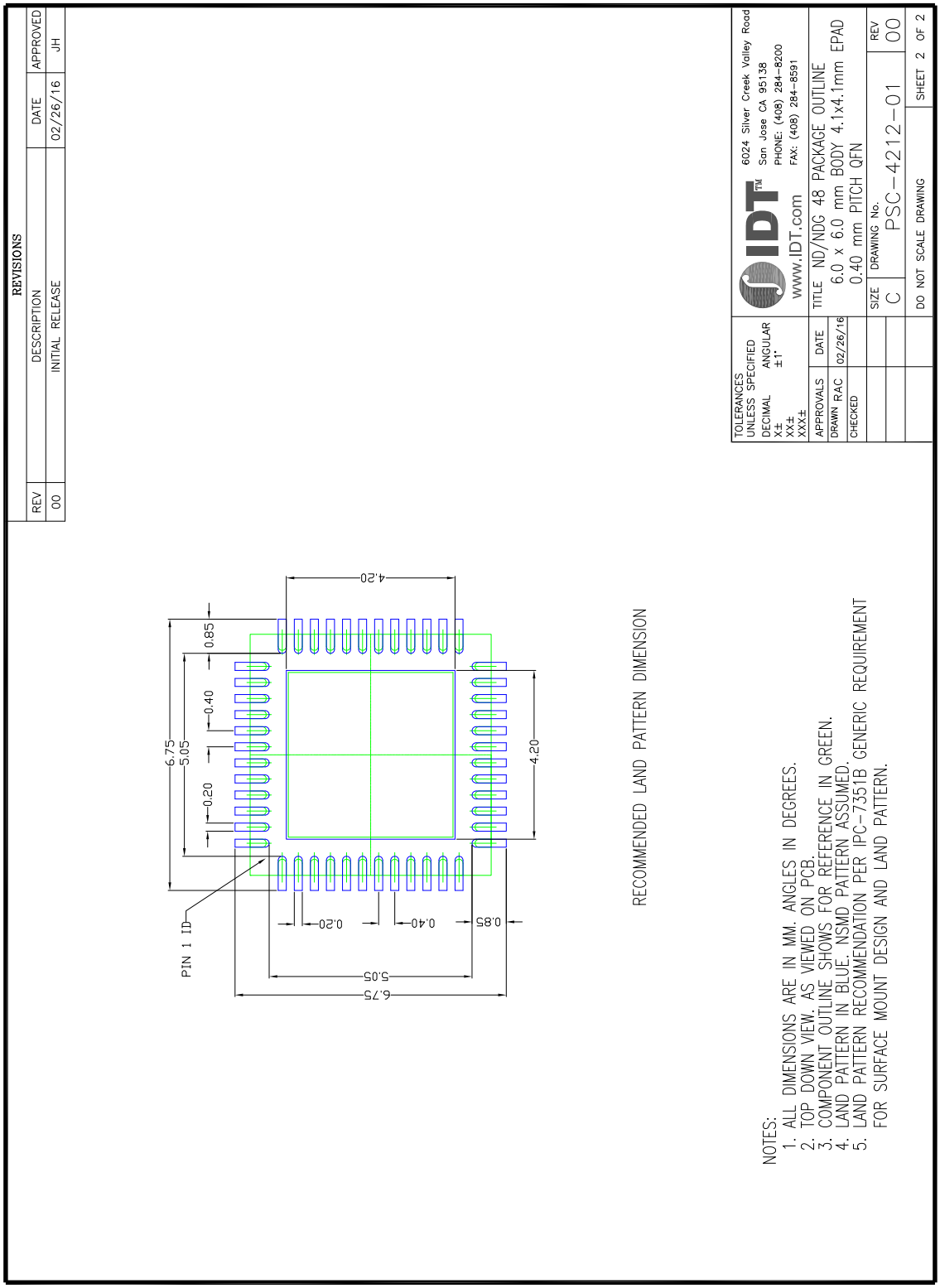
Notes:

1. Line 1: company name
2. Line 2: truncated part number.
3. “L” denotes RoHS compliant package.
4. Line 3: YYWW is the last two digits of the year and week that the part was assembled.
5. Line 4: Country of origin.
6. Line 5: LOT is the lot number.

Package Outline and Dimensions (NDG48)



Package Outline and Dimensions (NDG48), cont.



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9VRS4338DKLF	Trays	48-pin MLF	0 to +85° C
9VRS4338DKLFT	Tape and Reel	48-pin MLF	0 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"D" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Intiator	Description	Page #
A	2/26/2016	RDW	Updated POD drawings with current NDG48 spec.	Various

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

Tech Support
www.idt.com/go/support

Corporate Headquarters
Integrated Device Technology, Inc.
www.idt.com