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FMB MB9B400A Series

32-bit ARM® Cortex®-M3 based Microcontroller
MB9BF404NA/RA, MB9BF405NA/RA, MB9BF406NA/RA

Data Sheet (Full Production)



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Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or VIO range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification.

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FM3 MB9B400A Series

32-bit ARM® Cortex®-M3 based Microcontroller
MB9BF404NA/RA, MB9BF405NA/RA, MB9BF406NA/RA

Data Sheet (Full Production)



■ DESCRIPTION

The MB9B400A Series are a highly integrated 32-bit microcontroller that target for high-performance and cost-sensitive embedded control applications.

The MB9B400A Series are based on the ARM Cortex-M3 Processor and on-chip Flash memory and SRAM, and peripheral functions, including Motor Control Timers, ADCs and Communication Interfaces (CAN, UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE0 product categories in "FM3 Family PERIPHERAL MANUAL".

Note: ARM and Cortex are the trademarks of ARM Limited in the EU and other countries.



■ FEATURES

• 32-bit ARM Cortex-M3 Core

- Processor version: r2p0
- Up to 80MHz Frequency Operation
- Memory Protection Unit (MPU): improve the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

• On-chip Memories

[Flash memory]

- Up to 512 Kbyte
- Read cycle: 0wait-cycle@up to 60MHz, 2wait-cycle* above
 - *: Instruction pre-fetch buffer is included. So when CPU access continuously, it becomes 0wait-cycle
- Security function for code protection

[SRAM]

This series contain a total of up to 64Kbyte on-chip SRAM. This is composed of two independent SRAM(SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 32 Kbyte
- SRAM1: Up to 32 Kbyte

• CAN Interface (Max. 2channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

- **Multi-function Serial Interface (Max. 8channels)**

- 4 channels with 16steps × 9bit FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch.3)
- Operation mode is selectable from the followings for each channel.
 - UART
 - CSIO
 - LIN
 - I²C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13-16bit length)
- LIN break delimiter generate (can be changed 1-4bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I²C]

- Standard-mode (Max.100kbps) / Fast-mode (Max.400Kbps) supported

- **External Bus Interface**

- Supports SRAM, NOR& NAND Flash device
- Up to 8 chip selects
- 8/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size : Up to 256 Mbytes

- **DMA Controller (8channels)**

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32bit(4Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

- **A/D Converter (Max. 16channels)**

- [12-bit A/D Converter]

- Successive Approximation Register type
 - Built-in 3unit
 - Conversion time: 1.0 μ s@5V
 - Priority conversion available (priority at 2levels)
 - Scanning conversion mode
 - Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

- **Base Timer (Max. 8channels)**

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
 - 16-bit PPG timer
 - 16/32-bit reload timer
 - 16/32-bit PWC timer

- **Multi-function Timer (Max. 2units)**

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer \times 3ch/unit
 - Input capture \times 4ch/unit
 - Output compare \times 6ch/unit
 - A/D activation compare \times 3ch/unit
 - Waveform generator \times 3ch/unit
 - 16-bit PPG timer \times 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
 - DC chopper waveform output function
 - Dead time function
 - Input capture function
 - A/D convertor activate function
 - DTIF (Motor emergency stop) interrupt function

- **Quadrature Position/Revolution Counter (QPRC) (Max. 2units)**

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
 - 16-bit position counter
 - 16-bit revolution counter
 - Two 16-bit compare registers

- **Dual Timer (Two 32/16bit Down Counter)**

The Dual Timer consists of two programmable 32/16-bit down counters. Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

- **Watch Counter**

The Watch counter is used for wake up from sleep mode.

- Interval timer: up to 64s(Max.)@ Sub Clock : 32.768kHz

- **Watch dog Timer (2channels)**

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, "Hardware" watchdog is active in any low-power consumption modes except STOP mode.

- **External Interrupt Controller Unit**

- Up to 16 external vectors
- Include one non-maskable interrupt(NMI)

- **General Purpose I/O Port**

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O Ports@120pin Package

- **CRC (Cyclic Redundancy Check) Accelerator**

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

- **Clock and Reset**

- [Clocks]

- Five clock sources (2 ext. osc, 2 CR osc, and Main PLL) that are dynamically selectable.

- Main Clock : 4MHz to 48MHz
 - Sub Clock : 32.768kHz
 - Built-in high-speed CR Clock : 4MHz
 - Built-in low-speed CR Clock : 100kHz
 - Main PLL Clock

- [Resets]

- Reset requests from INITX pins
 - Power-on reset
 - Software reset
 - Watchdog timers reset
 - Low-voltage detector reset
 - Clock supervisor reset

- **Clock Super Visor (CSV)**

- Clocks generated by CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
 - External OSC frequency anomaly is detected, interrupt or reset is asserted.

- **Low Voltage Detector (LVD)**

- This series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage has been set, Low Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
 - LVD2: auto-reset operation

- **Low-Power Consumption Mode**

- Three low-power consumption modes supported.

- SLEEP
 - TIMER
 - STOP

- **Debug**

- Serial Wire JTAG Debug Port (SWJ-DP)
 - Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

- **Power Supply**

- VCC = 2.7V to 5.5V: Correspond to the wide range voltage.

■ PRODUCT LINEUP

• Memory size

Product device	MB9BF404NA/RA	MB9BF405NA/RA	MB9BF406NA/RA
On-chip Flash memory	256Kbyte	384Kbyte	512Kbyte
On-chip SRAM	32Kbyte	48Kbyte	64Kbyte

• Function

Product device		MB9BF404NA MB9BF405NA MB9BF406NA	MB9BF404RA MB9BF405RA MB9BF406RA
Pin count		100	120
CPU		Cortex-M3	
Freq.		80MHz	
Power supply voltage range		2.7V to 5.5V	
CAN Interface		2ch(Max)	
DMAC		8ch	
External Bus Interface		Addr:25bit (Max.) Data:8/16 bit CS:5(Max.) Support: SRAM, NOR Flash	Addr:25bit (Max.) Data:8/16 bit CS:8(Max.) Support: SRAM, NOR & NAND Flash
Multi-function Serial Interface (UART/CSIO/LIN/I ² C)		8ch (Max.)	
Base Timer (PWC/ Reload timer/PWM/PPG)		8ch (Max.)	
MF- Timer	A/D activation compare	3ch.	2 units (Max.)
	Input capture	4ch.	
	Free-run timer	3ch.	
	Output compare	6ch.	
	Waveform generator	3ch.	
	PPG	3ch.	
QPRC		2ch (Max.)	
Dual Timer		1 unit	
Watch Counter		1 unit	
CRC Accelerator		Yes	
Watchdog timer		1ch(SW) + 1ch(HW)	
External Interrupts		16pins (Max.)+ NMI × 1	
I/O ports		80pins (Max.)	100pins (Max.)
12 bit A/D converter		16ch (3 units)	
CSV (Clock Super Visor)		Yes	
LVD (Low Voltage Detector)		2ch	
Built-in CR	High-speed	4MHz	
	Low-speed	100kHz	
Debug Function		SWJ-DP/ETM	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See "■ ELECTRICAL CHARACTERISTICS 4.AC Characteristics (3)Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

■ PACKAGES

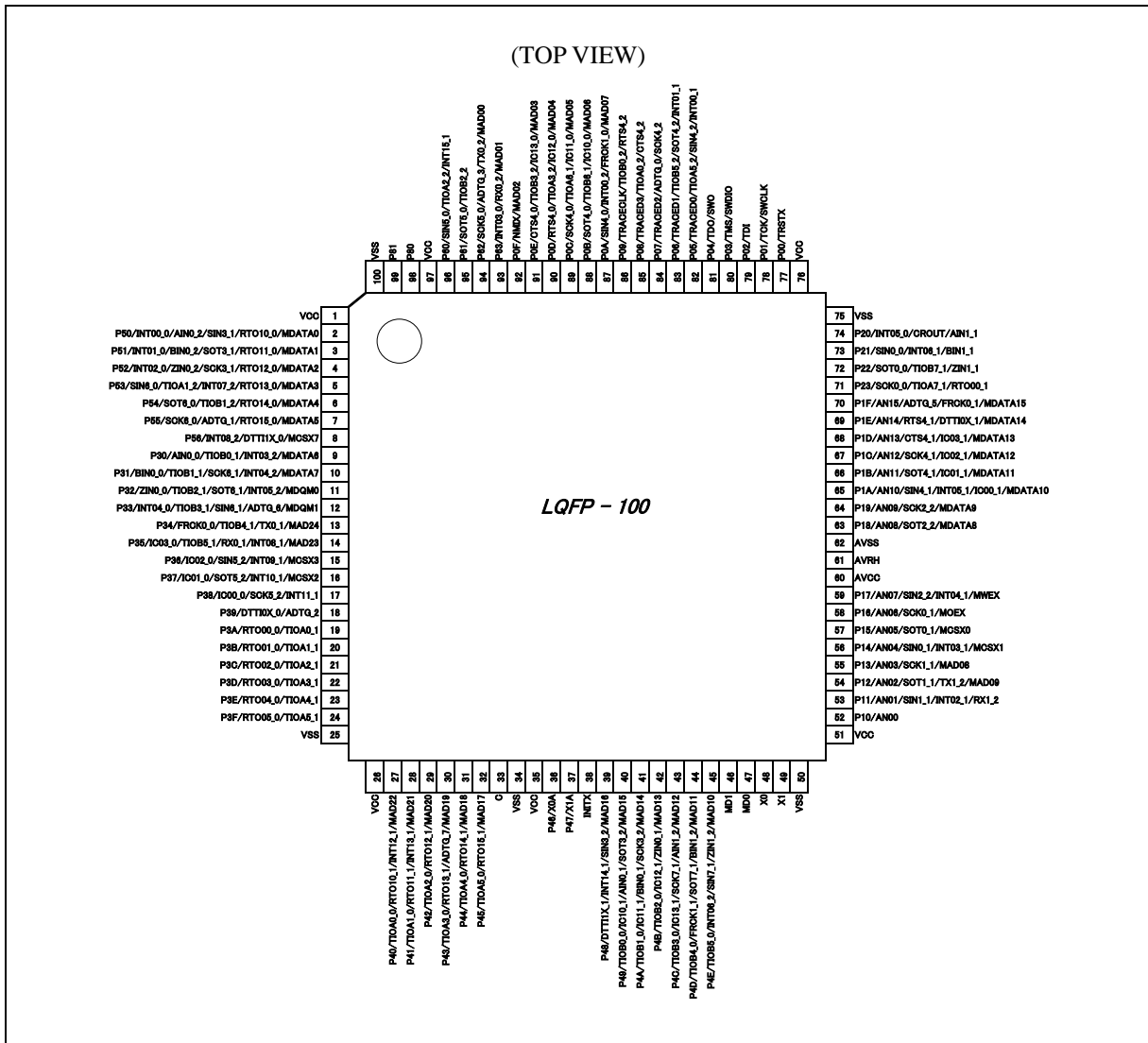
Package \ Product name	MB9BF404NA MB9BF405NA MB9BF406NA	MB9BF404RA MB9BF405RA MB9BF406RA
LQFP: FPT-100P-M23 (0.5mm pitch)	○	-
LQFP: FPT-120P-M37 (0.5mm pitch)	-	○
BGA: BGA-112P-M04 (0.8mm pitch)	○	-

○ : Supported

Note : Refer to "■PACKAGE DIMENSIONS" for detailed information on each package.

PIN ASSIGNMENT

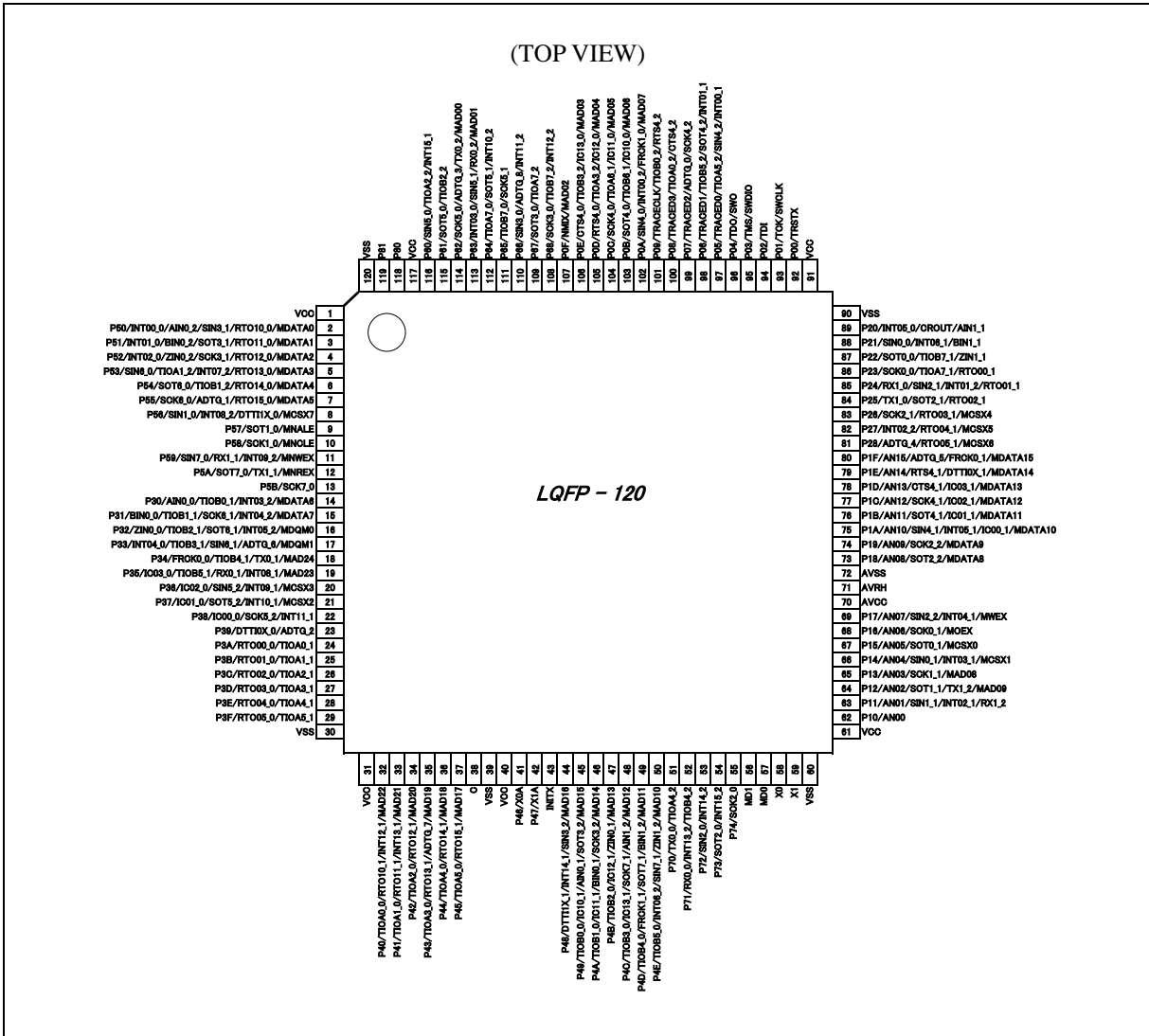
FPT-100P-M23



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

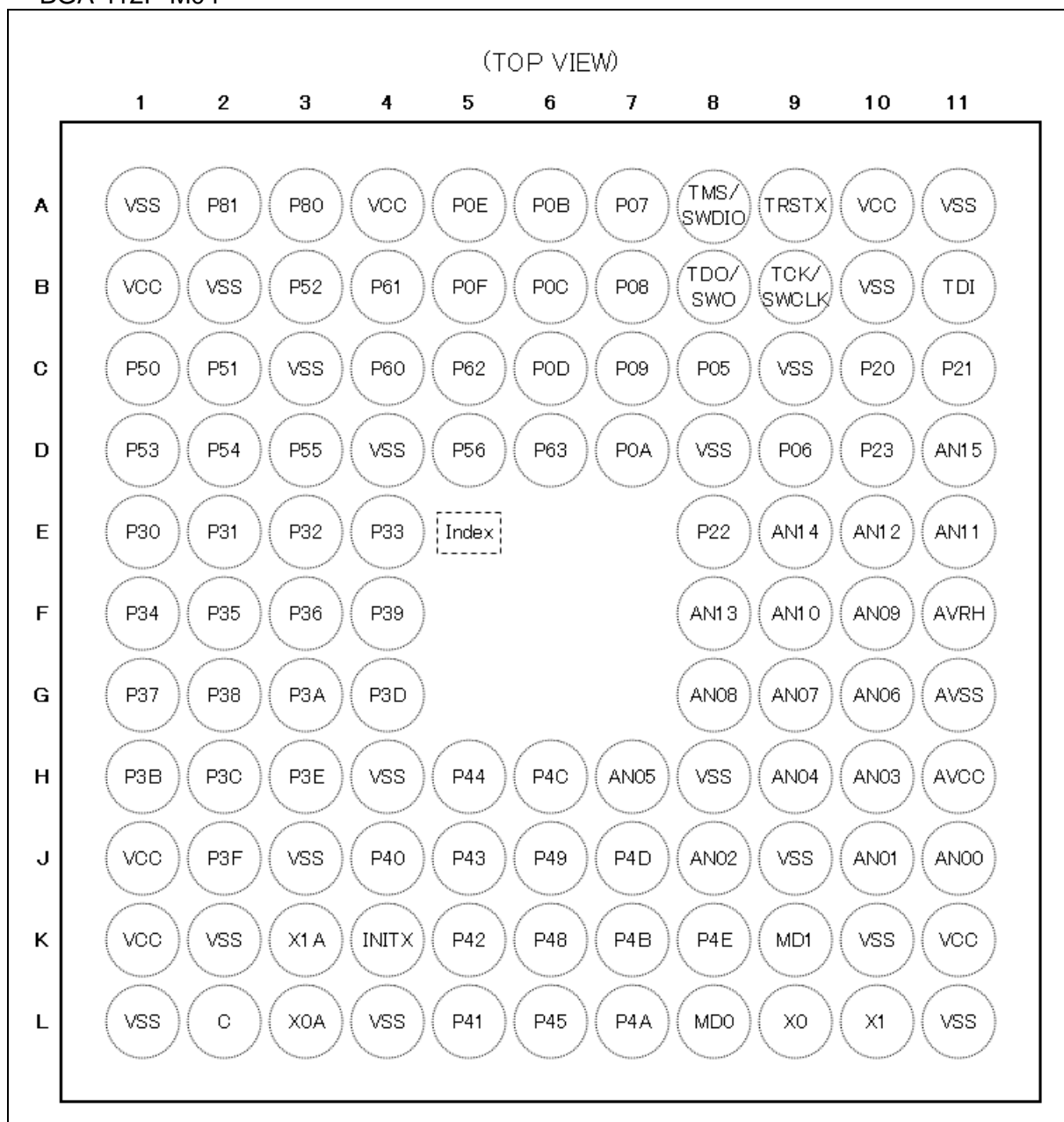
• FPT-120P-M21



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

• BGA-112P-M04



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ LIST OF PIN FUNCTIONS

- List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
1	B1	1	VCC	-	
2	C1	2	P50	E	H
			INT00_0		
			AIN0_2		
			SIN3_1		
			RTO10_0 (PPG10_0)		
			MDATA0		
3	C2	3	P51	E	H
			INT01_0		
			BIN0_2		
			SOT3_1 (SDA3_1)		
			RTO11_0 (PPG10_0)		
			MDATA1		
4	B3	4	P52	E	H
			INT02_0		
			ZIN0_2		
			SCK3_1 (SCL3_1)		
			RTO12_0 (PPG12_0)		
			MDATA2		
5	D1	5	P53	E	H
			SIN6_0		
			TIOA1_2		
			INT07_2		
			RTO13_0 (PPG12_0)		
			MDATA3		
6	D2	6	P54	E	I
			SOT6_0 (SDA6_0)		
			TIOB1_2		
			RTO14_0 (PPG14_0)		
			MDATA4		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
7	D3	7	P55	E	I
			SCK6_0 (SCL6_0)		
			ADTG_1		
			RTO15_0 (PPG14_0)		
			MDATA5		
8	D5	8	P56	E	H
			SIN1_0 (120pin only)		
			INT08_2		
			DTTI1X_0		
-	-	9	P57	E	I
			SOT1_0 (SDA1_0)		
			MNALE		
-	-	10	P58	E	I
			SCK1_0 (SCL1_0)		
			MNCLE		
-	-	11	P59	E	H
			SIN7_0		
			RX1_1		
			INT09_2		
			MNWEX		
-	-	12	P5A	E	I
			SOT7_0 (SDA7_0)		
			TX1_1		
			MNREX		
-	-	13	P5B	E	I
			SCK7_0 (SCL7_0)		
9	E1	14	P30	E	H
			AIN0_0		
			TIOB0_1		
			INT03_2		
			MDATA6		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
10	E2	15	P31	E	H
			BIN0_0		
			TIOB1_1		
			SCK6_1 (SCL6_1)		
			INT04_2		
			MDATA7		
11	E3	16	P32	E	H
			ZIN0_0		
			TIOB2_1		
			SOT6_1 (SDA6_1)		
			INT05_2		
			MDQM0		
12	E4	17	P33	E	H
			INT04_0		
			TIOB3_1		
			SIN6_1		
			ADTG_6		
			MDQM1		
13	F1	18	P34	E	I
			FRCK0_0		
			TIOB4_1		
			TX0_1		
			MAD24		
14	F2	19	P35	E	H
			IC03_0		
			TIOB5_1		
			RX0_1		
			INT08_1		
			MAD23		
15	F3	20	P36	E	H
			IC02_0		
			SIN5_2		
			INT09_1		
			MCSX3		
16	G1	21	P37	E	H
			IC01_0		
			SOT5_2 (SDA5_2)		
			INT10_1		
			MCSX2		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
17	G2	22	P38	E	H
			IC00_0		
			SCK5_2 (SCL5_2)		
			INT11_1		
18	F4	23	P39	E	I
			DTTIOX_0		
			ADTG_2		
19	G3	24	P3A	G	I
			RTO00_0 (PPG00_0)		
			TIOA0_1		
-	B2	-	VSS	-	-
20	H1	25	P3B	G	I
			RTO01_0 (PPG00_0)		
			TIOA1_1		
21	H2	26	P3C	G	I
			RTO02_0 (PPG02_0)		
			TIOA2_1		
22	G4	27	P3D	G	I
			RTO03_0 (PPG02_0)		
			TIOA3_1		
23	H3	28	P3E	G	I
			RTO04_0 (PPG04_0)		
			TIOA4_1		
24	J2	29	P3F	G	I
			RTO05_0 (PPG04_0)		
			TIOA5_1		
25	L1	30	VSS	-	-
26	J1	31	VCC	-	-
27	J4	32	P40	G	H
			TIOA0_0		
			RTO10_1 (PPG10_1)		
			INT12_1		
			MAD22		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
28	L5	33	P41	G	H
			TIOA1_0		
			RTO11_1 (PPG10_1)		
			INT13_1		
			MAD21		
29	K5	34	P42	G	I
			TIOA2_0		
			RTO12_1 (PPG12_1)		
			MAD20		
30	J5	35	P43	G	I
			TIOA3_0		
			RTO13_1 (PPG12_1)		
			ADTG_7		
			MAD19		
-	K2	-	VSS	-	-
-	J3	-	VSS	-	-
-	H4	-	VSS	-	-
31	H5	36	P44	G	I
			TIOA4_0		
			RTO14_1 (PPG14_1)		
			MAD18		
32	L6	37	P45	G	I
			TIOA5_0		
			RTO15_1 (PPG14_1)		
			MAD17		
33	L2	38	C	-	-
34	L4	39	VSS	-	-
35	K1	40	VCC	-	-
36	L3	41	P46	D	M
			X0A		
37	K3	42	P47	D	N
			X1A		
38	K4	43	INITX	B	C
39	K6	44	P48	E	H
			DTTI1X_1		
			INT14_1		
			SIN3_2		
			MAD16		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
40	J6	45	P49	E	I
			TIOB0_0		
			IC10_1		
			AIN0_1		
			SOT3_2 (SDA3_2)		
			MAD15		
41	L7	46	P4A	E	I
			TIOB1_0		
			IC11_1		
			BIN0_1		
			SCK3_2 (SCL3_2)		
			MAD14		
42	K7	47	P4B	E	I
			TIOB2_0		
			IC12_1		
			ZIN0_1		
			MAD13		
43	H6	48	P4C	E	I
			TIOB3_0		
			IC13_1		
			SCK7_1 (SCL7_1)		
			AIN1_2		
			MAD12		
44	J7	49	P4D	E	I
			TIOB4_0		
			FRCK1_1		
			SOT7_1 (SDA7_1)		
			BIN1_2		
			MAD11		
45	K8	50	P4E	E	H
			TIOB5_0		
			INT06_2		
			SIN7_1		
			ZIN1_2		
			MAD10		
-	-	51	P70	E	I
			TX0_0		
			TIOA4_2		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
-	-	52	P71	E	H
			RX0_0		
			INT13_2		
			TIOB4_2		
-	-	53	P72	E	H
			SIN2_0		
			INT14_2		
-	-	54	P73	E	H
			SOT2_0 (SDA2_0)		
			INT15_2		
-	-	55	P74	E	I
			SCK2_0 (SCL2_0)		
46	K9	56	MD1	C	D
47	L8	57	MD0	C	D
48	L9	58	X0	A	A
49	L10	59	X1	A	B
50	L11	60	VSS	-	
51	K11	61	VCC	-	
52	J11	62	P10	F	K
			AN00		
53	J10	63	P11	F	L
			AN01		
			SIN1_1		
			INT02_1		
			RX1_2		
-	K10	-	VSS	-	
-	J9	-	VSS	-	
54	J8	64	P12	F	K
			AN02		
			SOT1_1 (SDA1_1)		
			TX1_2		
			MAD09		
55	H10	65	P13	F	K
			AN03		
			SCK1_1 (SCL1_1)		
			MAD08		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
56	H9	66	P14	F	L
			AN04		
			SIN0_1		
			INT03_1		
			MCSX1		
57	H7	67	P15	F	K
			AN05		
			SOT0_1 (SDA0_1)		
			MCSX0		
58	G10	68	P16	F	K
			AN06		
			SCK0_1 (SCL0_1)		
			MOEX		
59	G9	69	P17	F	L
			AN07		
			SIN2_2		
			INT04_1		
			MWEX		
60	H11	70	AVCC	-	
61	F11	71	AVRH	-	
62	G11	72	AVSS	-	
63	G8	73	P18	F	K
			AN08		
			SOT2_2 (SDA2_2)		
			MDATA8		
64	F10	74	P19	F	K
			AN09		
			SCK2_2 (SCL2_2)		
			MDATA9		
65	F9	75	P1A	F	L
			AN10		
			SIN4_1		
			INT05_1		
			IC00_1		
			MDATA10		
-	H8	-	VSS	-	

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
66	E11	76	P1B	F	K
			AN11		
			SOT4_1 (SDA4_1)		
			IC01_1		
			MDATA11		
67	E10	77	P1C	F	K
			AN12		
			SCK4_1 (SCL4_1)		
			IC02_1		
			MDATA12		
68	F8	78	P1D	F	K
			AN13		
			CTS4_1		
			IC03_1		
			MDATA13		
69	E9	79	P1E	F	K
			AN14		
			RTS4_1		
			DTTIOX_1		
			MDATA14		
70	D11	80	P1F	F	K
			AN15		
			ADTG_5		
			FRCK0_1		
			MDATA15		
-	-	81	P28	E	I
			ADTG_4		
			RTO05_1 (PPG04_1)		
			MCSX6		
-	-	82	P27	E	H
			INT02_2		
			RTO04_1 (PPG04_1)		
			MCSX5		
-	-	83	P26	E	I
			SCK2_1 (SCL2_1)		
			RTO03_1 (PPG02_1)		
			MCSX4		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
-	-	84	P25	E	I
			TX1_0		
			SOT2_1 (SDA2_1)		
			RTO02_1 (PPG02_1)		
-	B10	-	VSS	-	-
-	C9	-	VSS	-	-
-	-	85	P24	E	H
			RX1_0		
			SIN2_1		
			INT01_2		
			RTO01_1 (PPG00_1)		
71	D10	86	P23	E	I
			SCK0_0 (SCL0_0)		
			TIOA7_1		
			RTO00_1 (PPG00_1)		
72	E8	87	P22	E	I
			SOT0_0 (SDA0_0)		
			TIOB7_1		
			ZIN1_1		
73	C11	88	P21	E	H
			SIN0_0		
			INT06_1		
			BIN1_1		
74	C10	89	P20	E	H
			INT05_0		
			CROUT		
			AIN1_1		
75	A11	90	VSS	-	-
76	A10	91	VCC	-	-
77	A9	92	P00	E	E
			TRSTX		
78	B9	93	P01	E	E
			TCK		
			SWCLK		
79	B11	94	P02	E	E
			TDI		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
80	A8	95	P03	E	E
			TMS		
			SWDIO		
81	B8	96	P04	E	E
			TDO		
			SWO		
82	C8	97	P05	E	F
			TRACED0		
			TIOA5_2		
			SIN4_2		
-	D8	-	VSS	-	-
83	D9	98	P06	E	F
			TRACED1		
			TIOB5_2		
			SOT4_2 (SDA4_2)		
			INT01_1		
84	A7	99	P07	E	G
			TRACED2		
			ADTG_0		
			SCK4_2 (SCL4_2)		
85	B7	100	P08	E	G
			TRACED3		
			TIOA0_2		
			CTS4_2		
86	C7	101	P09	E	G
			TRACECLK		
			TIOB0_2		
			RTS4_2		
87	D7	102	P0A	E	H
			SIN4_0		
			INT00_2		
			FRCK1_0		
			MAD07		
88	A6	103	P0B	E	I
			SOT4_0 (SDA4_0)		
			TIOB6_1		
			IC10_0		
			MAD06		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
89	B6	104	P0C	E	I
			SCK4_0 (SCL4_0)		
			TIOA6_1		
			IC11_0		
			MAD05		
90	C6	105	P0D	E	I
			RTS4_0		
			TIOA3_2		
			IC12_0		
			MAD04		
91	A5	106	P0E	E	I
			CTS4_0		
			TIOB3_2		
			IC13_0		
			MAD03		
-	D4	-	VSS	-	-
-	C3	-	VSS	-	-
92	B5	107	P0F	E	J
			NMIX		
			MAD02		
-	-	108	P68	E	H
			SCK3_0 (SCL3_0)		
			TIOB7_2		
			INT12_2		
-	-	109	P67	E	I
			SOT3_0 (SDA3_0)		
			TIOA7_2		
-	-	110	P66	E	H
			SIN3_0		
			ADTG_8		
			INT11_2		
-	-	111	P65	E	I
			TIOB7_0		
			SCK5_1 (SCL5_1)		
-	-	112	P64	E	H
			TIOA7_0		
			SOT5_1 (SDA5_1)		
			INT10_2		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
93	D6	113	P63	E	H
			INT03_0		
			RX0_2		
			MAD01		
-	-		SIN5_1		
94	C5	114	P62	E	I
			SCK5_0 (SCL5_0)		
			ADTG_3		
			TX0_2		
			MAD00		
95	B4	115	P61	E	I
			SOT5_0 (SDA5_0)		
			TIOB2_2		
96	C4	116	P60	E	H
			SIN5_0		
			TIOA2_2		
			INT15_1		
97	A4	117	VCC	-	
98	A3	118	P80	H	O
99	A2	119	P81	H	O
100	A1	120	VSS	-	

• List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
ADC	ADTG_0	A/D converter external trigger input pin.	84	A7	99
	ADTG_1		7	D3	7
	ADTG_2		18	F4	23
	ADTG_3		94	C5	114
	ADTG_4		-	-	81
	ADTG_5		70	D11	80
	ADTG_6		12	E4	17
	ADTG_7		30	J5	35
	ADTG_8		-	-	110
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	J11	62
	AN01		53	J10	63
	AN02		54	J8	64
	AN03		55	H10	65
	AN04		56	H9	66
	AN05		57	H7	67
	AN06		58	G10	68
	AN07		59	G9	69
	AN08		63	G8	73
	AN09		64	F10	74
	AN10		65	F9	75
AN11	66		E11	76	
AN12	67		E10	77	
AN13	68		F8	78	
AN14	69		E9	79	
AN15	70		D11	80	
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin.	27	J4	32
	TIOA0_1		19	G3	24
	TIOA0_2		85	B7	100
	TIOB0_0	Base timer ch.0 TIOB pin.	40	J6	45
	TIOB0_1		9	E1	14
	TIOB0_2		86	C7	101
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin.	28	L5	33
	TIOA1_1		20	H1	25
	TIOA1_2		5	D1	5
	TIOB1_0	Base timer ch.1 TIOB pin.	41	L7	46
	TIOB1_1		10	E2	15
	TIOB1_2		6	D2	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin.	29	K5	34
	TIOA2_1		21	H2	26
	TIOA2_2		96	C4	116
	TIOB2_0	Base timer ch.2 TIOB pin.	42	K7	47
	TIOB2_1		11	E3	16
	TIOB2_2		95	B4	115

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin.	30	J5	35
	TIOA3_1		22	G4	27
	TIOA3_2		90	C6	105
	TIOB3_0	Base timer ch.3 TIOB pin.	43	H6	48
	TIOB3_1		12	E4	17
	TIOB3_2		91	A5	106
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin.	31	H5	36
	TIOA4_1		23	H3	28
	TIOA4_2		-	-	51
	TIOB4_0	Base timer ch.4 TIOB pin.	44	J7	49
	TIOB4_1		13	F1	18
	TIOB4_2		-	-	52
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin.	32	L6	37
	TIOA5_1		24	J2	29
	TIOA5_2		82	C8	97
	TIOB5_0	Base timer ch.5 TIOB pin.	45	K8	50
	TIOB5_1		14	F2	19
	TIOB5_2		83	D9	98
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin.	89	B6	104
	TIOB6_1	Base timer ch.6 TIOB pin.	88	A6	103
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin.	-	-	112
	TIOA7_1		71	D10	86
	TIOA7_2		-	-	109
	TIOB7_0	Base timer ch.7 TIOB pin.	-	-	111
	TIOB7_1		72	E8	87
	TIOB7_2		-	-	108
CAN 0	TX0_0	CAN interface ch.0 TX output.	-	-	51
	TX0_1		13	F1	18
	TX0_2		94	C5	114
	RX0_0	CAN interface ch.0 RX input.	-	-	52
	RX0_1		14	F2	19
	RX0_2		93	D6	113
CAN 1	TX1_0	CAN interface ch.1 TX output.	-	-	84
	TX1_1		-	-	12
	TX1_2		54	J8	64
	RX1_0	CAN interface ch.1 RX input.	-	-	85
	RX1_1		-	-	11
	RX1_2		53	J10	63

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Debugger	SWCLK	Serial wire debug interface clock input.	78	B9	93
	SWDIO	Serial wire debug interface data input / output.	80	A8	95
	SWO	Serial wire viewer output.	81	B8	96
	TCK	J-TAG test clock input.	78	B9	93
	TDI	J-TAG test data input.	79	B11	94
	TDO	J-TAG debug data output.	81	B8	96
	TMS	J-TAG test mode state input/output.	80	A8	95
	TRACECLK	Trace CLK output of ETM.	86	C7	101
	TRACED0	Trace data output of ETM.	82	C8	97
	TRACED1		83	D9	98
	TRACED2		84	A7	99
	TRACED3		85	B7	100
	TRSTX	J-TAG test reset Input.	77	A9	92
External Bus	MAD00	External bus interface address bus.	94	C5	114
	MAD01		93	D6	113
	MAD02		92	B5	107
	MAD03		91	A5	106
	MAD04		90	C6	105
	MAD05		89	B6	104
	MAD06		88	A6	103
	MAD07		87	D7	102
	MAD08		55	H10	65
	MAD09		54	J8	64
	MAD10		45	K8	50
	MAD11		44	J7	49
	MAD12		43	H6	48
	MAD13		42	K7	47
	MAD14		41	L7	46
	MAD15		40	J6	45
	MAD16		39	K6	44
	MAD17		32	L6	37
	MAD18		31	H5	36
	MAD19		30	J5	35
	MAD20		29	K5	34
	MAD21		28	L5	33
	MAD22		27	J4	32
	MAD23		14	F2	19
	MAD24	13	F1	18	
	MCSX0	External bus interface chip select output pin.	57	H7	67
	MCSX1		56	H9	66
	MCSX2		16	G1	21
	MCSX3		15	F3	20
	MCSX4		-	-	83
	MCSX5		-	-	82
	MCSX6		-	-	81
	MCSX7		8	D5	8

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
External Bus	MDATA0	External bus interface data bus.	2	C1	2
	MDATA1		3	C2	3
	MDATA2		4	B3	4
	MDATA3		5	D1	5
	MDATA4		6	D2	6
	MDATA5		7	D3	7
	MDATA6		9	E1	14
	MDATA7		10	E2	15
	MDATA8		63	G8	73
	MDATA9		64	F10	74
	MDATA10		65	F9	75
	MDATA11		66	E11	76
	MDATA12		67	E10	77
	MDATA13		68	F8	78
	MDATA14		69	E9	79
	MDATA15	70	D11	80	
	MDQM0	External bus interface byte mask signal output.	11	E3	16
	MDQM1		12	E4	17
	MNALE	External bus interface ALE signal to control NAND Flash output pin.	-	-	9
	MNCLE	External bus interface CLE signal to control NAND Flash output pin.	-	-	10
MNREX	External bus interface read enable signal to control NAND Flash.	-	-	12	
MNWEX	External bus interface write enable signal to control NAND Flash.	-	-	11	
MOEX	External bus interface read enable signal for SRAM.	58	G10	68	
MWEX	External bus interface write enable signal for SRAM.	59	G9	69	

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
External Interrupt	INT00_0	External interrupt request 00 input pin.	2	C1	2
	INT00_1		82	C8	97
	INT00_2		87	D7	102
	INT01_0	External interrupt request 01 input pin.	3	C2	3
	INT01_1		83	D9	98
	INT01_2		-	-	85
	INT02_0	External interrupt request 02 input pin.	4	B3	4
	INT02_1		53	J10	63
	INT02_2		-	-	82
	INT03_0	External interrupt request 03 input pin.	93	D6	113
	INT03_1		56	H9	66
	INT03_2		9	E1	14
	INT04_0	External interrupt request 04 input pin.	12	E4	17
	INT04_1		59	G9	69
	INT04_2		10	E2	15
	INT05_0	External interrupt request 05 input pin.	74	C10	89
	INT05_1		65	F9	75
	INT05_2		11	E3	16
	INT06_1	External interrupt request 06 input pin.	73	C11	88
	INT06_2		45	K8	50
	INT07_2	External interrupt request 07 input pin.	5	D1	5
	INT08_1	External interrupt request 08 input pin.	14	F2	19
	INT08_2		8	D5	8
	INT09_1	External interrupt request 09 input pin.	15	F3	20
	INT09_2		-	-	11
	INT10_1	External interrupt request 10 input pin.	16	G1	21
	INT10_2		-	-	112
	INT11_1	External interrupt request 11 input pin.	17	G2	22
	INT11_2		-	-	110
	INT12_1	External interrupt request 12 input pin.	27	J4	32
INT12_2	-		-	108	
INT13_1	External interrupt request 13 input pin.	28	L5	33	
INT13_2		-	-	52	
INT14_1	External interrupt request 14 input pin.	39	K6	44	
INT14_2		-	-	53	
INT15_1	External interrupt request 15 input pin.	96	C4	116	
INT15_2		-	-	54	
NMIX	Non-Maskable Interrupt input.	92	B5	107	

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
GPIO	P00	General-purpose I/O port 0.	77	A9	92
	P01		78	B9	93
	P02		79	B11	94
	P03		80	A8	95
	P04		81	B8	96
	P05		82	C8	97
	P06		83	D9	98
	P07		84	A7	99
	P08		85	B7	100
	P09		86	C7	101
	P0A		87	D7	102
	P0B		88	A6	103
	P0C		89	B6	104
	P0D		90	C6	105
	P0E		91	A5	106
	P0F		92	B5	107
	P10	General-purpose I/O port 1.	52	J11	62
	P11		53	J10	63
	P12		54	J8	64
	P13		55	H10	65
	P14		56	H9	66
	P15		57	H7	67
	P16		58	G10	68
	P17		59	G9	69
	P18		63	G8	73
	P19		64	F10	74
	P1A		65	F9	75
	P1B		66	E11	76
P1C	67	E10	77		
P1D	68	F8	78		
P1E	69	E9	79		
P1F	70	D11	80		
P20	General-purpose I/O port 2.	74	C10	89	
P21		73	C11	88	
P22		72	E8	87	
P23		71	D10	86	
P24		-	-	85	
P25		-	-	84	
P26		-	-	83	
P27		-	-	82	
P28		-	-	81	

Module	Pin name	Function	Pin No.			
			LQFP-100	BGA-112	LQFP-120	
GPIO	P30	General-purpose I/O port 3.	9	E1	14	
	P31		10	E2	15	
	P32		11	E3	16	
	P33		12	E4	17	
	P34		13	F1	18	
	P35		14	F2	19	
	P36		15	F3	20	
	P37		16	G1	21	
	P38		17	G2	22	
	P39		18	F4	23	
	P3A		19	G3	24	
	P3B		20	H1	25	
	P3C		21	H2	26	
	P3D		22	G4	27	
	P3E		23	H3	28	
	P3F		24	J2	29	
	P40		General-purpose I/O port 4.	27	J4	32
	P41			28	L5	33
	P42			29	K5	34
	P43			30	J5	35
	P44			31	H5	36
	P45			32	L6	37
	P46			36	L3	41
	P47			37	K3	42
	P48	39		K6	44	
	P49	40		J6	45	
	P4A	41		L7	46	
	P4B	42		K7	47	
	P4C	43		H6	48	
	P4D	44		J7	49	
	P4E	45		K8	50	
	P50	General-purpose I/O port 5.		2	C1	2
	P51		3	C2	3	
	P52		4	B3	4	
	P53		5	D1	5	
	P54		6	D2	6	
	P55		7	D3	7	
	P56		8	D5	8	
	P57		-	-	9	
	P58		-	-	10	
	P59		-	-	11	
	P5A		-	-	12	
	P5B		-	-	13	

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
GPIO	P60	General-purpose I/O port 6.	96	C4	116
	P61		95	B4	115
	P62		94	C5	114
	P63		93	D6	113
	P64		-	-	112
	P65		-	-	111
	P66		-	-	110
	P67		-	-	109
	P68	-	-	108	
	P70	General-purpose I/O port 7.	-	-	51
	P71		-	-	52
	P72		-	-	53
	P73		-	-	54
	P74	-	-	55	
	P80	General-purpose I/O port 8.	98	A3	118
	P81		99	A2	119
Multi Function Serial 0	SIN0_0	Multifunction serial interface ch.0 input pin.	73	C11	88
	SIN0_1		56	H9	66
	SOT0_0 (SDA0_0)	Multifunction serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I ² C (operation mode 4).	72	E8	87
	SOT0_1 (SDA0_1)		57	H7	67
	SCK0_0 (SCL0_0)	Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I ² C (operation mode 4).	71	D10	86
SCK0_1 (SCL0_1)	58		G10	68	
Multi Function Serial 1	SIN1_0	Multifunction serial interface ch.1 input pin.	-	-	8
	SIN1_1		53	J10	63
	SOT1_0 (SDA1_0)	Multifunction serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I ² C (operation mode 4).	-	-	9
	SOT1_1 (SDA1_1)		54	J8	64
	SCK1_0 (SCL1_0)	Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I ² C (operation mode 4).	-	-	10
SCK1_1 (SCL1_1)	55		H10	65	

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 2	SIN2_0	Multifunction serial interface ch.2 input pin.	-	-	53
	SIN2_1		-	-	85
	SIN2_2		59	G9	69
	SOT2_0 (SDA2_0)	Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I ² C (operation mode 4).	-	-	54
	SOT2_1 (SDA2_1)		-	-	84
	SOT2_2 (SDA2_2)		63	G8	73
	SCK2_0 (SCL2_0)	Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I ² C (operation mode 4).	-	-	55
	SCK2_1 (SCL2_1)		-	-	83
	SCK2_2 (SCL2_2)		64	F10	74
Multi Function Serial 3	SIN3_0	Multifunction serial interface ch.3 input pin.	-	-	110
	SIN3_1		2	C1	2
	SIN3_2		39	K6	44
	SOT3_0 (SDA3_0)	Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I ² C (operation mode 4).	-	-	109
	SOT3_1 (SDA3_1)		3	C2	3
	SOT3_2 (SDA3_2)		40	J6	45
	SCK3_0 (SCL3_0)	Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I ² C (operation mode 4).	-	-	108
	SCK3_1 (SCL3_1)		4	B3	4
	SCK3_2 (SCL3_2)		41	L7	46

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin.	87	D7	102
	SIN4_1		65	F9	75
	SIN4_2		82	C8	97
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I ² C (operation mode 4).	88	A6	103
	SOT4_1 (SDA4_1)		66	E11	76
	SOT4_2 (SDA4_2)		83	D9	98
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I ² C (operation mode 4).	89	B6	104
	SCK4_1 (SCL4_1)		67	E10	77
	SCK4_2 (SCL4_2)		84	A7	99
	RTS4_0	Multifunction serial interface ch.4 RTS output pin.	90	C6	105
	RTS4_1		69	E9	79
	RTS4_2		86	C7	101
	CTS4_0	Multifunction serial interface ch.4 CTS input pin.	91	A5	106
	CTS4_1		68	F8	78
	CTS4_2		85	B7	100
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin.	96	C4	116
	SIN5_1		-	-	113
	SIN5_2		15	F3	20
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I ² C (operation mode 4).	95	B4	115
	SOT5_1 (SDA5_1)		-	-	112
	SOT5_2 (SDA5_2)		16	G1	21
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I ² C (operation mode 4).	94	C5	114
	SCK5_1 (SCL5_1)		-	-	111
	SCK5_2 (SCL5_2)		17	G2	22

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin.	5	D1	5
	SIN6_1		12	E4	17
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I ² C (operation mode 4).	6	D2	6
	SOT6_1 (SDA6_1)		11	E3	16
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I ² C (operation mode 4).	7	D3	7
	SCK6_1 (SCL6_1)		10	E2	15
Multi Function Serial 7	SIN7_0	Multifunction serial interface ch.7 input pin.	-	-	11
	SIN7_1		45	K8	50
	SOT7_0 (SDA7_0)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I ² C (operation mode 4).	-	-	12
	SOT7_1 (SDA7_1)		44	J7	49
	SCK7_0 (SCL7_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I ² C (operation mode 4).	-	-	13
	SCK7_1 (SCL7_1)		43	H6	48

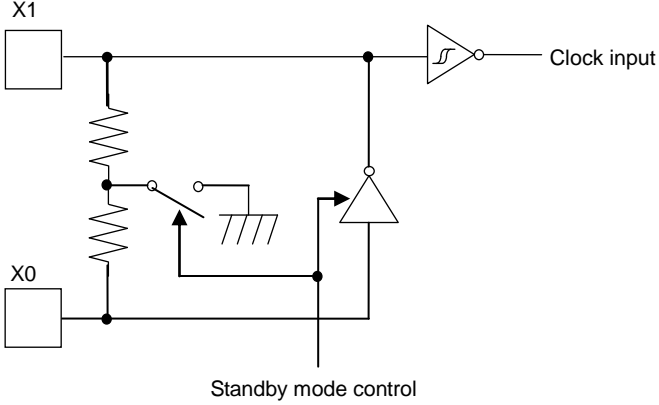
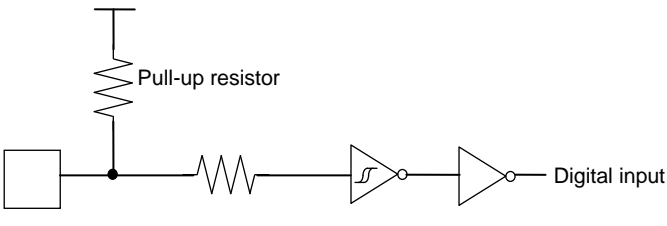
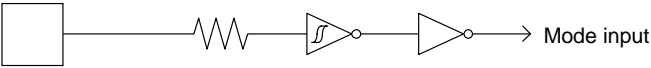
Module	Pin name	Function	Pin No.			
			LQFP-100	BGA-112	LQFP-120	
Multi Function Timer 0	DTTIOX_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	18	F4	23	
	DTTIOX_1		69	E9	79	
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	13	F1	18	
	FRCK0_1		70	D11	80	
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0. ICxx describes channel number.	17	G2	22	
	IC00_1		65	F9	75	
	IC01_0		16	G1	21	
	IC01_1		66	E11	76	
	IC02_0		15	F3	20	
	IC02_1		67	E10	77	
	IC03_0		14	F2	19	
	IC03_1		68	F8	78	
	RTO00_0 (PPG00_0)		Wave form generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output modes.	19	G3	24
	RTO00_1 (PPG00_1)			71	D10	86
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output modes.	20	H1	25	
	RTO01_1 (PPG00_1)		-	-	85	
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output modes.	21	H2	26	
	RTO02_1 (PPG02_1)		-	-	84	
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output modes.	22	G4	27	
	RTO03_1 (PPG02_1)		-	-	83	
RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output modes.	23	H3	28		
RTO04_1 (PPG04_1)		-	-	82		
RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output modes.	24	J2	29		
RTO05_1 (PPG04_1)		-	-	81		

Module	Pin name	Function	Pin No.			
			LQFP-100	BGA-112	LQFP-120	
Multi Function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of multi-function timer 1.	8	D5	8	
	DTTI1X_1		39	K6	44	
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin.	87	D7	102	
	FRCK1_1		44	J7	49	
	IC10_0	16-bit input capture ch.0 input pin of multi-function timer 1. ICxx describes channel number.	88	A6	103	
	IC10_1		40	J6	45	
	IC11_0		89	B6	104	
	IC11_1		41	L7	46	
	IC12_0		90	C6	105	
	IC12_1		42	K7	47	
	IC13_0		91	A5	106	
	IC13_1		43	H6	48	
	RTO10_0 (PPG10_0)		Wave form generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output modes.	2	C1	2
	RTO10_1 (PPG10_1)			27	J4	32
	RTO11_0 (PPG10_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG 1 output modes.	3	C2	3	
	RTO11_1 (PPG10_1)		28	L5	33	
	RTO12_0 (PPG12_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output modes.	4	B3	4	
	RTO12_1 (PPG12_1)		29	K5	34	
	RTO13_0 (PPG12_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG 1 output modes.	5	D1	5	
	RTO13_1 (PPG12_1)		30	J5	35	
RTO14_0 (PPG14_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output modes.	6	D2	6		
RTO14_1 (PPG14_1)		31	H5	36		
RTO15_0 (PPG14_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG 1 output modes.	7	D3	7		
RTO15_1 (PPG14_1)		32	L6	37		

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin.	9	E1	14
	AIN0_1		40	J6	45
	AIN0_2		2	C1	2
	BIN0_0	QPRC ch.0 BIN input pin.	10	E2	15
	BIN0_1		41	L7	46
	BIN0_2		3	C2	3
	ZIN0_0	QPRC ch.0 ZIN input pin.	11	E3	16
	ZIN0_1		42	K7	47
	ZIN0_2		4	B3	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin.	74	C10	89
	AIN1_2		43	H6	48
	BIN1_1	QPRC ch.1 BIN input pin.	73	C11	88
	BIN1_2		44	J7	49
	ZIN1_1	QPRC ch.1 ZIN input pin.	72	E8	87
	ZIN1_2		45	K8	50

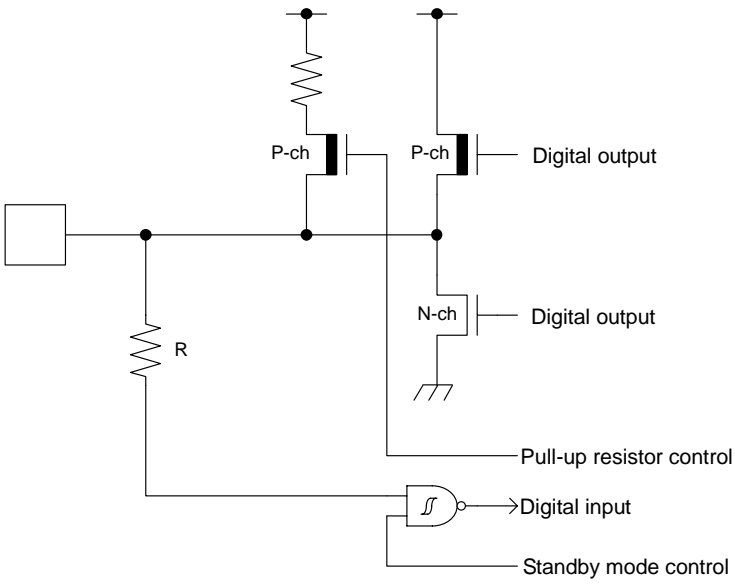
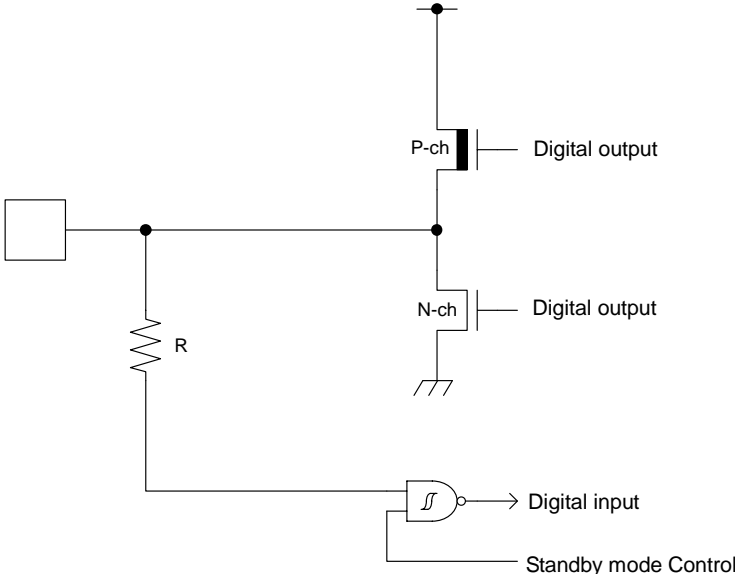
Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
RESET	INITX	External Reset Input. A reset is valid when INITX=L.	38	K4	43
Mode	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to flash memory, MD0=H must be input.	47	L8	57
	MD1	Mode 1 pin. Input must always be at the "L" level.	46	K9	56
POWER	VCC	Power Pin.	1	B1	1
	VCC		26	J1	31
	VCC		35	K1	40
	VCC		51	K11	61
	VCC		76	A10	91
	VCC		97	A4	117
GND	VSS	GND Pin.	-	B2	-
	VSS		25	L1	30
	VSS		-	K2	-
	VSS		-	J3	-
	VSS		-	H4	-
	VSS		34	L4	39
	VSS		50	L11	60
	VSS		-	K10	-
	VSS		-	J9	-
	VSS		-	H8	-
	VSS		-	B10	-
	VSS		-	C9	-
	VSS		75	A11	90
	VSS		-	D8	-
	VSS		-	D4	-
	VSS		-	C3	-
VSS	100	A1	120		
CLOCK	X0	Main clock (oscillation) input pin.	48	L9	58
	X0A	Sub clock (oscillation) input pin.	36	L3	41
	X1	Main clock (oscillation) I/O pin.	49	L10	59
	X1A	Sub clock (oscillation) I/O pin.	37	K3	42
	CROUT	Built-in High-speed CR-osc clock output port.	74	C10	89
Analog POWER	AVCC	A/D converter analog power pin.	60	H11	70
	AVRH	A/D converter analog reference voltage input pin.	61	F11	71
Analog GND	AVSS	A/D converter GND pin.	62	G11	72
C-pin	C	Power stabilization capacity pin.	33	L2	38

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 <p style="text-align: center;">Standby mode control</p>	<ul style="list-style-type: none"> • Oscillation feedback resistor : Approximately 1MΩ • With Standby mode control
B	 <p style="text-align: center;">Pull-up resistor</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input • pull-up resistor : Approximately 50kΩ
C		<ul style="list-style-type: none"> • CMOS level hysteresis input

Type	Circuit	Remarks
D	<p>The diagram shows two oscillator blocks, X1A and X0A, connected to a common bus. X1A is at the top and X0A is at the bottom. Each block contains a pull-up resistor, a feedback resistor, and a feedback capacitor. The bus is connected to various control signals: Digital output (P-ch and N-ch), Digital input, Standby mode control, and Pull-up resistor control. The bus is also connected to a resistor R and a feedback resistor.</p>	<ul style="list-style-type: none"> • It is possible to select the sub oscillation / GPIO function <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> • Oscillation feedback resistor : Approximately 20MΩ • With Standby mode control <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=-4mA, I_{OL}=4mA$

Type	Circuit	Remarks
E	<p>The diagram for Type E shows a CMOS output stage. A pull-up resistor R is connected to the output node. The output node is driven by a P-ch transistor (pull-up) and an N-ch transistor (pull-down). The P-ch transistor is controlled by a 'Pull-up resistor control' signal. The N-ch transistor is controlled by a 'Standby mode control' signal. The output node is also connected to a 'Digital output' terminal. A 'Digital input' terminal is connected to the output node through an AND gate, which is also controlled by the 'Standby mode control' signal.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=-4mA, I_{OL}=4mA$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off • +B input is available
F	<p>The diagram for Type F shows a CMOS output stage similar to Type E. It includes a pull-up resistor R, P-ch and N-ch transistors, and digital input/output nodes. The P-ch transistor is controlled by a 'Pull-up resistor control' signal. The N-ch transistor is controlled by a 'Standby mode control' signal. The output node is connected to a 'Digital output' terminal. A 'Digital input' terminal is connected to the output node through an AND gate, controlled by the 'Standby mode control' signal. Additionally, there is an 'Analog input' terminal connected to the output node through an AND gate, controlled by an 'Input control' signal. The 'Input control' signal is also connected to the N-ch transistor's gate.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=-4mA, I_{OL}=4mA$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=-12\text{mA}$, $I_{OL}=12\text{mA}$ • +B input is available
H		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby mode control • $I_{OH}=-25.3\text{mA}$, $I_{OL}=19.7\text{mA}$

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

- (1) **Preventing Over-Voltage and Over-Current Conditions**

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

- (2) **Protection of Output Pins**

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

- (3) **Handling of Unused Input Pins**

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

- **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.

Store products in locations where temperature changes are slight.

- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

When you open Dry Package that recommends humidity 40% to 70% relative humidity.

- (3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

- **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

<http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf>

■ HANDLING DEVICES

- Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 μF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

- Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/ μs when there is a momentary fluctuation on switching the power supply.

- Crystal oscillator circuit

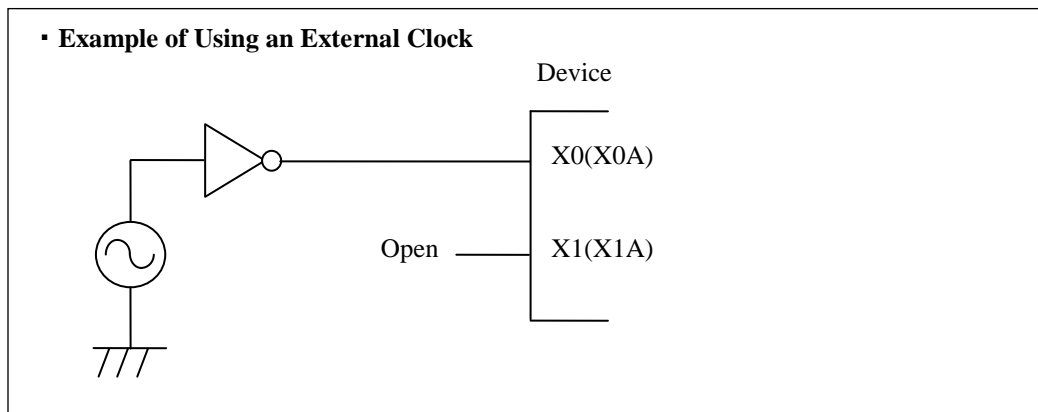
Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

- Using an external clock

When using an external clock, the clock signal should be input to the X0,X0A pin only and the X1,X1A pin should be kept open.



- Handling when using Multi function serial pin as I²C pin

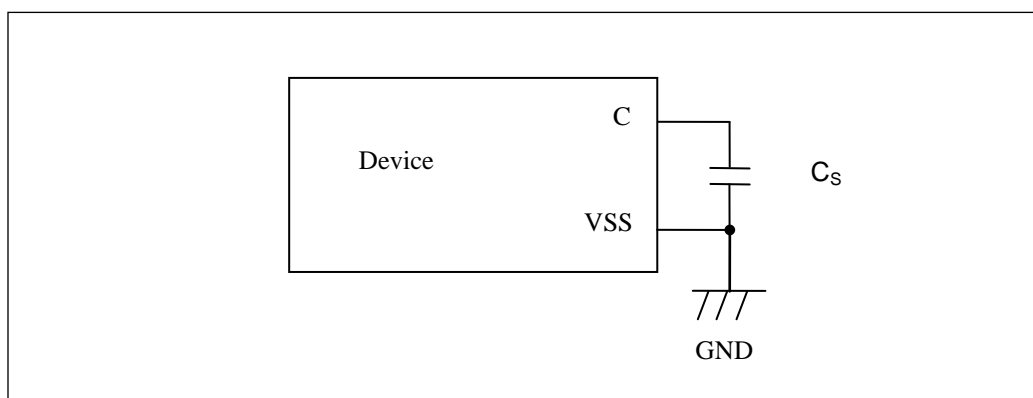
If it is using multi function serial pin as I²C pins, P-ch transistor of digital output is always disable.

However, I²C pins need to keep the electrical characteristic like other pins and not to connect to external I²C bus system with power OFF.

- **C Pin**

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.

However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about $4.7\mu\text{F}$ would be recommended for this series.



- **Mode pins (MD0, MD1)**

Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- **Notes on power-on**

Turn power on/off in the following order or at the same time.

If not using the A/D converter, connect $AVCC = VCC$ and $AVSS = VSS$.

Turning on : $VCC \rightarrow AVCC \rightarrow AVRH$

Turning off : $AVRH \rightarrow AVCC \rightarrow VCC$

- **Serial Communication**

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

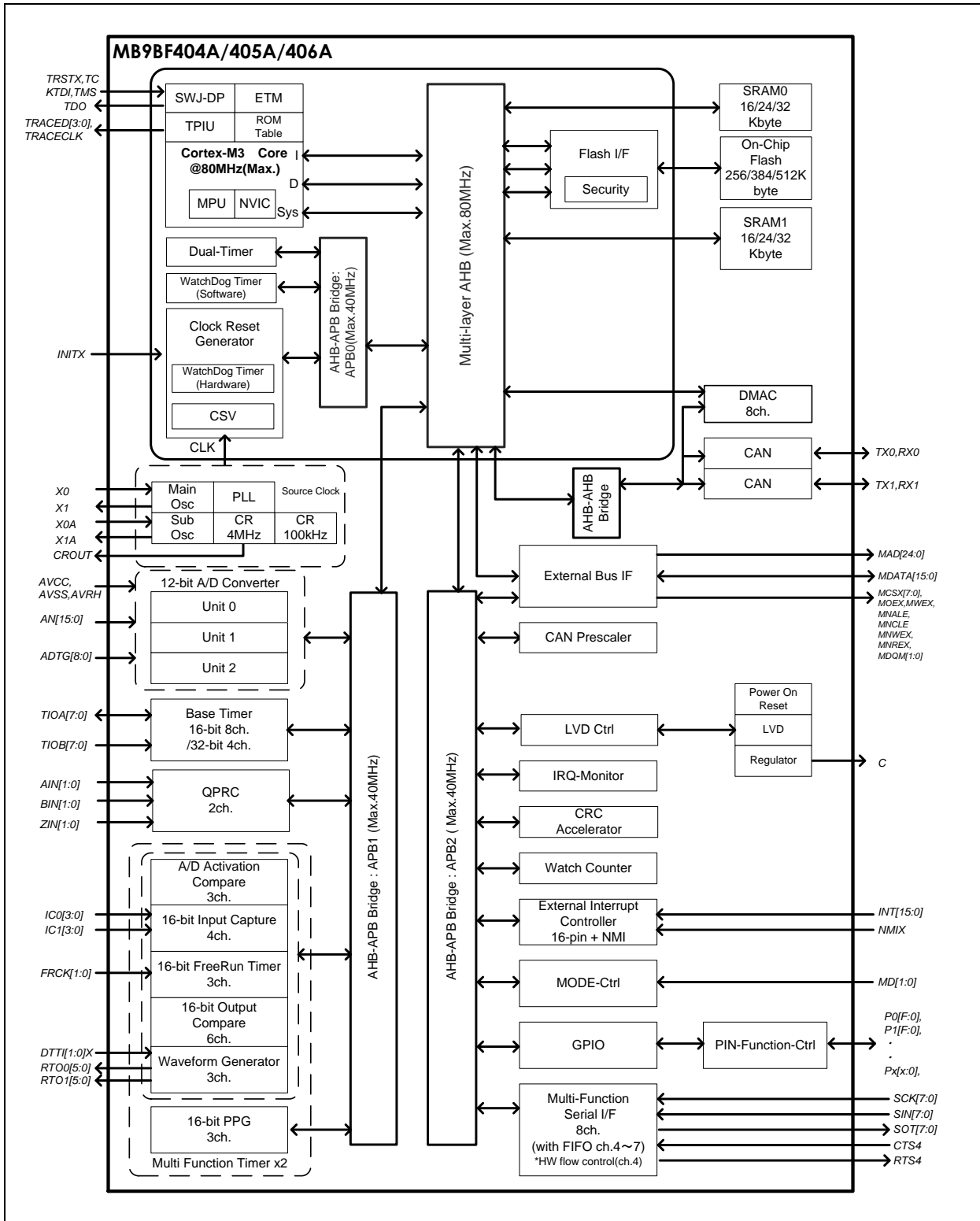
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

- **Differences in features among the products with different memory sizes and between FLASH products and MASK products**

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between FLASH products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

■ BLOCK DIAGRAM

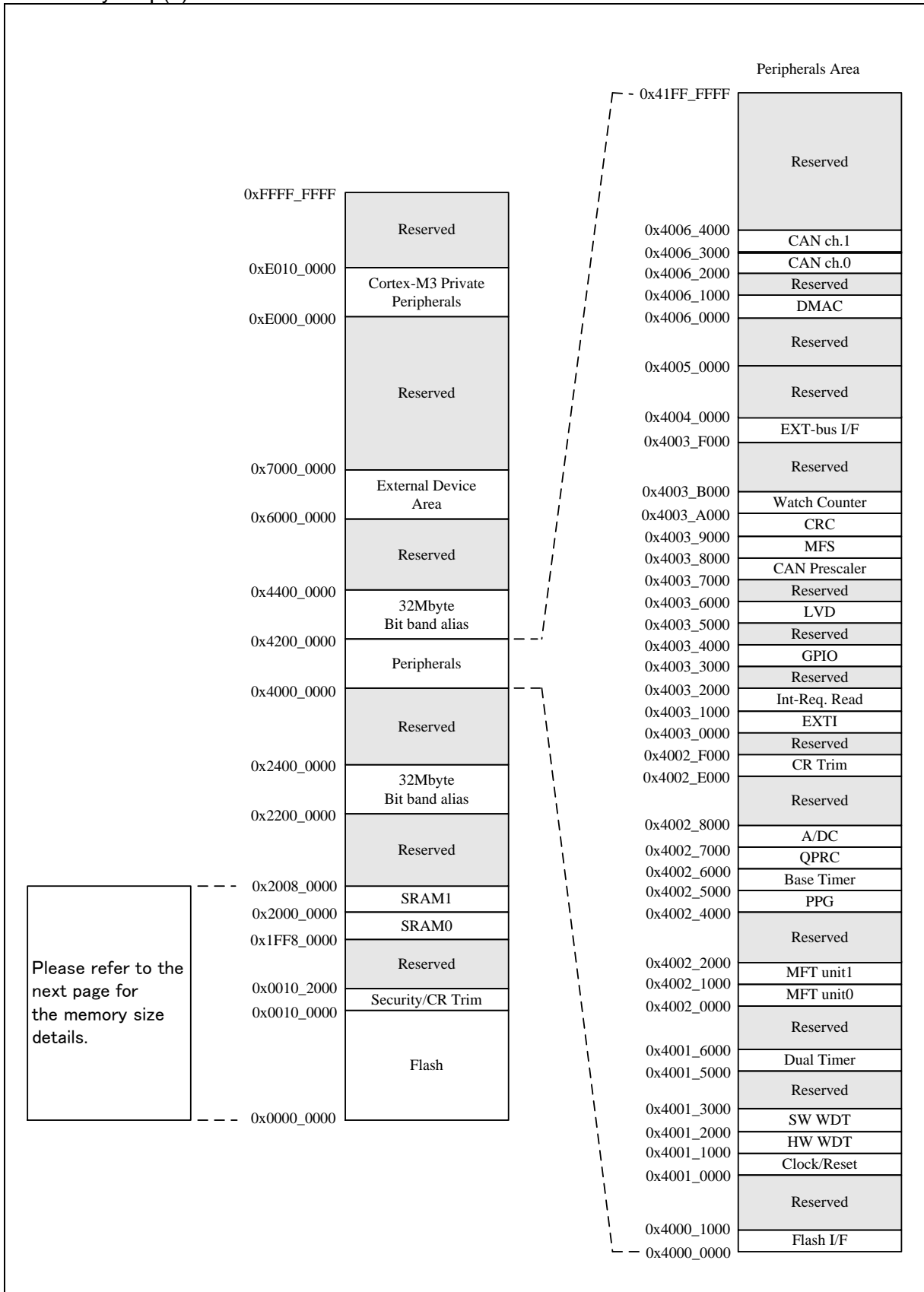


■ MEMORY SIZE

See " • Memory size" in "■PRODUCT LINEUP" to confirm the memory size.

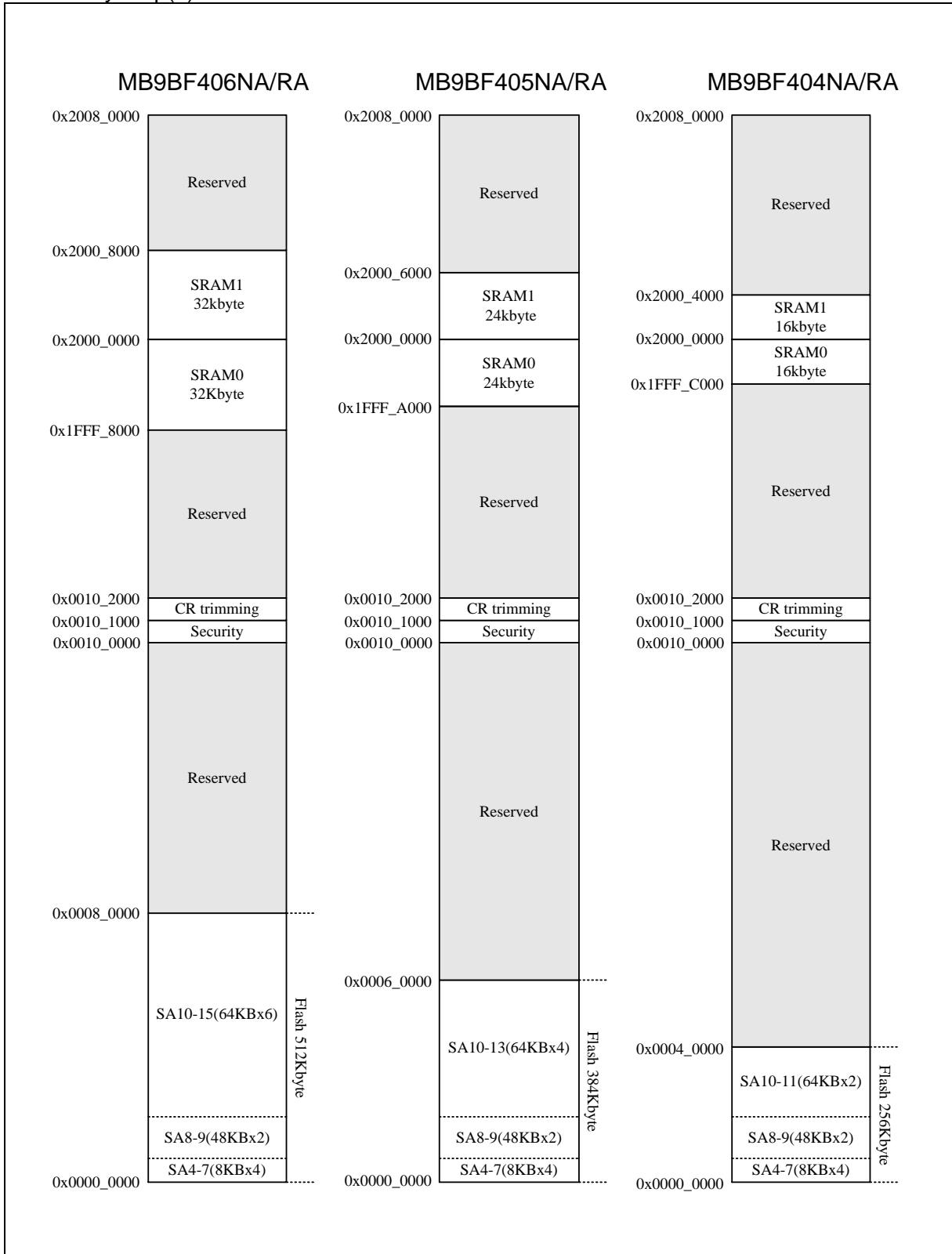
■ MEMORY MAP

• Memory Map(1)



Please refer to the next page for the memory size details.

• Memory Map(2)



*: See "MB9B500/400/300/100/MB9A100 Series Flash programming Manual" for sector structure of Flash.

• Peripheral Address Map

Start address	End address	Bus	Peripherals	
0x4000_0000	0x4000_0FFF	AHB	Flash Memory I/F register	
0x4000_1000	0x4000_FFFF		Reserved	
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control	
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer	
0x4001_2000	0x4001_2FFF		Software Watchdog timer	
0x4001_3000	0x4001_4FFF		Reserved	
0x4001_5000	0x4001_5FFF		Dual-Timer	
0x4001_6000	0x4001_FFFF		Reserved	
0x4002_0000	0x4002_0FFF		APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF	Multi-function timer unit1		
0x4002_2000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	PPG		
0x4002_5000	0x4002_5FFF	Base Timer		
0x4002_6000	0x4002_6FFF	Quadrature Position/Revolution Counter		
0x4002_7000	0x4002_7FFF	A/D Converter		
0x4002_8000	0x4002_DFFF	Reserved		
0x4002_E000	0x4002_EFFF	Internal CR trimming		
0x4002_F000	0x4002_FFFF	Reserved		
0x4003_0000	0x4003_0FFF	APB2		External Interrupt Controller
0x4003_1000	0x4003_1FFF			Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF			Reserved
0x4003_3000	0x4003_3FFF		GPIO	
0x4003_4000	0x4003_4FFF		Reserved	
0x4003_5000	0x4003_5FFF		Low Voltage Detector	
0x4003_6000	0x4003_6FFF		Reserved	
0x4003_7000	0x4003_7FFF		CAN prescaler	
0x4003_8000	0x4003_8FFF		Multi-function serial Interface	
0x4003_9000	0x4003_9FFF		CRC	
0x4003_A000	0x4003_AFFF		Watch Counter	
0x4003_B000	0x4003_EFFF		Reserved	
0x4003_F000	0x4003_FFFF		External Memory interface	
0x4004_0000	0x4004_FFFF		AHB	Reserved
0x4005_0000	0x4005_FFFF	Reserved		
0x4006_0000	0x4006_0FFF	DMAC register		
0x4006_1000	0x4006_1FFF	Reserved		
0x4006_2000	0x4006_2FFF	CAN ch.0		
0x4006_3000	0x4006_3FFF	CAN ch.1		
0x4006_4000	0x41FF_FFFF	Reserved		

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX=0
This is the period when the INITX pin is the "L" level.
- INITX=1
This is the period when the INITX pin is the "H" level.
- SPL=0
This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "0".
- SPL=1
This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "1".
- Input enabled
Indicates that the input function can be used.
- Internal input fixed at "0"
This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z
Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled
Indicates that the setting is disabled.
- Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.
- Analog input is enabled
Indicates that the analog input is enabled.
- Trace output
Indicates that the trace function can be used.

● LIST OF PIN STATUS

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	Main crystal oscillator output pin	H output/ Internal input fixed at "0"/ or Input enabled	H output/ Internal input fixed at "0"	H output/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled		Maintain previous state	Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled		Maintain previous state	Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled		Maintain previous state	Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop (*2)/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop (*2)/ Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"

*1 : Oscillation is stopped at sub timer mode, Low speed CR timer mode, and stop mode.

*2 : Oscillation is stopped at stop mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^{*1,*2}	V _{CC}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Analog power supply voltage ^{*1,*3}	AV _{CC}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Analog reference voltage ^{*1,*3}	AV _{RH}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Input voltage ^{*1}	V _I	V _{SS} - 0.5	V _{CC} + 0.5 (≤ 6.5V)	V	
Analog pin input voltage ^{*1}	V _{IA}	V _{SS} - 0.5	AV _{CC} + 0.5 (≤ 6.5V)	V	
Output voltage ^{*1}	V _O	V _{SS} - 0.5	V _{CC} + 0.5 (≤ 6.5V)	V	
Clamp maximum current	I _{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	Σ [I _{CLAMP}]		+20	mA	*7
"L" level maximum output current ^{*4}	I _{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80, P81
"L" level average output current ^{*5}	I _{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			19.7	mA	P80, P81
"L" level total maximum output current	Σ I _{OL}	-	100	mA	
"L" level total average output current ^{*6}	Σ I _{OLAV}	-	50	mA	
"H" level maximum output current ^{*4}	I _{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80, P81
"H" level average output current ^{*5}	I _{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 25.3	mA	P80, P81
"H" level total maximum output current	Σ I _{OH}	-	- 100	mA	
"H" level total average output current ^{*6}	Σ I _{OHAV}	-	- 50	mA	
Power consumption	P _D	-	800	mW	
Storage temperature	T _{STG}	- 55	+ 150	°C	

*1 : These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0V.

*2 : V_{CC} must not drop below V_{SS} - 0.5V.

*3 : Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

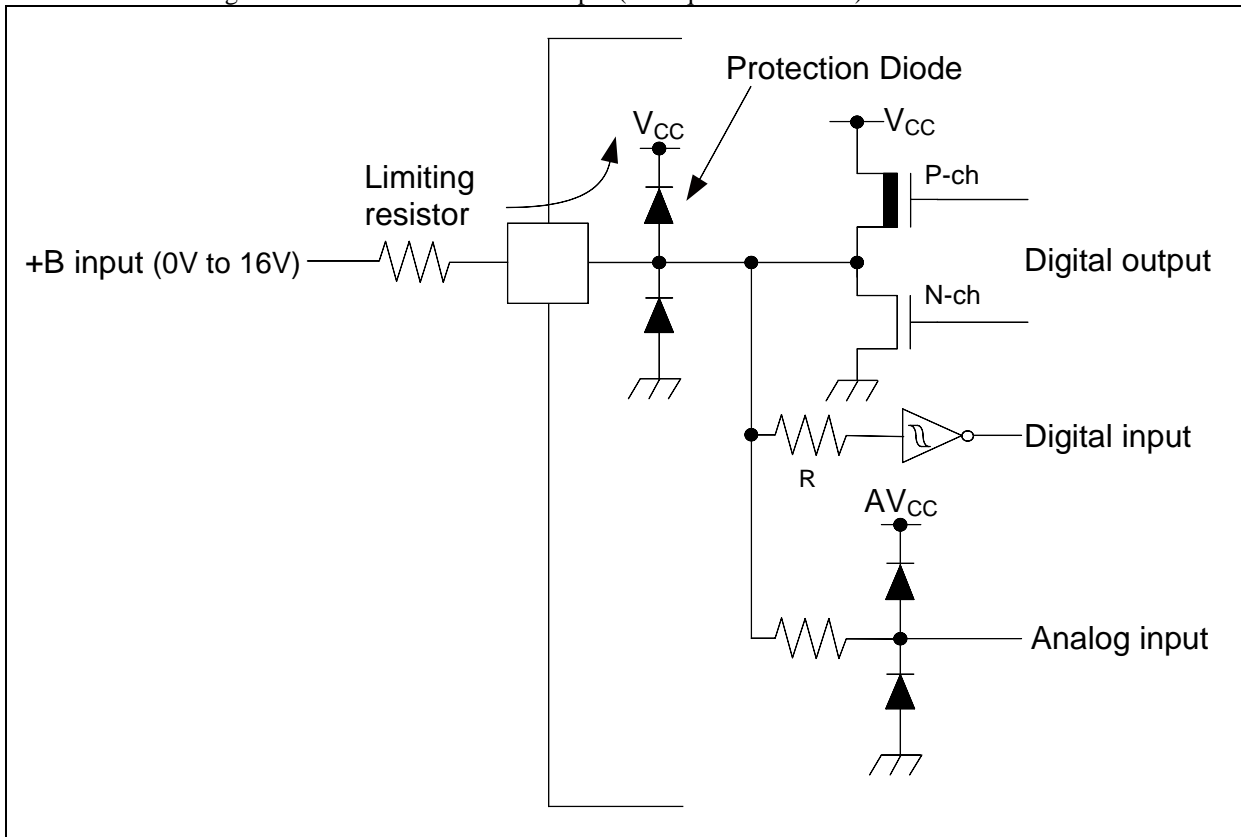
*4 : The maximum output current is the peak value for a single pin.

*5 : The average output is the average current for a single pin over a period of 100 ms.

*6 : The total average output current is the average current for all pins over a period of 100 ms.

*7 :

- See "■LIST OF PIN FUNCTIONS" and "■I/O CIRCUIT TYPE" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



<WARNING>

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks	
			Min	Max			
Power supply voltage	V _{CC}	-	2.7* ²	5.5	V		
Analog power supply voltage	AV _{CC}	-	2.7	5.5	V	AV _{CC} = V _{CC}	
Analog reference voltage	AV _{RH}	-	2.7	AV _{CC}	V		
Smoothing capacitor	C _S	-	1	10	μF	For built-in regulator* ¹	
Operating Temperature	FPT-120P-M21 FPT-120P-M37 FPT-100P-M20 FPT-100P-M23 BGA-112P-M04	T _a	When mounted on four-layer PCB	- 40	+ 85	°C	
			When mounted on double-sided single-layer PCB	- 40	+ 85	°C	I _{CC} ≤ 100mA
				- 40	+ 70	°C	I _{CC} > 100mA

*1 : See " · C Pin" in "■HANDLING DEVICES" for the connection of the smoothing capacitor.

*2 : In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(1) Current rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks	
				Typ* ³	Max* ⁴			
RUN mode current	I _{CC}	V _{CC}	CPU : 80MHz, Peripheral : 40MHz, FLASH 2Wait FRWTR.RWT = 10 FSYNDN.SD = 000	96	118	mA	*1, *5	
			CPU : 60MHz, Peripheral : 30MHz, FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000	76	94	mA	*1, *5	
			CPU : 80MHz, Peripheral : 40MHz, FLASH 5Wait FRWTR.RWT = 10 FSYNDN.SD = 011	66	82	mA	*1, *5	
			CPU : 60MHz, Peripheral : 30MHz, FLASH 3Wait FRWTR.RWT = 00 FSYNDN.SD = 011	52	65	mA	*1, *5	
			High-speed CR RUN mode	CPU/Peripheral : 4MHz* ² FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000	6.0	9.2	mA	*1
			Sub RUN mode	CPU/Peripheral : 32kHz FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.2	2.24	mA	*1, *6
			Low-speed CR RUN mode	CPU/Peripheral : 100kHz FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.3	2.36	mA	*1
SLEEP mode current	I _{CCS}	V _{CC}	PLL SLEEP mode	Peripheral : 40MHz	43	54	mA	*1, *5
			High-speed CR SLEEP mode	Peripheral : 4MHz* ²	3.5	6.2	mA	*1
			Sub SLEEP mode	Peripheral : 32kHz	0.15	2.18	mA	*1, *6
			Low-speed CR SLEEP mode	Peripheral : 100kHz	0.22	2.27	mA	*1

*1: When all ports are fixed.

*2: When setting it to 4MHz by trimming.

*3: T_a=+25°C, V_{CC}=3.3V

*4: T_a=+85°C, V_{CC}=5.5V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks	
				Typ*2	Max*3			
TIMER mode current	I _{CC} T	VCC	Main TIMER mode	Ta = + 25°C, When LVD is off	2.4	2.5	mA	*1, *4
				Ta = + 85°C, When LVD is off	-	5.4	mA	*1, *4
			Sub TIMER mode	Ta = + 25°C, When LVD is off	110	300	μA	*1, *5
				Ta = + 85°C, When LVD is off	-	2.2	mA	*1, *5
STOP mode current	I _{CC} H	STOP mode	Ta = + 25°C, When LVD is off	50	200	μA	*1	
			Ta = + 85°C, When LVD is off	-	2	mA	*1	

*1: When all ports are fixed.

*2: V_{CC}=3.3V

*3: V_{CC}=5.5V

*4: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*5: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

· Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I _{CC} LVD	VCC	At operation for interrupt	2	10	μA	At not detect

· Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I _{CC} FLASH	VCC	At Write/Erase	13	24	mA	

· A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AV_{RL} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I _{CC} AD	AVCC	At 1unit operation	2.3	3.6	mA	
			At stop	0.1	2	μA	
Reference power supply current	I _{CC} AVRH	AVRH	At 1unit operation AVRH=5.5V	2.2	3.0	mA	
			At stop	0.03	0.6	μA	

(2) Pin Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0,1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0,1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
"H" level output voltage	V_{OH}	4mA type	$V_{CC} \geq 4.5 V$ $I_{OH} = -4mA$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -2mA$					
		12mA type	$V_{CC} \geq 4.5 V$ $I_{OH} = -12mA$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -8mA$					
		P80, P81	$V_{CC} \geq 4.5 V$ $I_{OH} = -25.3mA$	$V_{CC} - 0.4$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -13.4mA$					
"L" level output voltage	V_{OL}	4mA type	$V_{CC} \geq 4.5 V$ $I_{OL} = 4mA$	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5 V$ $I_{OL} = 2mA$					
		12mA type	$V_{CC} \geq 4.5 V$ $I_{OL} = 12mA$	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5 V$ $I_{OL} = 8mA$					
		P80, P81	$V_{CC} \geq 4.5 V$ $I_{OL} = 19.7mA$	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5 V$ $I_{OL} = 11.9mA$					
Input leak current	I_{IL}	-	-	-5	-	5	μA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5 V$	25	50	100	k Ω	
			$V_{CC} < 4.5 V$	30	80	200		
Input capacitance	C_{IN}	Other than V_{CC} , V_{SS} , AV_{CC} , AV_{SS} , AV_{RH}	-	-	5	15	pF	

4. AC Characteristics

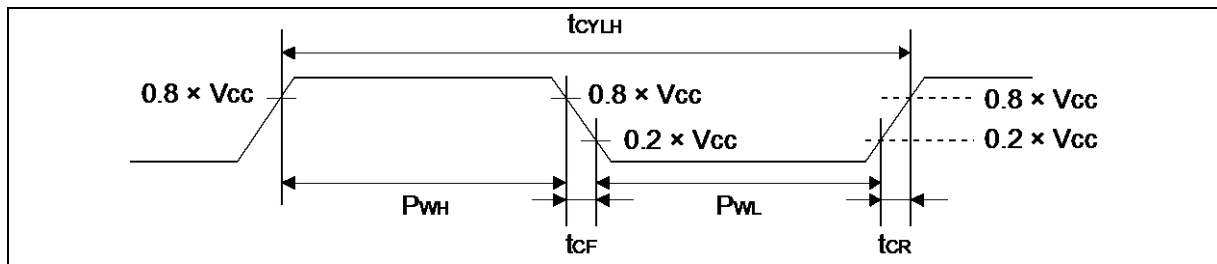
(1) Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F _{CH}	X0 X1	V _{CC} ≥ 4.5V	4	48	MHz	When crystal oscillator is connected
			V _{CC} < 4.5V	4	20		
			V _{CC} ≥ 4.5V	4	48	MHz	
			V _{CC} < 4.5V	4	20		
Input clock cycle	t _{CY LH}		V _{CC} ≥ 4.5V	20.83	250	ns	When using external clock
			V _{CC} < 4.5V	50	250		
Input clock pulse width	-		P _{WH} /t _{CY LH} P _{WL} /t _{CY LH}	45	55	%	When using external clock
Input clock rise time and fall time	t _{CF} t _{CR}		-	-	5	ns	When using external clock
Internal operating clock* ¹ frequency	F _{CM}	-	-	-	80	MHz	Master clock
	F _{CC}	-	-	-	80	MHz	Base clock (HCLK/FCLK)
	F _{CP0}	-	-	-	40	MHz	APB0 bus clock* ²
	F _{CP1}	-	-	-	40	MHz	APB1 bus clock* ²
	F _{CP2}	-	-	-	40	MHz	APB2 bus clock* ²
Internal operating clock* ¹ cycle time	t _{CYCC}	-	-	12.5	-	ns	Base clock (HCLK/FCLK)
	t _{CYCP0}	-	-	25	-	ns	APB0 bus clock* ²
	t _{CYCP1}	-	-	25	-	ns	APB1 bus clock* ²
	t _{CYCP2}	-	-	25	-	ns	APB2 bus clock* ²

*1: For more information about each internal operating clock, see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

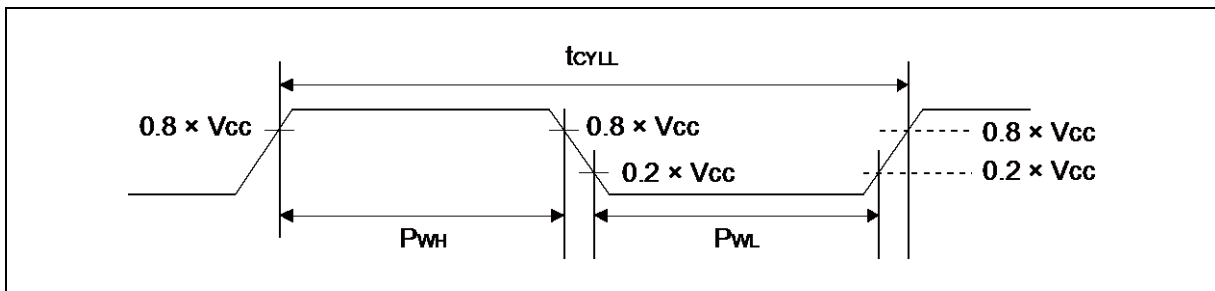
*2: For about each APB bus which each peripheral is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(2) Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F _{CL}	X0A X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t _{CYLL}		-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		P _{WH} /t _{CYLL} P _{WL} /t _{CYLL}	45	-	55	%	When using external clock



(3) Built-in CR Oscillation Characteristics

- Built-in high-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F _{CRH}	T _a = + 25°C	3.92	4	4.08	MHz	When trimming* ¹
		T _a = 0°C to + 70°C	3.84	4	4.16		
		T _a = - 40°C to + 85°C	3.8	4	4.2		
		T _a = - 40°C to + 85°C	3	4	5		When not trimming
Frequency stability time	t _{CRWT}	-	-	50	μs	* ²	

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: Frequency stable time is time to stable of the frequency of the High-speed CR.

clock after the trim value is set. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

- Built-in low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F _{CRL}	-	50	100	150	kHz	

(4-1) Operating Conditions of Main PLL(In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)* ¹	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLLI}	4	-	30	MHz	
PLL multiple rate	-	4	-	30	multiple	
PLL macro oscillation clock frequency	f _{PLLO}	60	-	120	MHz	
Main PLL clock frequency* ²	F _{CLKPLL}	-	-	80	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

(4-2) Operating Conditions of Main PLL(In the case of using built-in high speed CR)

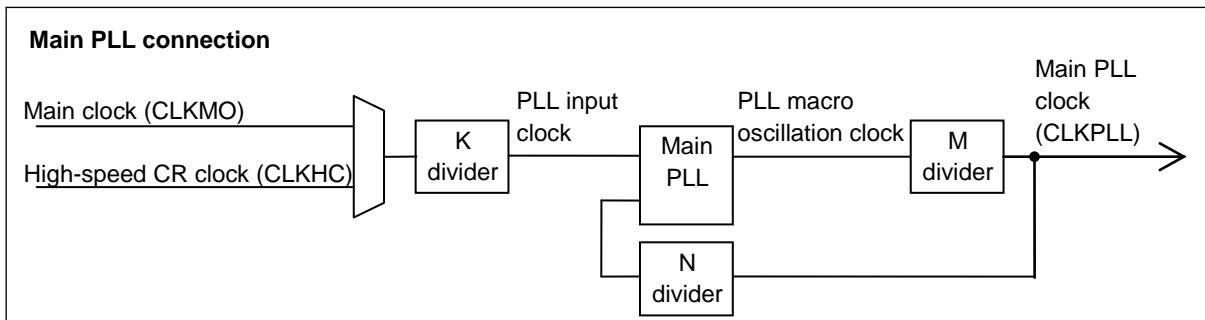
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)* ¹	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	15	-	28	multiple	
PLL macro oscillation clock frequency	f _{PLLO}	57	-	120	MHz	
Main PLL clock frequency* ²	F _{CLKPLL}	-	-	80	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

Note: Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency has been trimmed.



(5) Reset Input Characteristics

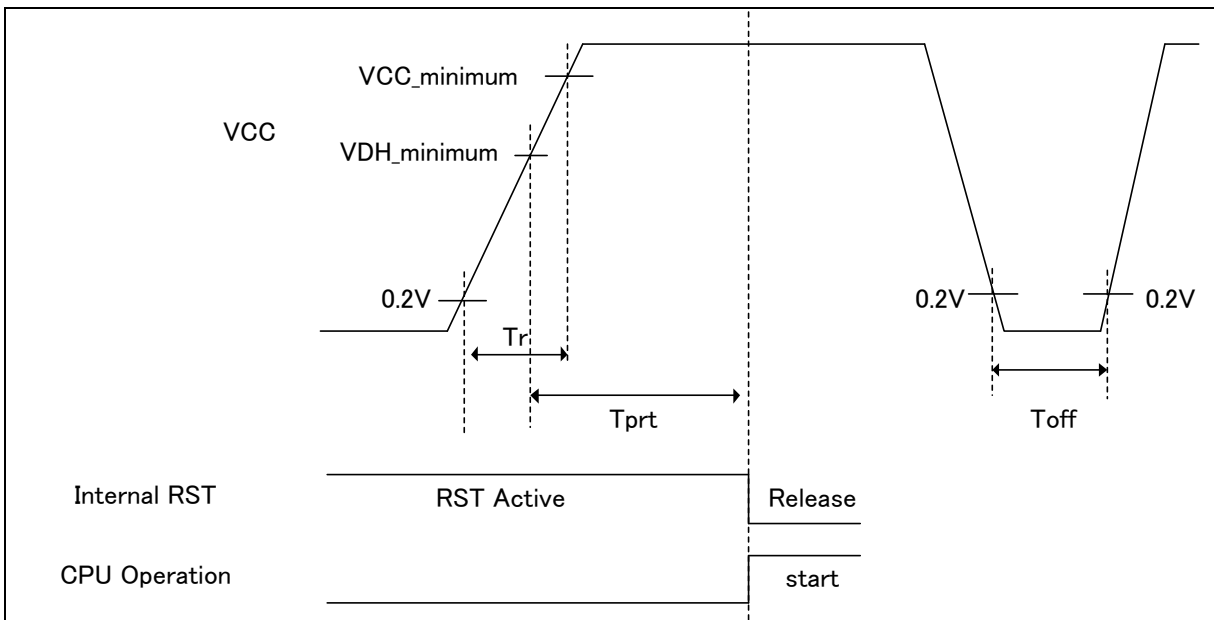
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{INITX}	INITX	-	500	-	ns	

(6) Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	V _{CC}	0	-	ms	
Power supply shut down time	Toff		1	-	ms	
Time until releasing Power-on reset	Tprt		0.422	0.704	ms	



Glossary

- VCC_{minimum} : Minimum V_{CC} of recommended operating conditions
- VDH_{minimum} : Minimum release voltage of Low-Voltage detection reset.
See "6. Low-Voltage Detection Characteristics"

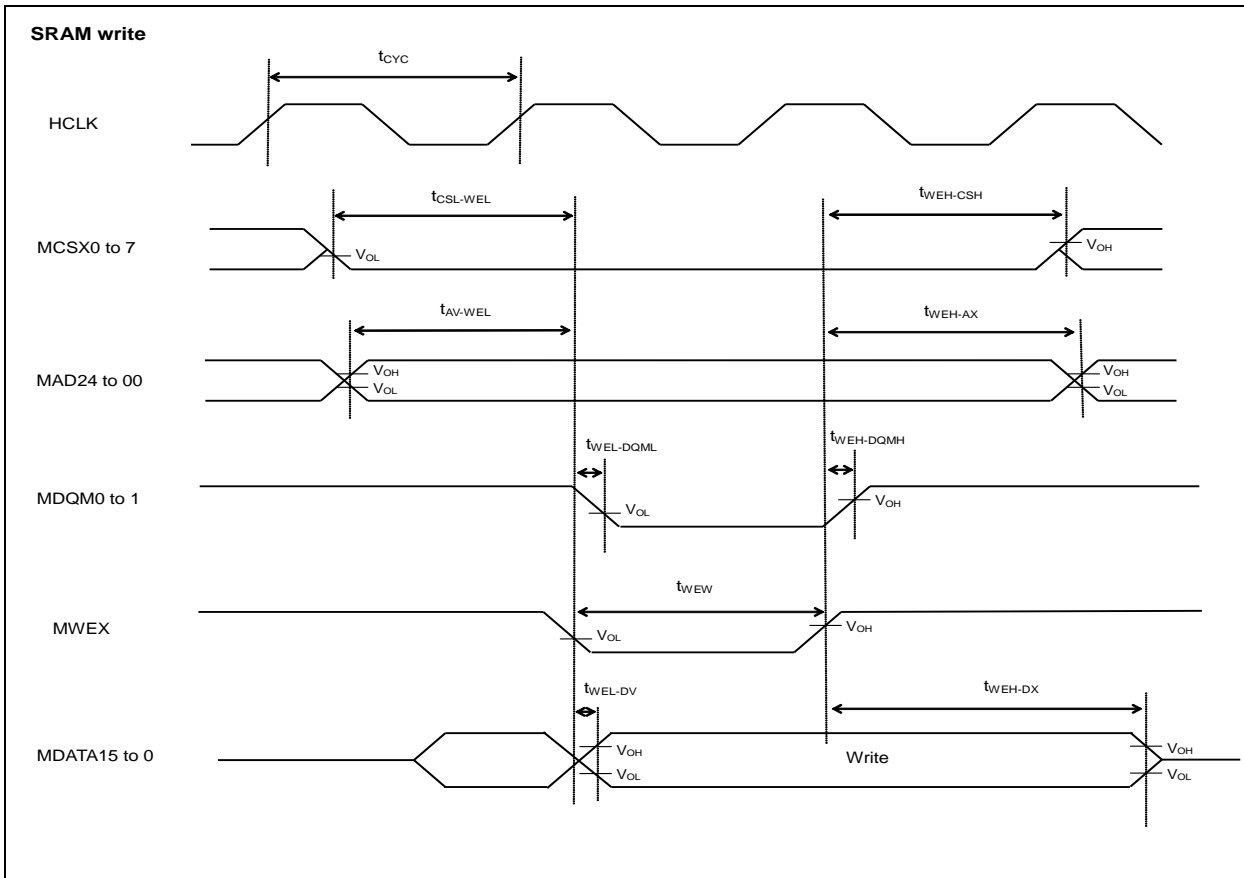
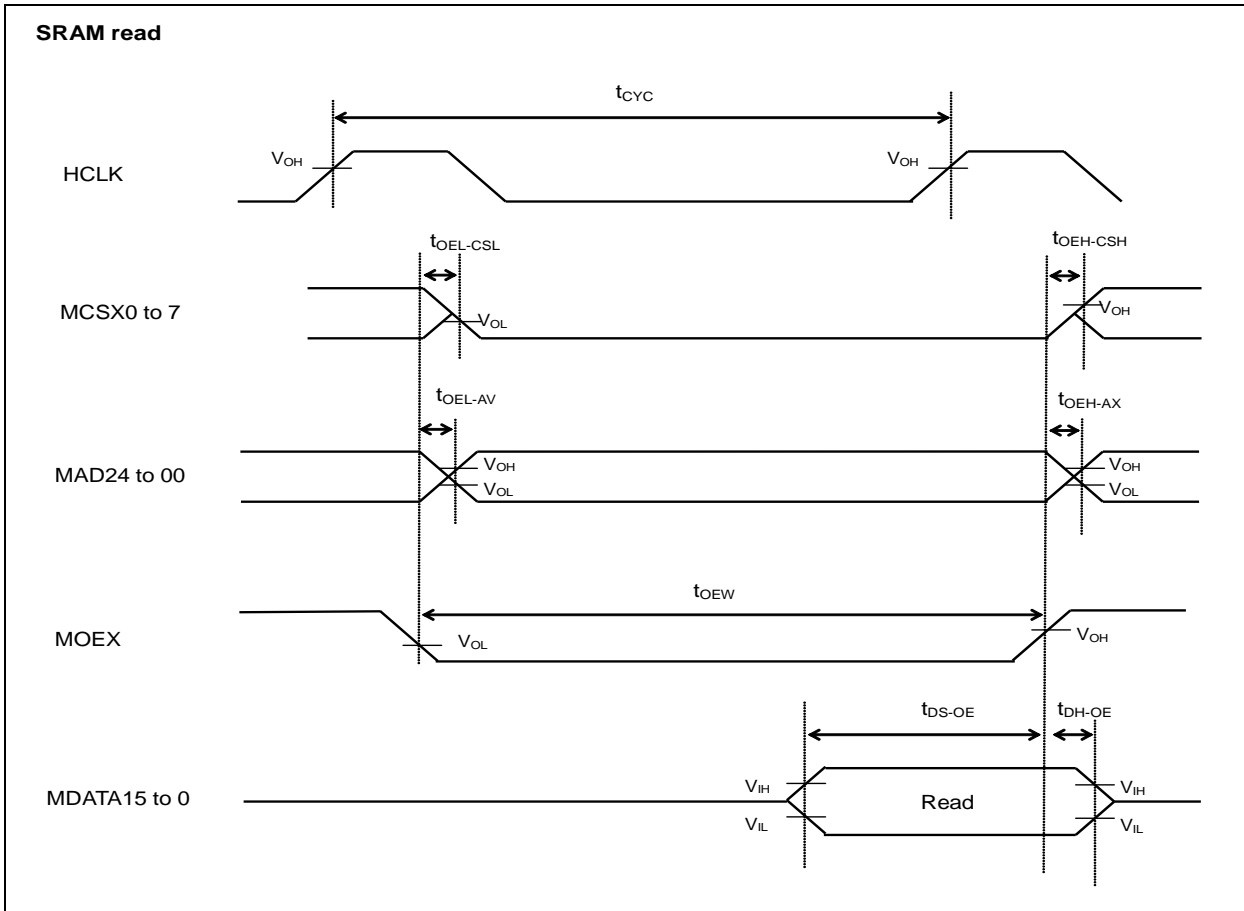
(7) External Bus Timing

· Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Min pulse width	t _{OEW}	MOEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 3	-	ns	
MOEX ↓ ⇒ Address delay time	t _{OEL - AV}	MOEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	10 20	ns	
MOEX ↑ ⇒ Address delay time	t _{OEH - AX}	MOEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	10 20	ns	
MOEX ↓ ⇒ MCSX ↓ delay time	t _{OEL - CSL}	MOEX MCSX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0	10	ns	
MOEX ↑ ⇒ MCSX ↑ delay time	t _{OEH - CSH}	MOEX MCSX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0	10	ns	
Data set up ⇒MOEX ↑ time	t _{DS - OE}	MOEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	20 38	- -	ns	
MOEX ↑ ⇒ Data hold time	t _{DH - OE}	MOEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0	-	ns	
MCSX ↓ ⇒ MWEX ↓ delay time	t _{CSL - WEL}	MCSX MWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 10	- -	ns	
MWEX ↑ ⇒ MCSX ↑ delay time	t _{WEH - CSH}	MCSX MWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 10	- -	ns	
Address ⇒ MWEX ↓ delay time	t _{AV - WEL}	MWEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	
MWEX ↑ ⇒ Address delay time	t _{WEH - AX}	MWEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	
MWEX ↓ ⇒ MDQM ↓ delay time	t _{WEL - DQML}	MWEX MDQM0 to 1	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	5 10	ns	
MWEX ↑ ⇒ MDQM ↑ delay time	t _{WEH - DQMH}	MWEX MDQM0 to 1	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	5 10	ns	
MWEX Min pulse width	t _{WEW}	MWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 3	-	ns	
MWEX ↓ ⇒ Data delay time	t _{WEL - DV}	MWEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	- 5 -15	5 15	ns	
MWEX ↑ ⇒ Data delay time	t _{WEH - DX}	MWEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	

Note: When the external load capacitance = 50pF.

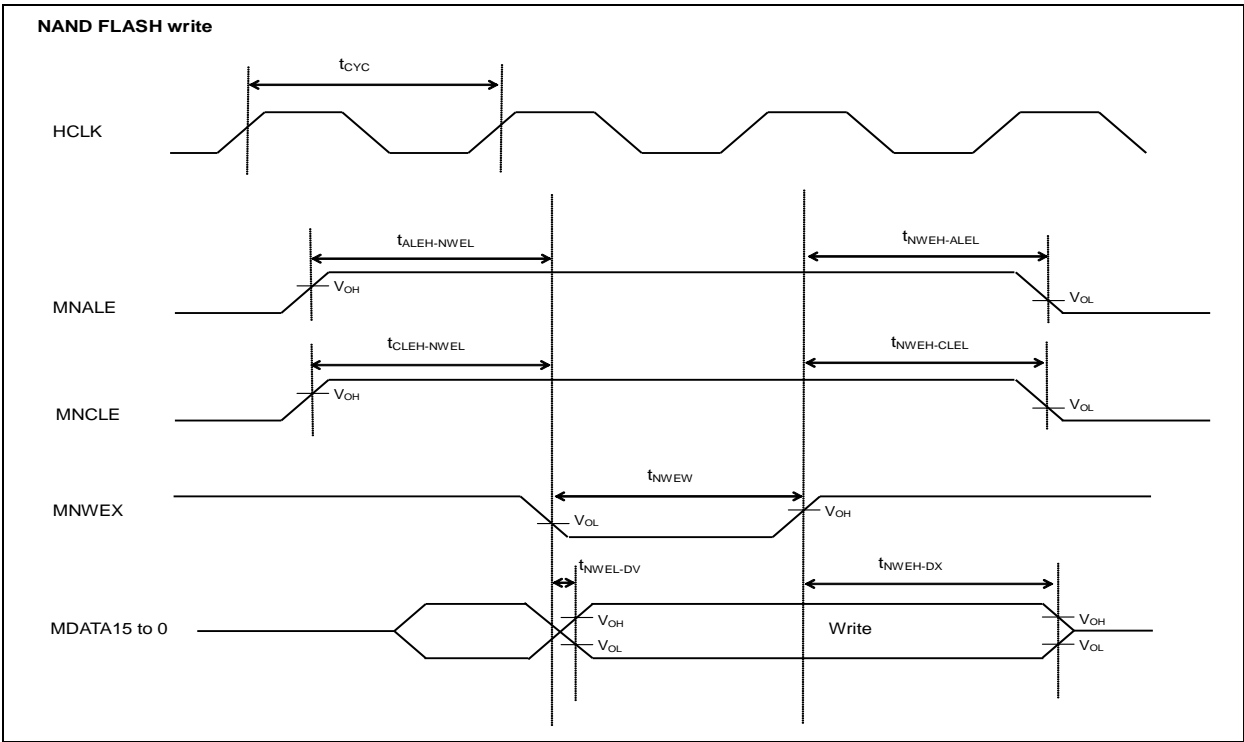
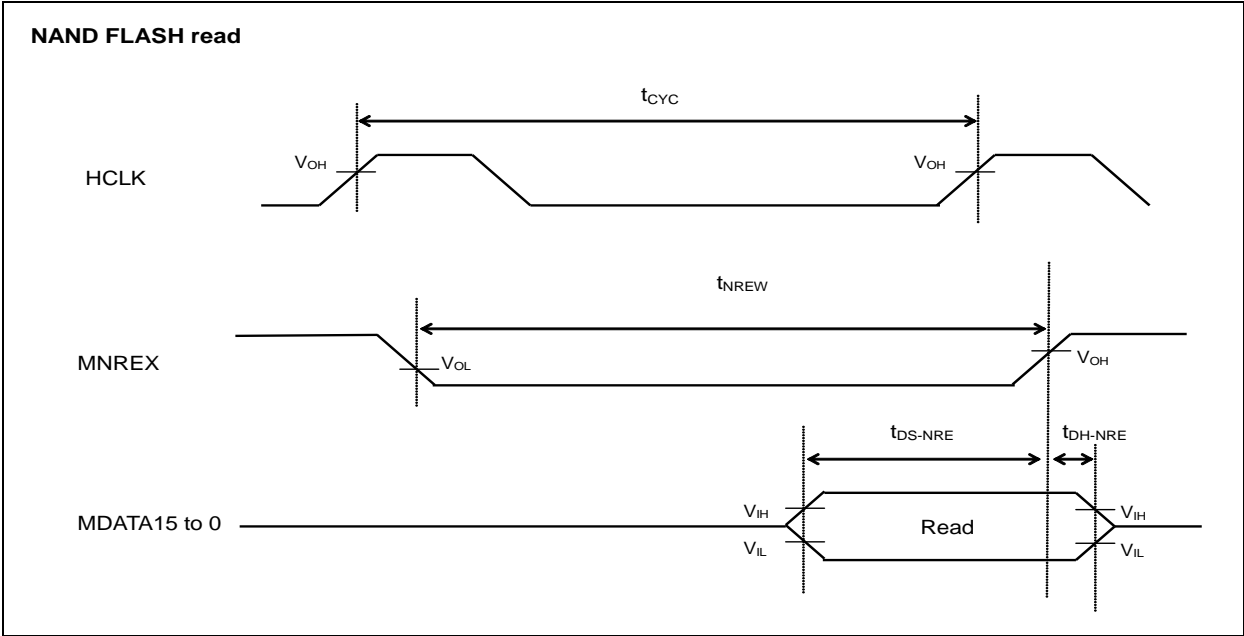


· NAND FLASH mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t _{NREW}	MNREX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 3	-	ns	
Data set up ⇒ MNREX ↑ time	t _{DS - NRE}	MNREX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	20 38	- -	ns	
MNREX ↑ ⇒ Data hold time	t _{DH - NRE}	MNREX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	- -	ns	
MNALE ↑ ⇒ MNWEX delay time	t _{ALEH - NWEL}	MNALE MNWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	
MNWEX ↑ ⇒ MNALE delay time	t _{NWEH - ALEL}	MNALE MNWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	
MNCLE ↑ ⇒ MNWEX delay time	t _{CLEH - NWEL}	MNCLE MNWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	
MNWEX ↑ ⇒ MNCLE delay time	t _{NWEH - CLEL}	MNCLE MNWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	
MNWEX Min pulse width	t _{NWEW}	MNWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 3	-	ns	
MNWEX ↓ ⇒ Data delay time	t _{NWEL - DV}	MNWEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	- 5 -15	+ 5 +15	ns	
MNWEX ↑ ⇒ Data delay time	t _{NWEH - DX}	MNWEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	

Note: when the external load capacitance = 50pF.

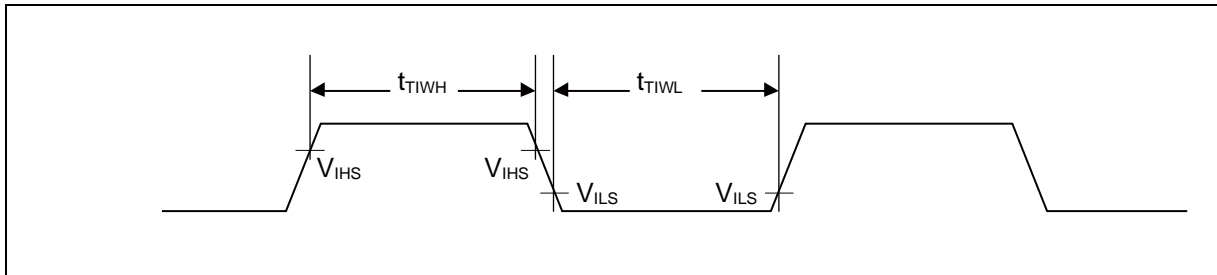


(8) Base Timer Input Timing

· Timer input timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

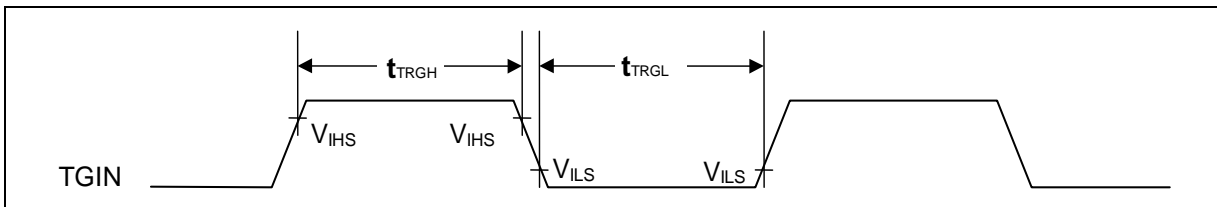
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



· Trigger input timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Base Timer is connected to, see "■BLOCK DIAGRAM" in this data sheet.

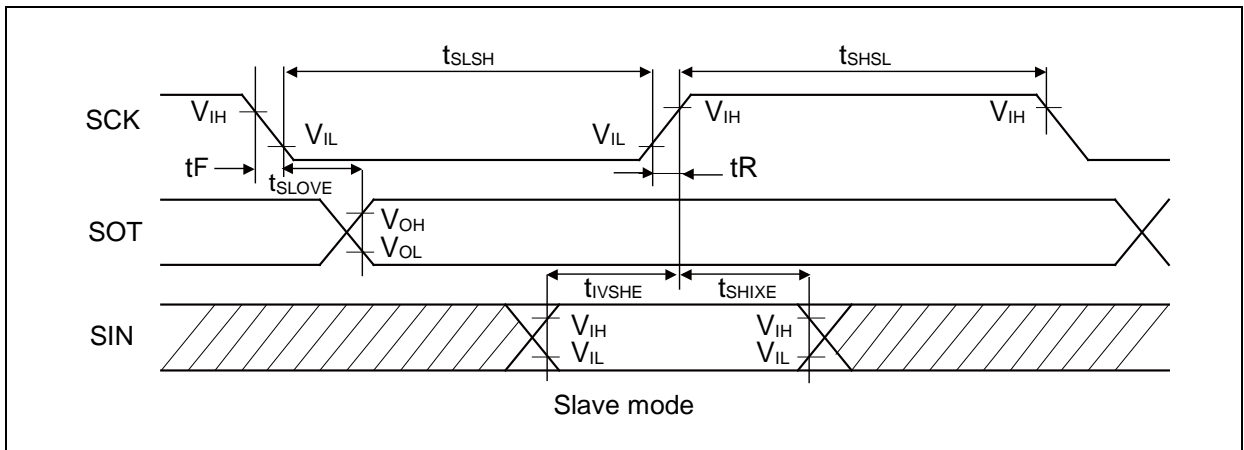
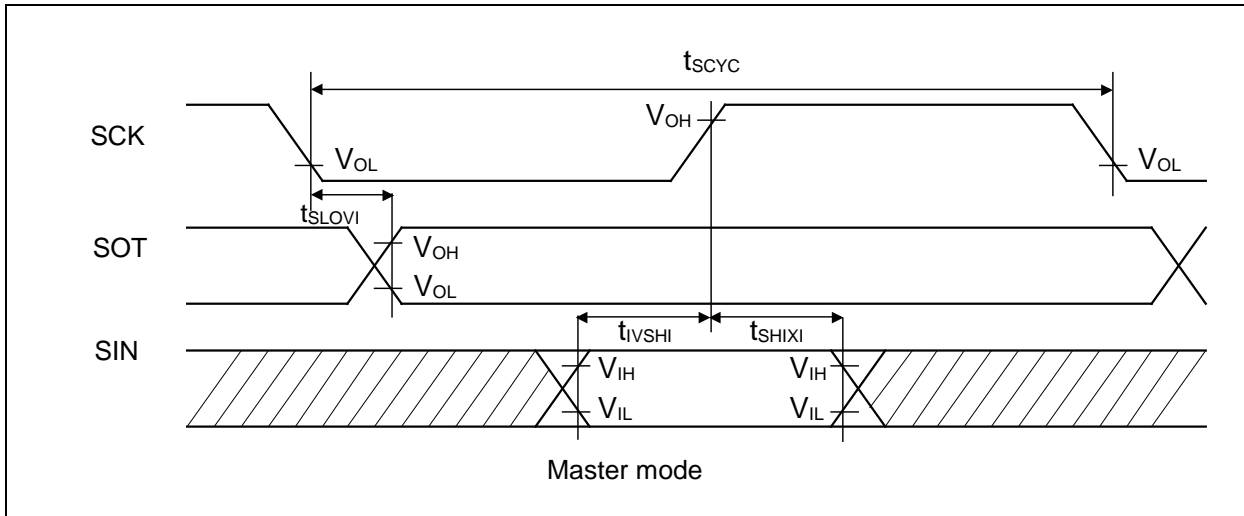
(9) CSIO/UART Timing

· CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCK _X	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK _X SOT _X		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t _{IVSHI}	SCK _X SIN _X		50	-	30	-	ns
SCK ↑ → SIN hold time	t _{SHIXI}	SCK _X SIN _X		0	-	0	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCK _X	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCK _X		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCK _X SOT _X		-	50	-	30	ns
SIN → SCK ↑ setup time	t _{IVSHE}	SCK _X SIN _X		10	-	10	-	ns
SCK ↑ → SIN hold time	t _{SHIXE}	SCK _X SIN _X		20	-	20	-	ns
SCK fall time	t _F	SCK _X		-	5	-	5	ns
SCK rise time	t _R	SCK _X		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time.
 - About the APB bus number which Multi-function Serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCK_{x_0} and SOT_{x_1} is not guaranteed.
 - When the external load capacitance = 50pF.

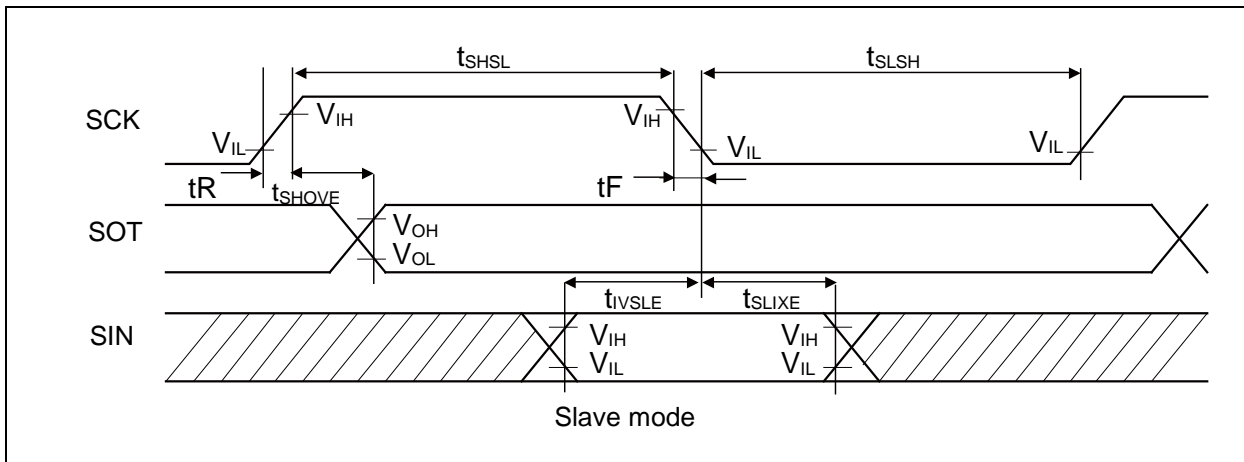
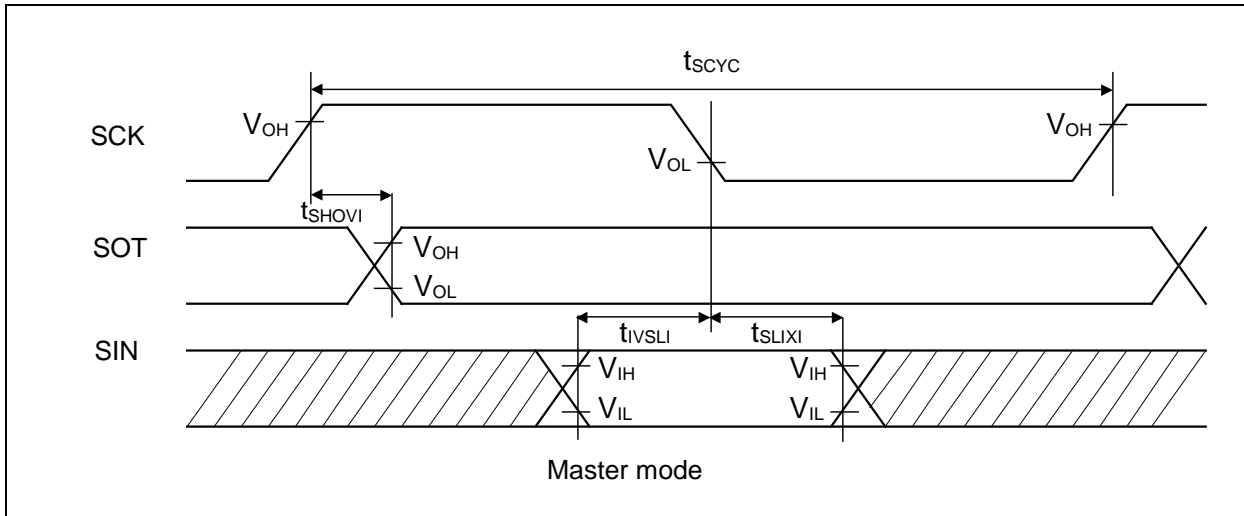


· CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCK _X	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	t _{SHOVI}	SCK _X SOT _X		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t _{IVSLI}	SCK _X SIN _X		50	-	30	-	ns
SCK ↓ → SIN hold time	t _{SLIXI}	SCK _X SIN _X		0	-	0	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCK _X	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCK _X		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	t _{SHOVE}	SCK _X SOT _X		-	50	-	30	ns
SIN → SCK ↓ setup time	t _{IVSLE}	SCK _X SIN _X		10	-	10	-	ns
SCK ↓ → SIN hold time	t _{SLIXE}	SCK _X SIN _X		20	-	20	-	ns
SCK fall time	t _F	SCK _X		-	5	-	5	ns
SCK rise time	t _R	SCK _X		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time.
 - About the APB bus number which Multi-function Serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCK_X_0 and SOT_X_1 is not guaranteed.
 - When the external load capacitance = 50pF.

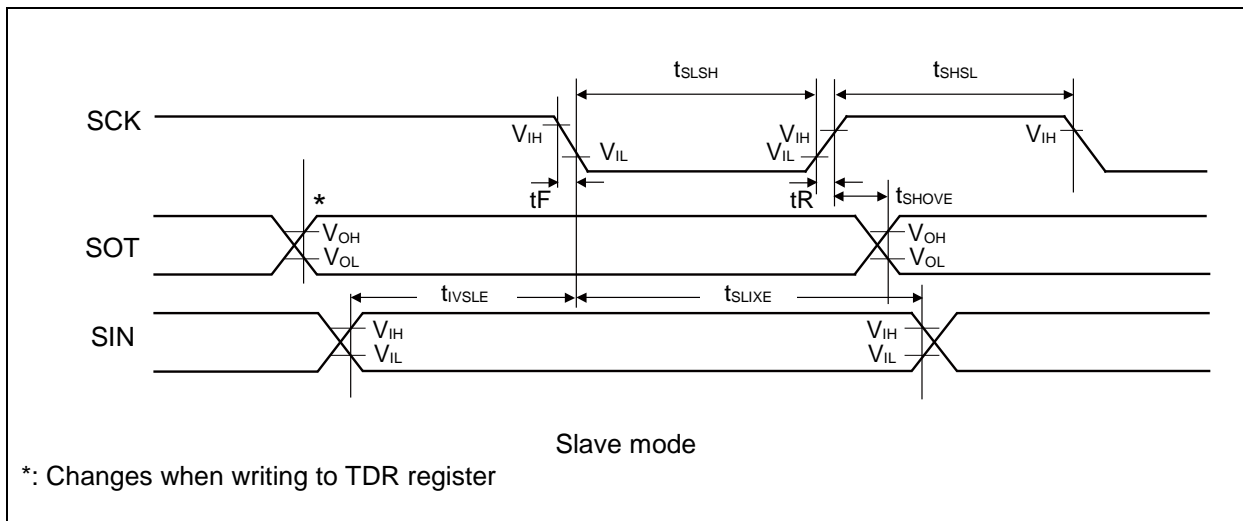
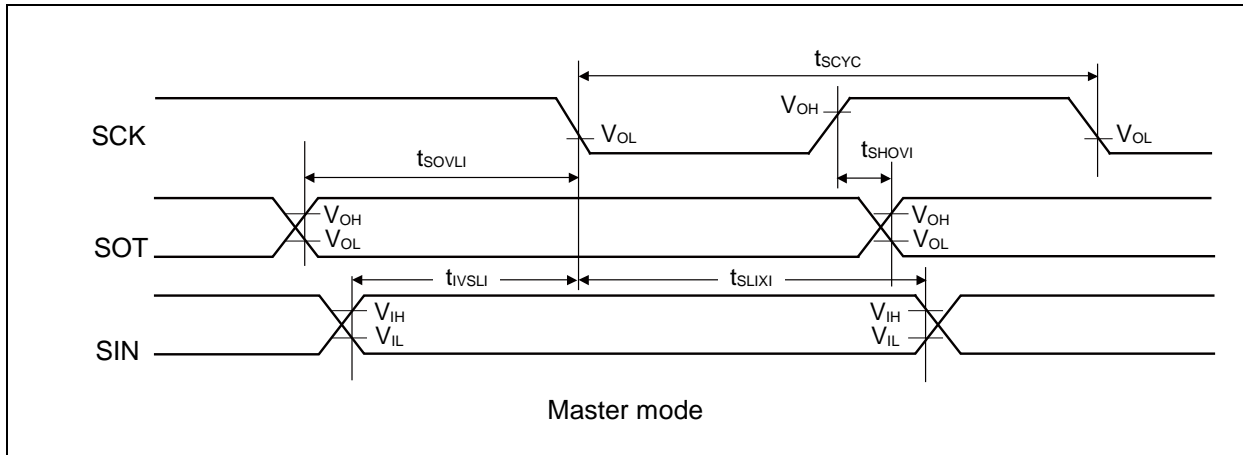


· CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCK _X	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	t _{SHOVI}	SCK _X SOT _X		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t _{IVSLI}	SCK _X SIN _X		50	-	30	-	ns
SCK ↓ → SIN hold time	t _{SLIXI}	SCK _X SIN _X		0	-	0	-	ns
SOT → SCK ↓ delay time	t _{SOVLI}	SCK _X SOT _X		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCK _X		2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCK _X	tcycp + 10	-	tcycp + 10	-	ns	
SCK ↑ → SOT delay time	t _{SHOVE}	SCK _X SOT _X	Slave mode	-	50	-	30	ns
SIN → SCK ↓ setup time	t _{IVSLE}	SCK _X SIN _X		10	-	10	-	ns
SCK ↓ → SIN hold time	t _{SLIXE}	SCK _X SIN _X		20	-	20	-	ns
SCK fall time	t _F	SCK _X		-	5	-	5	ns
SCK rise time	t _R	SCK _X		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time.
 - About the APB bus number which Multi-function Serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantees the same relocate port number.
For example, the combination of SCK_X_0 and SOT_X_1 is not guaranteed.
 - When the external load capacitance = 50pF.

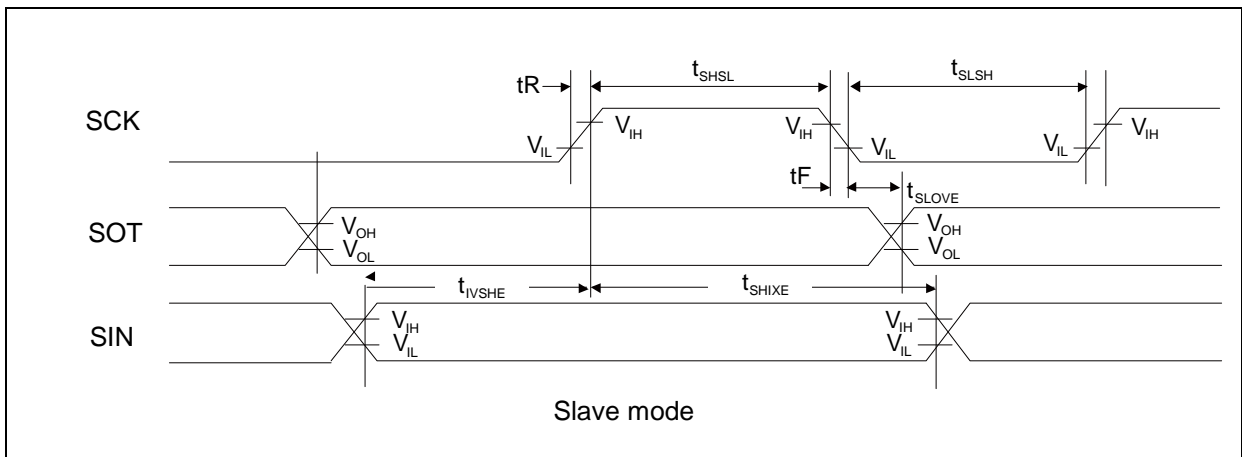
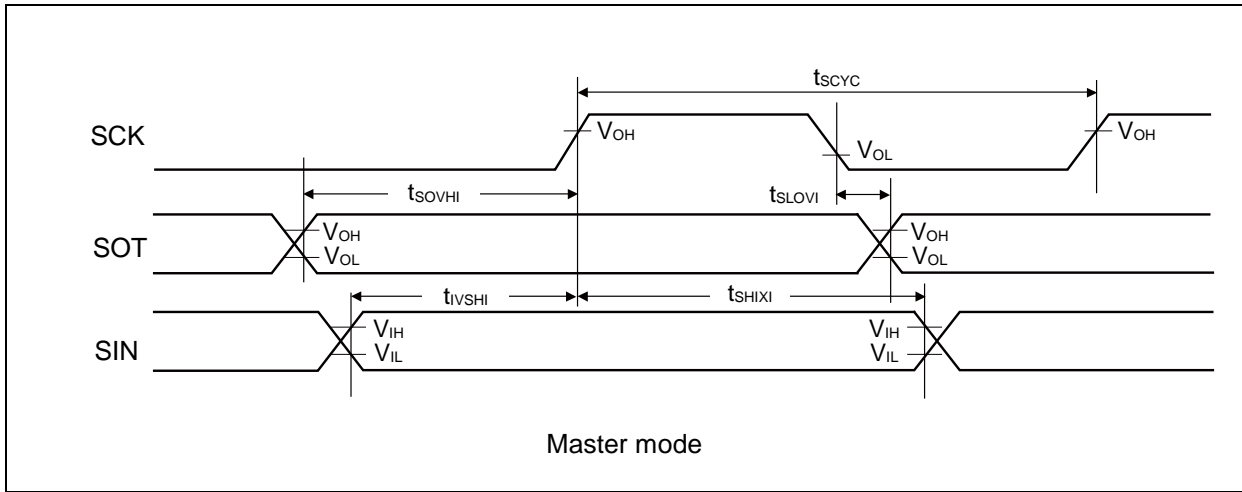


· CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCK _X	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK _X SOT _X		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t _{IVSHI}	SCK _X SIN _X		50	-	30	-	ns
SCK ↑ → SIN hold time	t _{SHIXI}	SCK _X SIN _X		0	-	0	-	ns
SOT → SCK ↑ delay time	t _{SOVHI}	SCK _X SOT _X		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCK _X		2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCK _X	tcycp + 10	-	tcycp + 10	-	ns	
SCK ↓ → SOT delay time	t _{SLOVE}	SCK _X SOT _X	Slave mode	-	50	-	30	ns
SIN → SCK ↑ setup time	t _{IVSHE}	SCK _X SIN _X		10	-	10	-	ns
SCK ↑ → SIN hold time	t _{SHIXE}	SCK _X SIN _X		20	-	20	-	ns
SCK fall time	t _F	SCK _X		-	5	-	5	ns
SCK rise time	t _R	SCK _X		-	5	-	5	ns

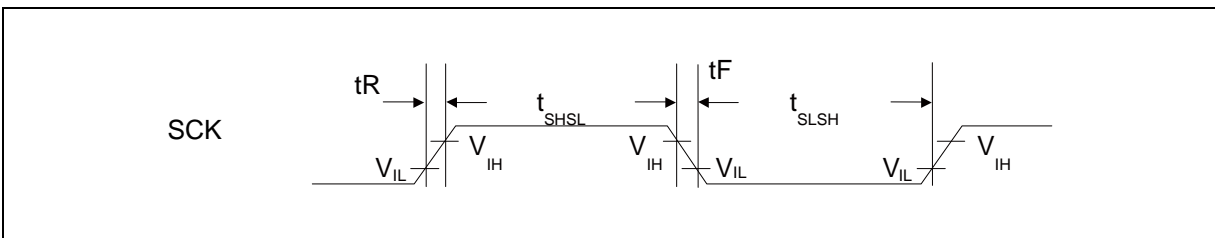
- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time.
 - About the APB bus number which Multi-function Serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCK_{X_0} and SOT_{X_1} is not guaranteed.
 - When the external load capacitance = 50pF.



· UART external clock input (EXT = 1)

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	t_{SLSH}	$C_L = 50pF$	$t_{cycp} + 10$	-	ns	
Serial clock "H" pulse width	t_{SHSL}		$t_{cycp} + 10$	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	



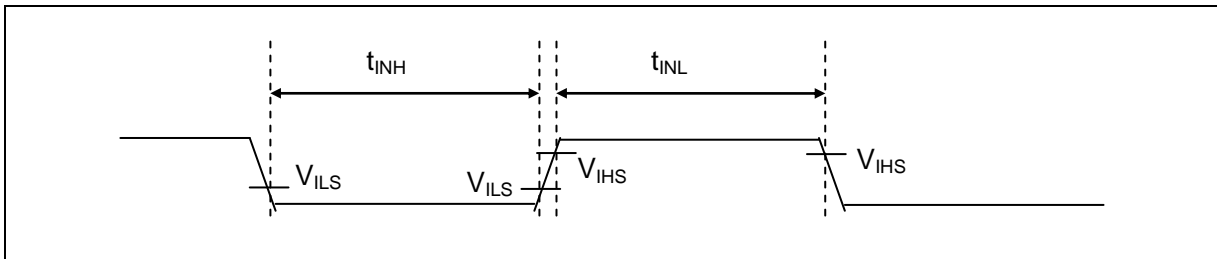
(10) External input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{INH} t _{INL}	ADTG	-	2t _{CYCP} *	-	ns	A/D converter trigger input
		FRCK _x					Free-run timer input clock
		IC _{xx}					Input capture
		DTTI _x X	-	2t _{CYCP} *	-	ns	Wave form generator
		INT _{xx} , NMIX	Except Timer mode, Stop mode	2t _{CYCP} + 100 *	-	ns	External interrupt NMI
	Timer mode, Stop mode	500	-	ns			

* : t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "■BLOCK DIAGRAM" in this data sheet.

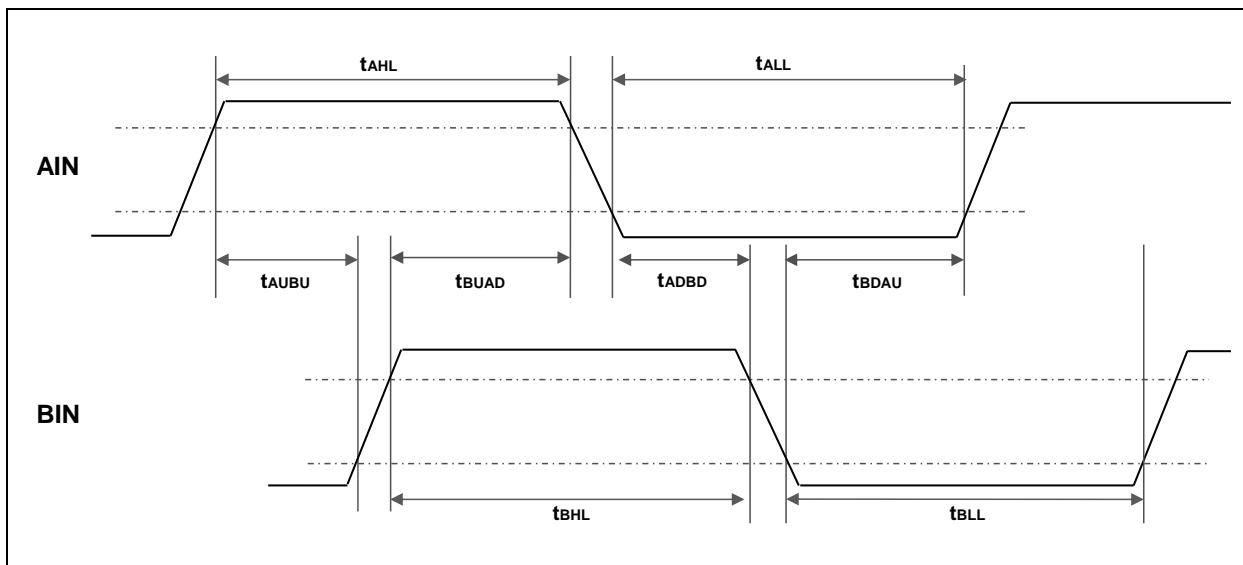


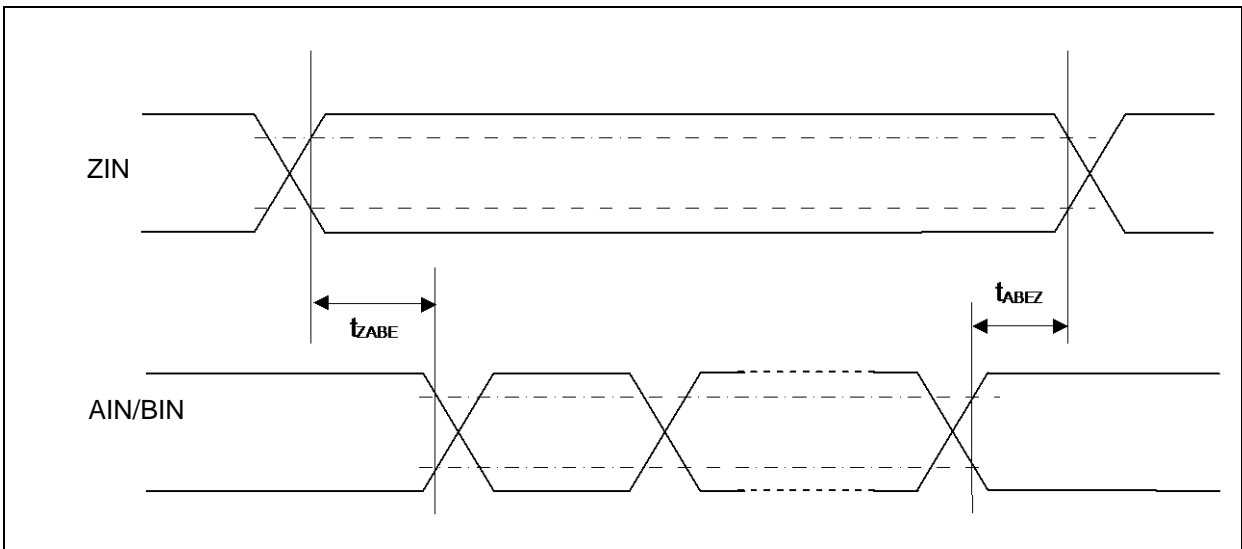
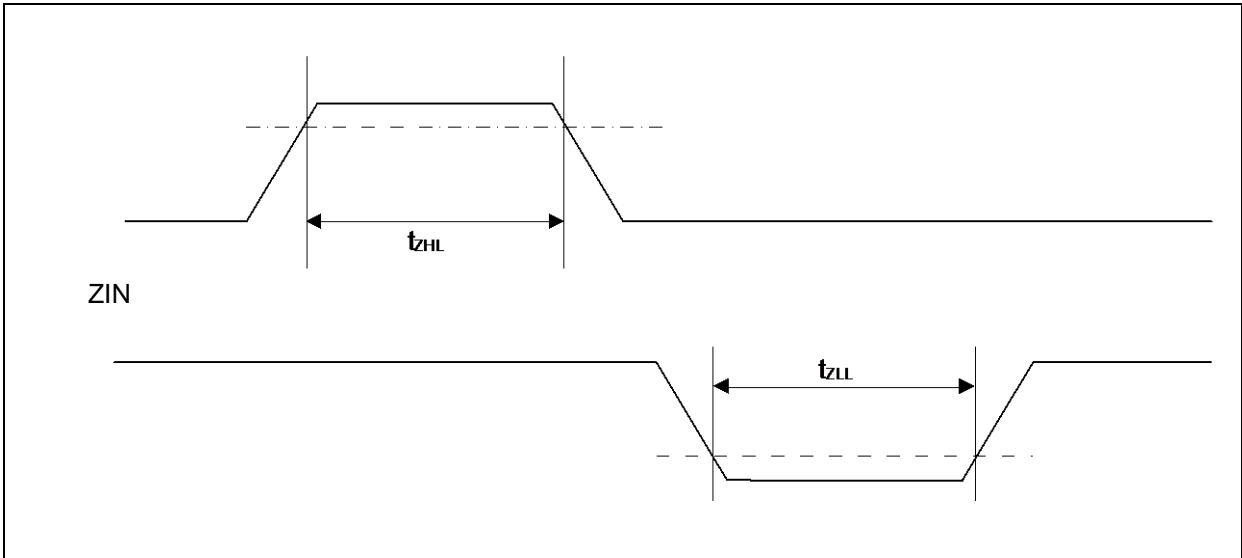
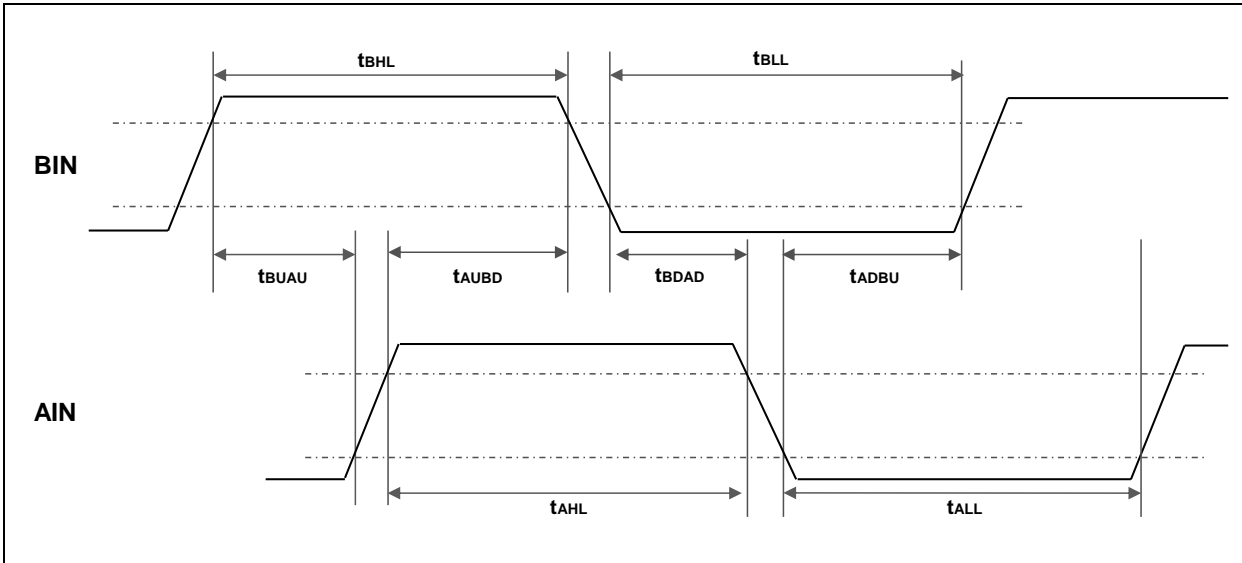
(11) Quadrature Position/Revolution Counter timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t _{AHL}	-	2t _{CYCP} *	-	ns
AIN pin "L" width	t _{ALL}	-			
BIN pin "H" width	t _{BHL}	-			
BIN pin "L" width	t _{BLL}	-			
BIN rise time from AIN pin "H" level	t _{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t _{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t _{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t _{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t _{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t _{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t _{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t _{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t _{ZHL}	QCR:CGSC="0"			
ZIN pin "L" width	t _{ZLL}	QCR:CGSC="0"			
AIN/BIN rise and fall time from determined ZIN level	t _{ZABE}	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rise and fall time	t _{ABEZ}	QCR:CGSC="1"			

*: t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see "■BLOCK DIAGRAM" in this data sheet.





(12) I2C timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F _{SCL}	C _L = 50pF, R = (V _p /I _{OL})* ¹	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HDSTA}		4.0	-	0.6	-	μs	
SCLclock "L" width	t _{LOW}		4.7	-	1.3	-	μs	
SCLclock "H" width	t _{HIGH}		4.0	-	0.6	-	μs	
(Repeated) START setup time SCL ↑ → SDA ↓	t _{SUSTA}		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ²	0	0.9* ³	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		4.0	-	0.6	-	μs	
Bus free time between "STOP condition" and "START condition"	t _{BUF}		4.7	-	1.3	-	μs	
Noise filter	t _{SP}		-	2 t _{CYCP} * ⁴	-	2 t _{CYCP} * ⁴	-	ns

*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.

V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

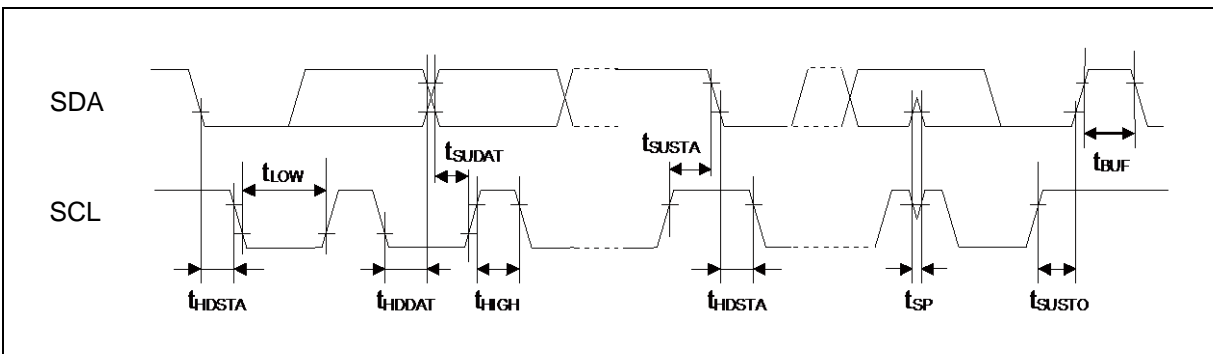
*3 : Fast-mode I²C bus device can be used on Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4 : t_{CYCP} is the APB bus clock cycle time.

About the APB bus number that I2C is connected to, see "■BLOCK DIAGRAM" in this data sheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.

To use Fast-mode, set the APB bus clock at 8 MHz or more.

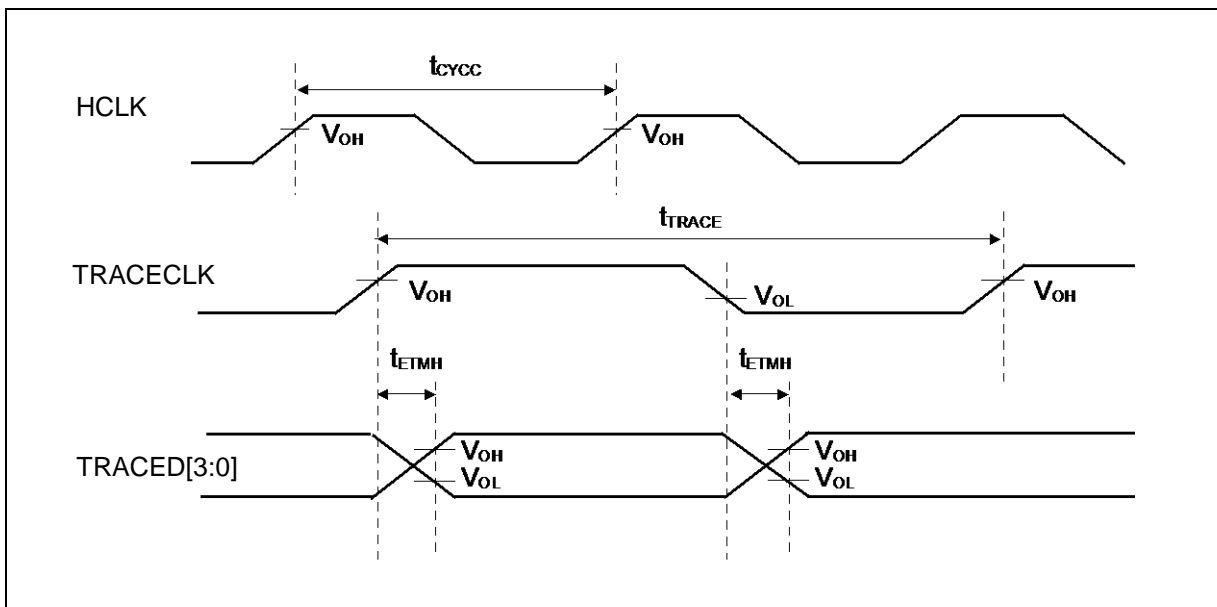


(13) ETM timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED3 - 0	$V_{CC} \geq 4.5V$	2	9	ns	
			$V_{CC} < 4.5V$	2	15		
TRACECLK Frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5V$	-	50	MHz	
			$V_{CC} < 4.5V$	-	32	MHz	
TRACECLK clock cycle time	t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5V$	20	-	ns	
			$V_{CC} < 4.5V$	31.25	-	ns	

Note: When the external load capacitance = 50pF.

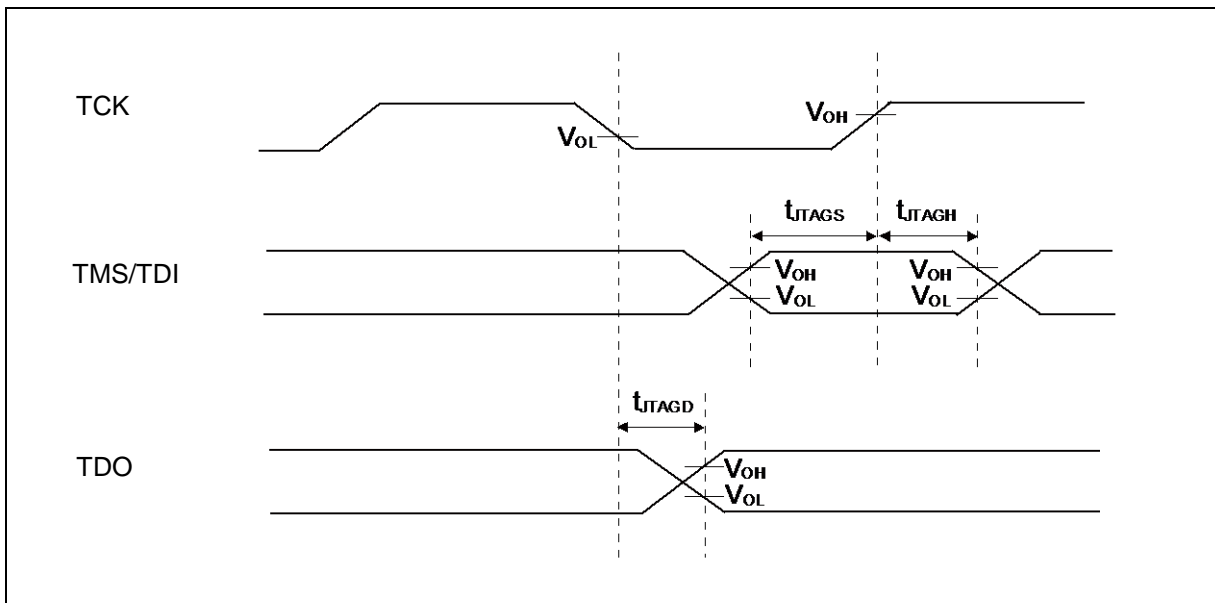


(14) JTAG timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAGS}	TCK TMS,TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TMS,TDI hold time	t_{JTAGH}	TCK TMS,TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TDO delay time	t_{JTAGD}	TCK TDO	$V_{CC} \geq 4.5V$	-	25	ns	
			$V_{CC} < 4.5V$	-	45		

Note: When the external load capacitance = 50pF.



5. 12bit A/D Converter

- Electrical characteristics for the A/D converter.

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 2	± 4.5	LSB	AVRH = 2.7V to 5.5V
Differential Nonlinearity	-	-	-	± 2	± 2.5	LSB	
Zero transition voltage	V _{ZT}	ANxx	-	± 5	± 20	mV	
Full-scale transition voltage	V _{FST}	ANxx	-	AVRH ± 10	AVRH ± 20	mV	
Conversion time	-	-	1.0* ¹	-	-	μs	
			2.666* ¹	-	-		AV _{CC} < 4.5V
Sampling time	T _s	-	*2	-	-	ns	AV _{CC} ≥ 4.5V
			*2	-	-		AV _{CC} < 4.5V
Compare clock cycle *3	T _{ck}	-	55.5	-	10000	ns	AV _{CC} ≥ 4.5V
			166.6* ⁴				AV _{CC} < 4.5V
State transition time to operation permission	T _{stt}	-	-	-	2.5	μs	
Analog input capacity	C _{AIN}	-	-	-	14.5	pF	
Analog input resistance	R _{AIN}	-	-	-	0.93	kΩ	AV _{CC} ≥ 4.5V
					2.04		AV _{CC} < 4.5V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AV _{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV _{CC}	V	

*1: The Conversion time is the value of sampling time(T_s) + compare time(T_c).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5V, HCLK=72MHz sampling time: 0.222μs compare time: 0.778μs

AV_{CC} < 4.5V, HCLK=54MHz sampling time: 0.333μs compare time: 2.333μs

Ensure that it satisfies the value of the sampling time (T_s) and compare clock cycle (T_{ck}).

For setting of the sampling time and compare clock cycle, see "CHAPTER 1-1: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

The registers setting of the A/D Converter are reflected in the operation according to the APB bus clock timing.

The sampling clock and compare clock is generated from the Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "■BLOCK DIAGRAM" in this data sheet.

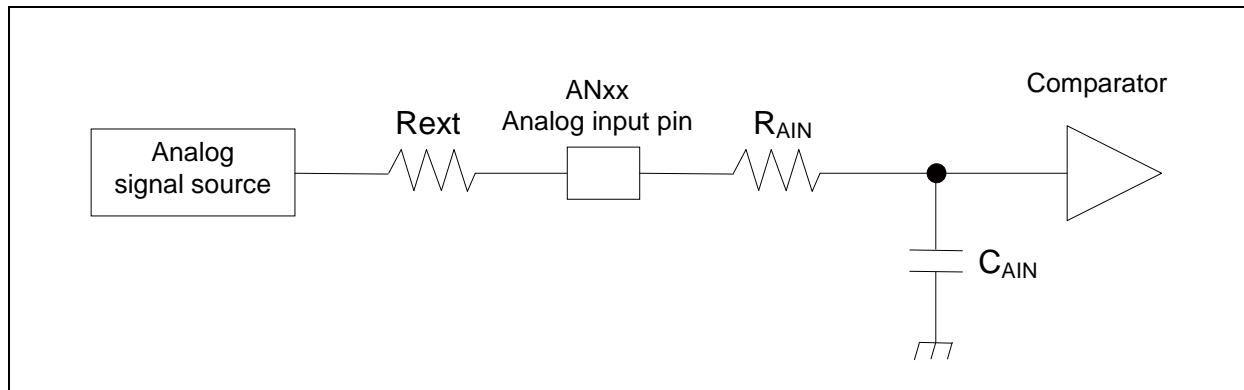
*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1)

*3: The Compare time (T_c) is the value of (Equation 2)

*4: When 12bit A/D converter is used at AV_{CC}<4.5V, there is a limitation as follows.

Please set the HCLK frequency under 54MHz.



$$\text{(Equation 1) } T_s \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$$

T_s : Sampling time

R_{AIN} : input resistance of A/D = $0.93\text{k}\Omega$ $4.5 \leq AV_{CC} \leq 5.5$
 input resistance of A/D = $2.04\text{k}\Omega$ $2.7 \leq AV_{CC} < 4.5$

C_{AIN} : input capacity of A/D = 14.5pF $2.7 \leq AV_{CC} \leq 5.5$

R_{ext} : Output impedance of external circuit

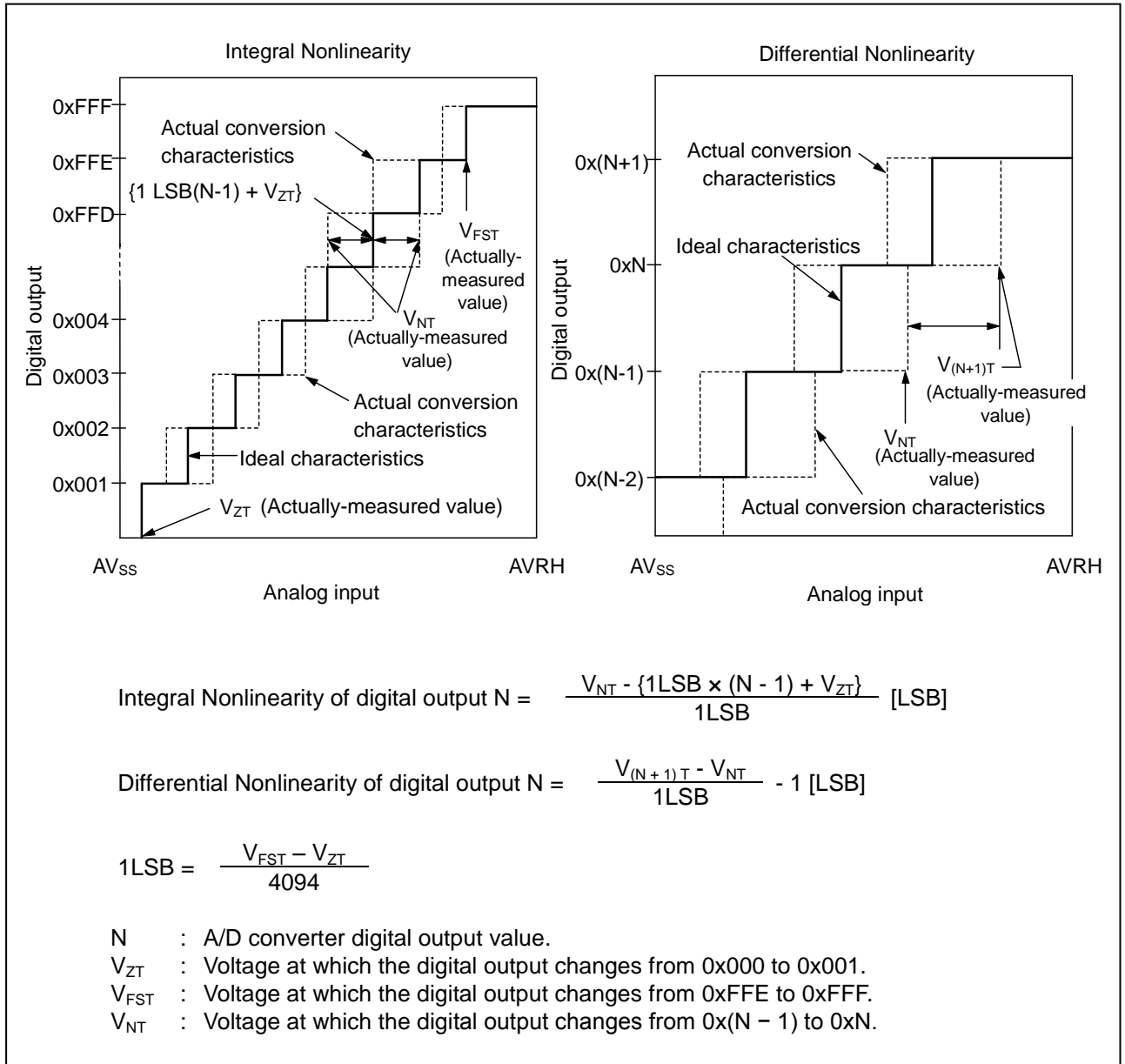
$$\text{(Equation 2) } T_c = T_{cck} \times 14$$

T_c : Compare time

T_{cck} : Compare clock cycle

• Definition of 12-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000 \longleftrightarrow 0b000000000001) and the full-scale transition point (0b111111111110 \longleftrightarrow 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



6. Low-Voltage Detection Characteristics

(1) Low-Voltage Detection Reset

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.20	2.40	2.60	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

(2) Interrupt of Low-Voltage Detection

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T _{LVDW}	-	-	-	2040 × tcycp *	μs	

* : tcycp indicates the APB2 bus clock cycle time.

7. Flash Memory Write/Erase Characteristics

(1) Write / Erase time

(V_{cc} = 2.7V to 5.5V, T_a = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.6	7.5	s	Includes write time prior to internal erase
	Small Sector	0.4	2.1		
Half word (16 bit) write time		25	400	μs	Not including system-level overhead time.
Chip erase time		16	76.8	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

(2) Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20 *	
10,000	10 *	
100,000	5 *	

*: At average + 85°C

8. Return Time from Low-Power Consumption Mode

(1) Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

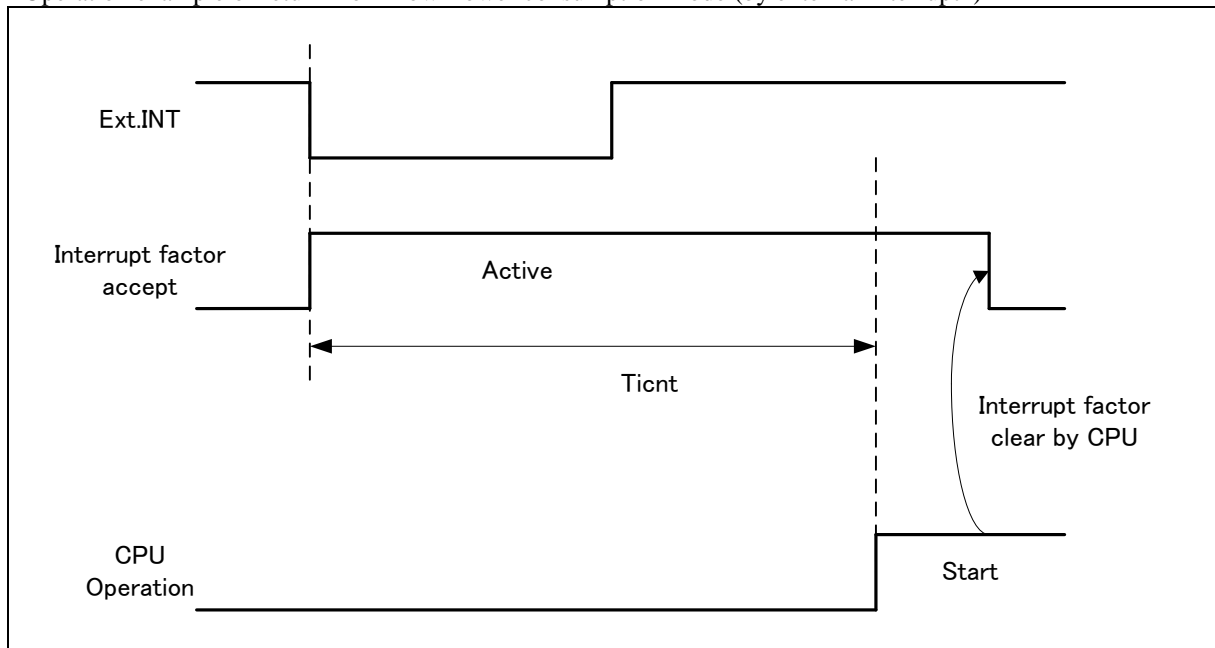
- Return Count Time

($V_{CC} = 2.7V$ to $5.5V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t _{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		33	100	μs	
Low-speed CR TIMER mode		445	1061	μs	
Sub TIMER mode		445	1061	μs	
STOP mode		445	1061	μs	

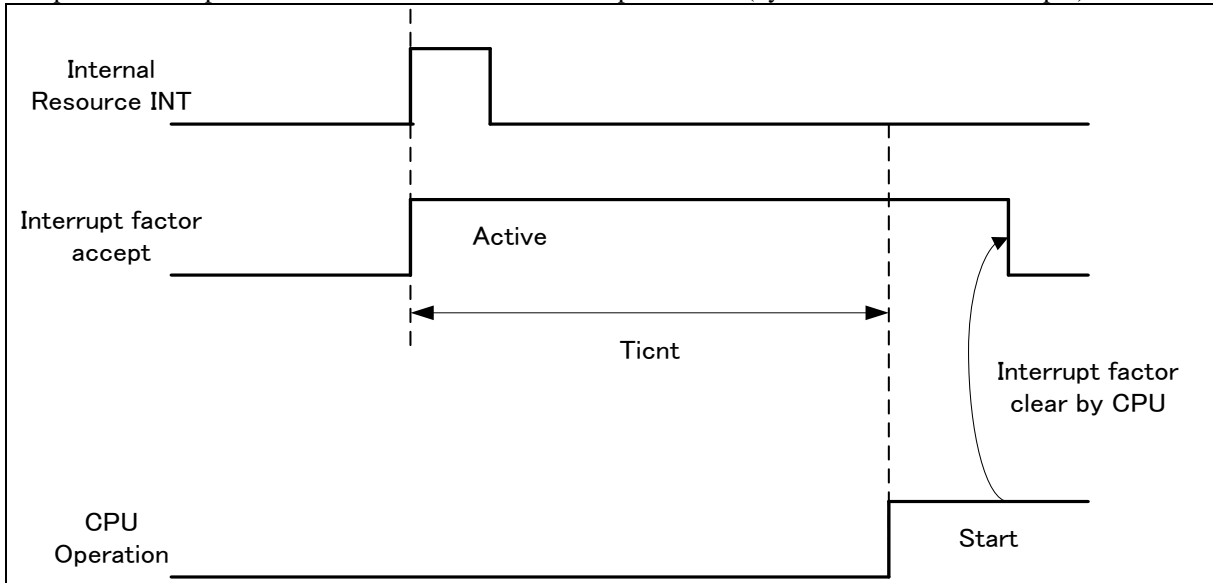
*: The maximum value depends on the accuracy of built-in CR.

- Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

• Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

- Notes:
- The return factor is different in each Low-Power consumption modes. See "CHAPTER 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family PERIPHERAL MANUAL about the return factor from Low-Power consumption mode.
 - When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".

(2) Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

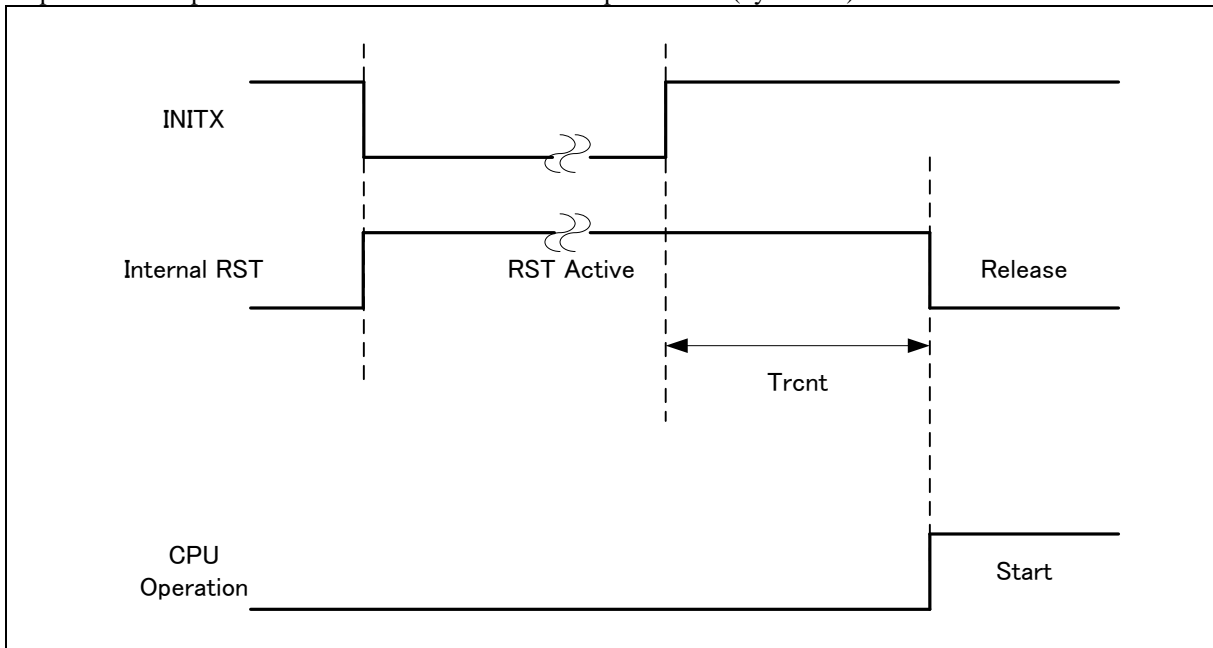
- Return Count Time

($V_{CC} = 2.7V$ to $5.5V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

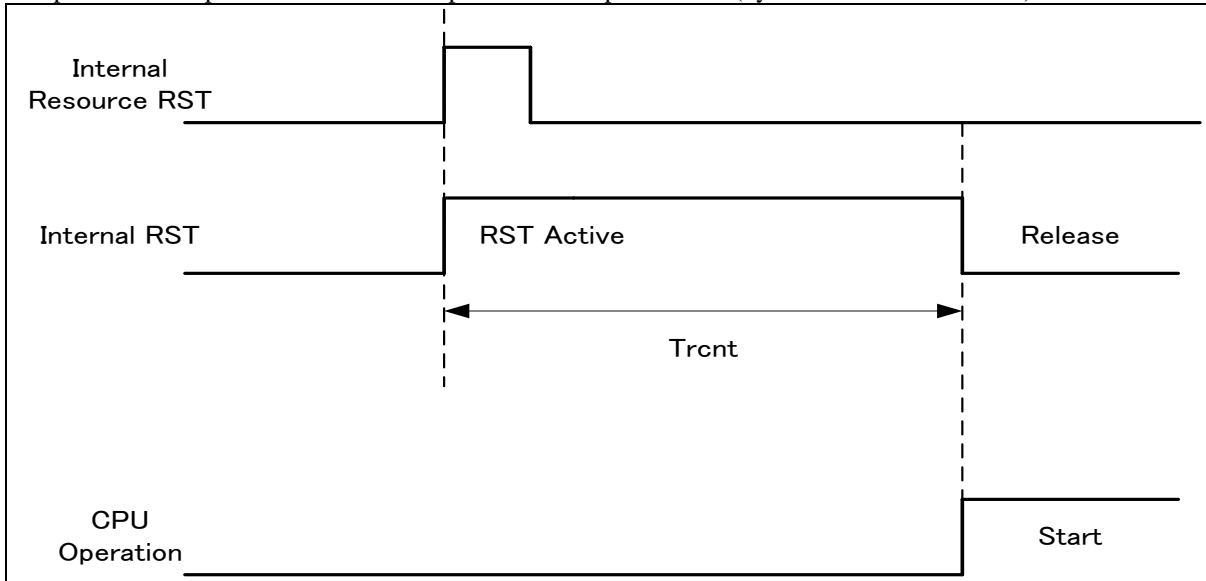
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	82	181	μs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		82	181	μs	
Low-speed CR TIMER mode		431	1003	μs	
Sub TIMER mode		431	1003	μs	
STOP mode		431	1003	μs	

*: The maximum value depends on the accuracy of built-in CR.

- Operation example of return from Low-Power consumption mode (by INITX)



- Operation example of return from low power consumption mode (by internal resource reset*)

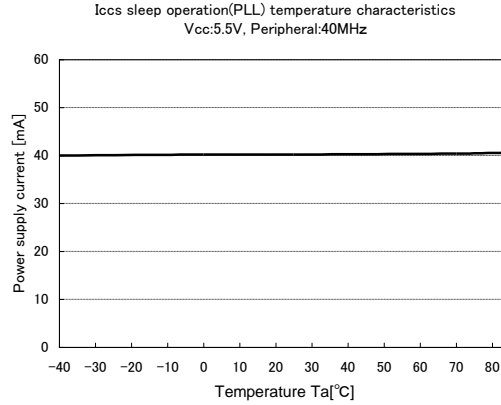
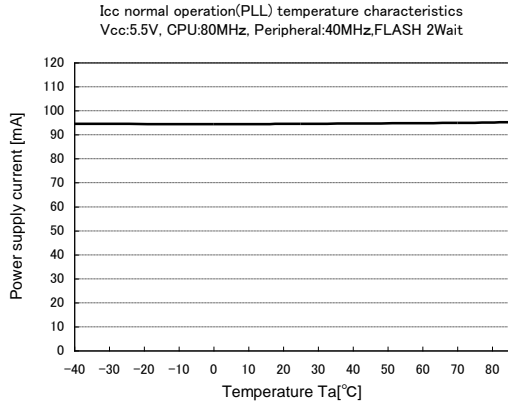


*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

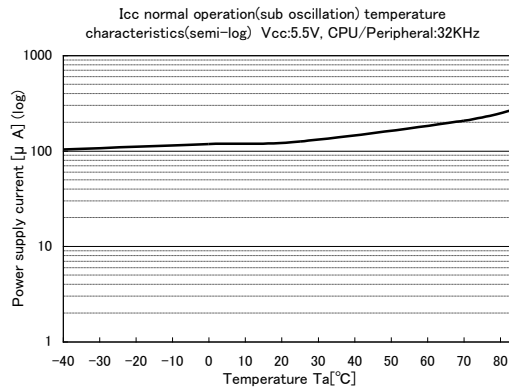
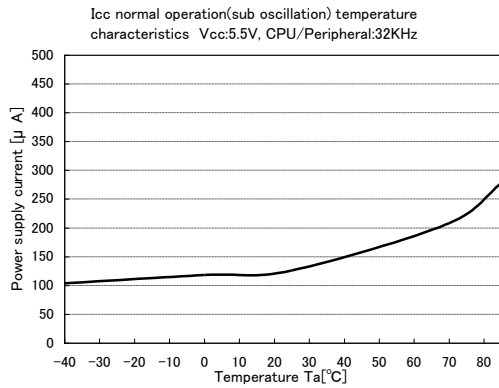
- Notes:
- The return factor is different in each Low-Power consumption modes. See "CHAPTER 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family PERIPHERAL MANUAL.
 - When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".
 - The time during the power-on reset/low-voltage detection reset is excluded. See "(6) Power-on Reset Timing in 4. AC Characteristics in ■ELECTRICAL CHARACTERISTICS" for the detail on the time during the power-on reset/low -voltage detection reset.
 - When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
 - The internal resource reset means the watchdog reset and the CSV reset.

■ EXAMPLE OF CHARACTERISTIC

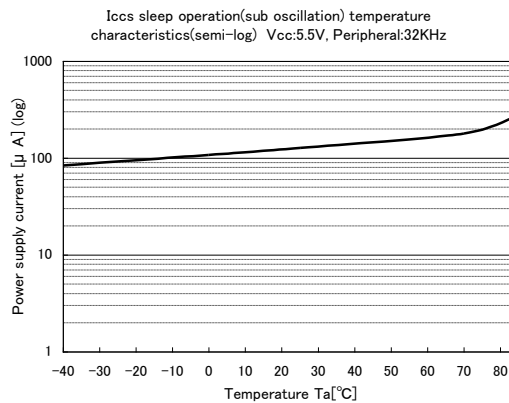
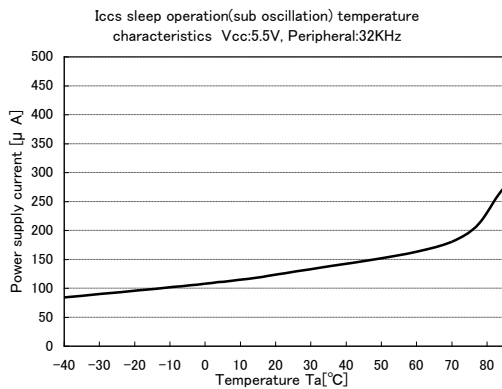
Power supply current (PLL run mode, PLL sleep mode)



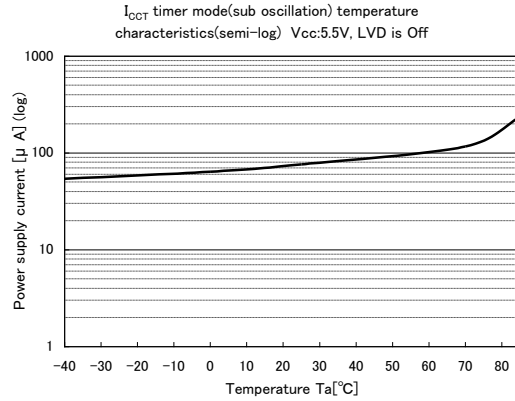
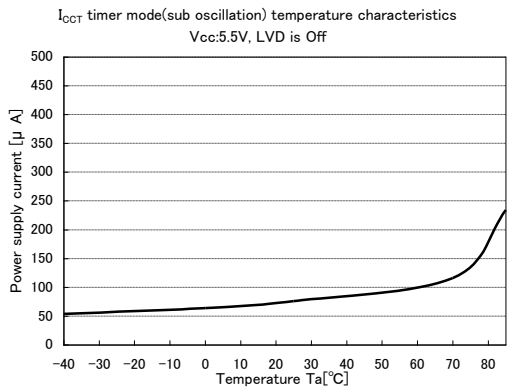
Power supply current (Sub run mode)



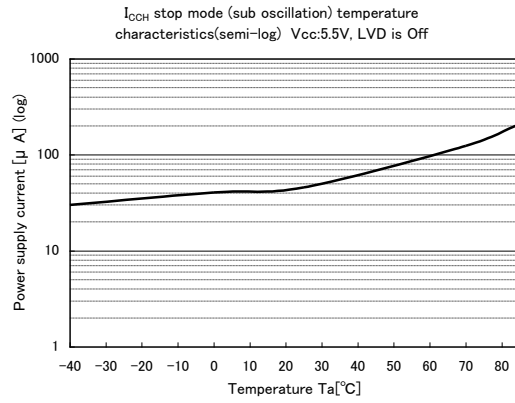
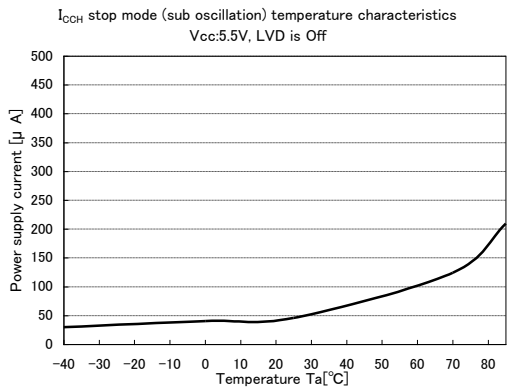
Power supply current (Sub sleep mode)



Power supply current (Sub timer mode)



Power supply current (Stop mode)



■ ORDERING INFORMATION

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9BF404NAPMC-G-JNE2	256Kbyte	32Kbyte	Plastic • LQFP (0.5mm pitch), 100-pin (FPT-100P-M23)	Tray
MB9BF405NAPMC-G-JNE2	384Kbyte	48Kbyte		
MB9BF406NAPMC-G-JNE2	512Kbyte	64Kbyte		
MB9BF404RAPMC-G-JNE2	256Kbyte	32Kbyte	Plastic • LQFP (0.5mm pitch), 120-pin (FPT-120P-M37)	
MB9BF405RAPMC-G-JNE2	384Kbyte	48Kbyte		
MB9BF406RAPMC-G-JNE2	512Kbyte	64Kbyte		
MB9BF404NABGL-G-YE1	256Kbyte	32Kbyte	Plastic • PFBGA (0.8mm pitch), 112-pin (BGA-112P-M04)	
MB9BF405NABGL-G-YE1	384Kbyte	48Kbyte		
MB9BF406NABGL-G-YE1	512Kbyte	64Kbyte		

■ PACKAGE DIMENSIONS

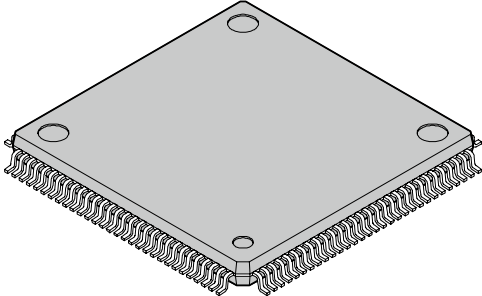
<p>100-pin plastic LQFP</p> <p>(FPT-100P-M23)</p>	Lead pitch	0.50 mm
	Package width x package length	14.00 mm x 14.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65 g

100-pin plastic LQFP (FPT-100P-M23)

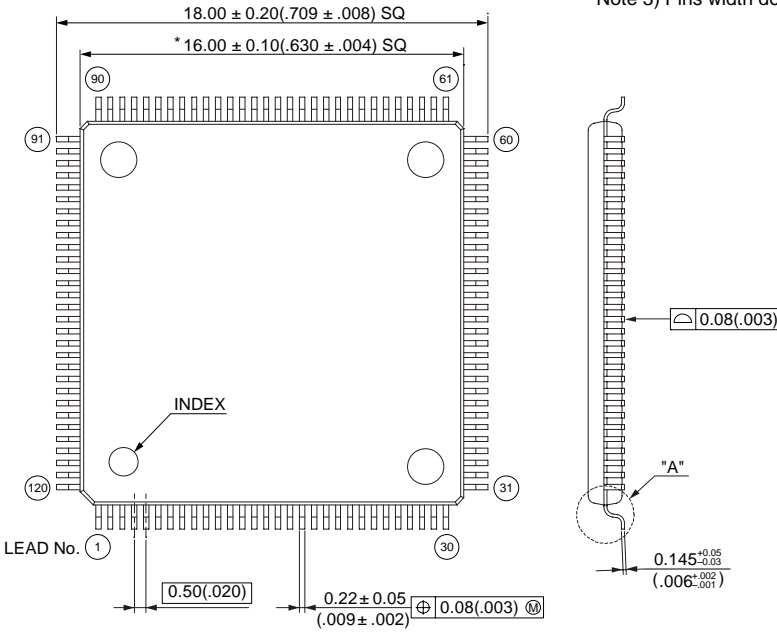
Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.

Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

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<p style="text-align: center;">120-pin plastic LQFP</p>  <p style="text-align: center;">(FPT-120P-M37)</p>	Lead pitch	0.50 mm
	Package width × package length	16.0 mm × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16 × 16-0.50

120-pin plastic LQFP
(FPT-120P-M37)

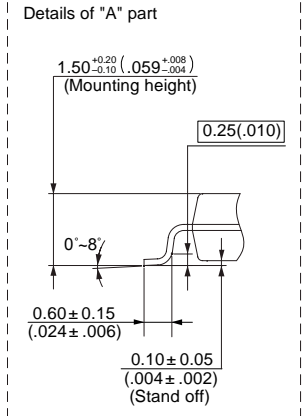


Top view dimensions:
 Overall width: 18.00 ± 0.20 (709 ± .008) SQ
 Pin array width: 16.00 ± 0.10 (630 ± .004) SQ
 Pin pitch: 0.50 (.020)
 Pin width: 0.22 ± 0.05 (.009 ± .002)
 Pin thickness: 0.08 (.003) M

Side view dimensions:
 Mounting height: $1.50^{+0.20}_{-0.10}$ (.059^{+0.08}_{-.004})
 Lead thickness: $0.145^{+0.05}_{-0.03}$ (.006^{.002}_{.001})
 Lead angle: 0°~8°
 Stand off: 0.10 ± 0.05 (.004 ± .002)

Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.

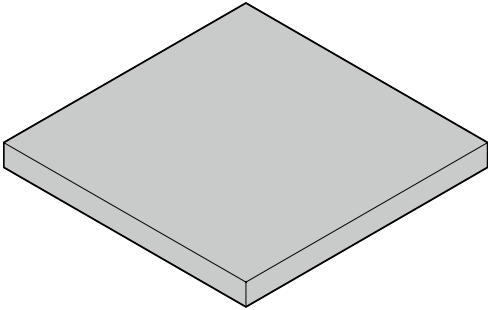
Details of "A" part

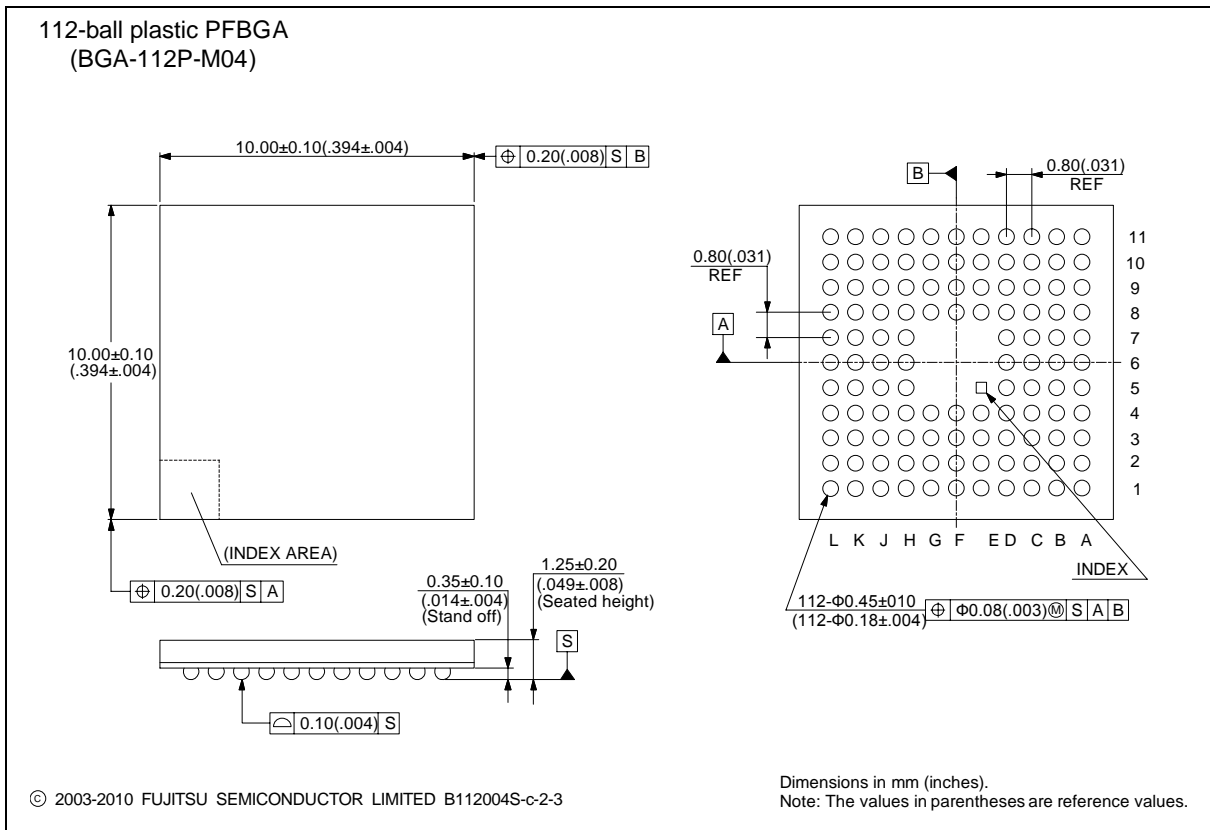


Lead thickness: 0.25 (.010)
 Stand off: 0.10 ± 0.05 (.004 ± .002)

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Dimensions in mm (inches).
 Note: The values in parentheses are reference values

<p>112-ball plastic PFBGA</p>  <p>(BGA-112P-M04)</p>	Ball pitch	0.80 mm
	Package width x package length	10.00 x 10.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Φ 0.45 mm
	Mounting height	1.45 mm Max.
	Weight	0.22 g



MAJOR CHANGES

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
3	<ul style="list-style-type: none"> ■ FEATURES ● External Bus Interface 	Added the description of Maximum area size
8	<ul style="list-style-type: none"> ■ PACKAGES 	Deleted the description of ES
17	<ul style="list-style-type: none"> ■ LIST OF PIN FUNCTIONS · List of pin numbers 	Modified the Pin state type of P4E from I to H
32-35	<ul style="list-style-type: none"> ■ LIST OF PIN FUNCTIONS · List of pin functions 	Added LIN to the description of SOTxx
42	<ul style="list-style-type: none"> ■ I/O CIRCUIT TYPE 	Added the description of I ² C to the type of E and F
42, 43	<ul style="list-style-type: none"> ■ I/O CIRCUIT TYPE 	Added about +B input
48	<ul style="list-style-type: none"> ■ HANDLING DEVICES 	Added "● Stabilizing power supply voltage"
48	<ul style="list-style-type: none"> ■ HANDLING DEVICES ● Crystal oscillator circuit 	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
49	<ul style="list-style-type: none"> ■ HANDLING DEVICES ● C Pin 	Changed the description
50	<ul style="list-style-type: none"> ■ BLOCK DIAGRAM 	Modified the block diagram
50	<ul style="list-style-type: none"> ■ MEMORY SIZE 	Changed to the following description See "● Memory size" in "■ PRODUCT LINEUP" to confirm the memory size.
51	<ul style="list-style-type: none"> ■ MEMORY MAP · Memory map(1) 	Modified the area of "External Device Area"
52	<ul style="list-style-type: none"> ■ MEMORY MAP · Memory map(2) 	Added the summary of Flash memory sector and the note
59, 60	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings 	<ul style="list-style-type: none"> · Added the Clamp maximum current · Added the output current of P80 and P81 · Added about +B input
61	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 2. Recommended Operation Conditions 	<ul style="list-style-type: none"> · Modified the minimum value of Analog reference voltage · Added Smoothing capacitor · Added the note about less than the minimum power supply voltage
62, 63	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current rating 	<ul style="list-style-type: none"> · Changed the table format · Added Main TIMER mode current · Added Flash Memory Current · Moved A/D Converter Current
65	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Main Clock Input Characteristics 	Added Master clock at Internal operating clock frequency
66	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Built-in CR Oscillation Characteristics 	Added Frequency stability time at Built-in high-speed CR
67	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-1)(4-2) Operating Conditions of Main PLL 	<ul style="list-style-type: none"> · Added Main PLL clock frequency · Added the figure of Main PLL connection
68	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (6) Power-on Reset Timing 	<ul style="list-style-type: none"> · Added Time until releasing Power-on reset · Changed the figure of timing
74-81	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) CSIO/UART Timing 	<ul style="list-style-type: none"> · Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
88	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 5. 12bit A/D Converter 	<ul style="list-style-type: none"> · Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AV_{cc} < 4.5V · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
92	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 7. Flash Memory Write/Erase Characteristics 	Change to the erase time of include write time prior to internal erase
93-96	<ul style="list-style-type: none"> ■ ELECTRICAL CHARACTERISTICS 8. Return Time from Low-Power Consumption Mode 	Added Return Time from Low-Power Consumption Mode
99	<ul style="list-style-type: none"> ■ ORDERING INFORMATION 	Change to full part number
100	<ul style="list-style-type: none"> ■ PACKAGE DIMENSIONS 	Deleted FPT-100P-M20 and FPT-120P-M21

Colophon

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