Dual Synchronous Buck Controller with 5V/3.3V 100mA LDOs for Notebook System Power

General Description

The uP1590 is a dual synchronous buck controller with 5V/3.3V 100mA LDOs for notebook system power supply solution.

The uP1590 supports high efficiency, fast transient response and provides a combined POK signal. The ultrasonic mode maintains the switching frequency above audio frequency, which eliminates noise in audio applications. The proprietary RCOT™ technology provides fast transient response and high noise immunity.

The uP1590 has internal soft-start to control the inrush current. Other features include over current protection, over/under voltage protection, power-up sequencing, POK output, and thermal shutdown. The uP1590 is available in the space saving package WQFN3x3-20L, specified from -40°C to 85°C.

Applications

- **Notebook and Subnotebook System Power Supplies**
- **3-4 Cell Li-Ion Battery-Power Devices**
- **Dual Output Supplies for DSP, Memory, Logic and Microprocessor**

Features

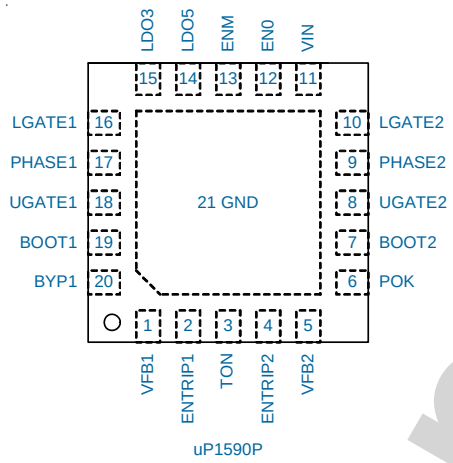
- **Wide Input Voltage Range: 5.5V to 26V**
- **Two Synchronous Buck Controllers**
  - **Dual Fixed 5V/3.3V Outputs or Adjustable from 2V to 5.5V**
  - **Selectable DEM and USM in Light Load (uP1590P)**
  - **Internal Soft-Start and Soft-Discharge**
  - **RCOT™ (Robust Constant On-Time) Control Architecture**
  - **4500ppm/°C $R_{DS(ON)}$ Current Sensing**
- **100mA 5V/3.3V LDO with Switches**
- **Secondary FB Input Maintains Charge Pump Voltage (uP1590Q Only)**
- **Power OK Indicator**
- **OVP/UVP/OCP/OTP**
- **WQFN3x3-20L**
- **RoHS Compliant and Halogen Free**

Ordering Information

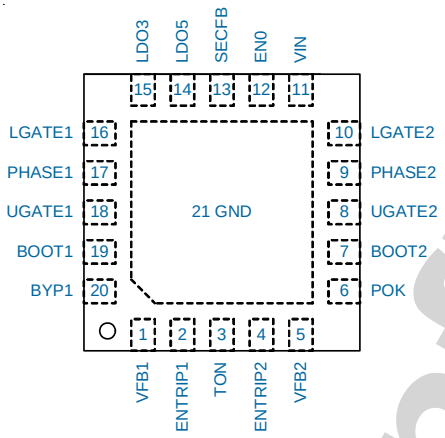
Order Number	Package Type	Top Marking	Operation Mode	Remark
uP1590PQKF	WQFN3x3-20L	uP1590P	Selectable by ENM Pin	Pin 13: ENM
uP1590QQKF		uP1590Q	DEM	Pin 13: SECFB
uP1590RQKF		uP1590R	USM	Pin 13: TP

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

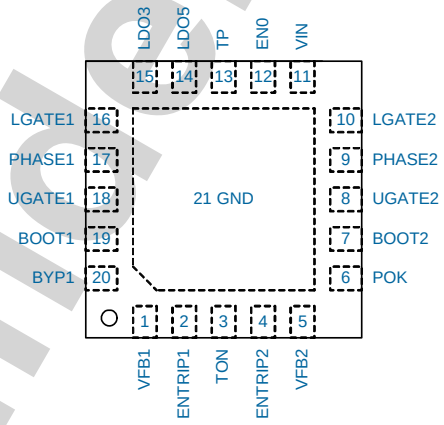
Pin Configuration



uP1590P

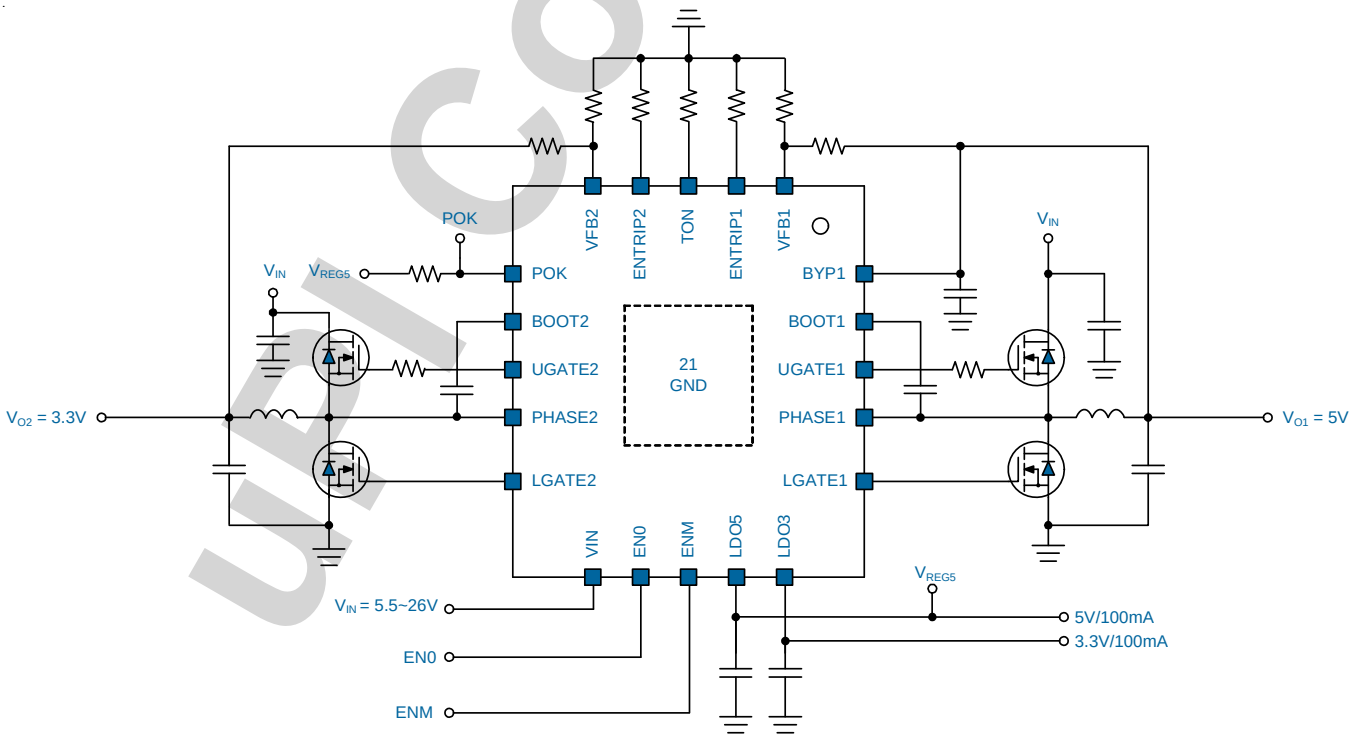


uP1590Q



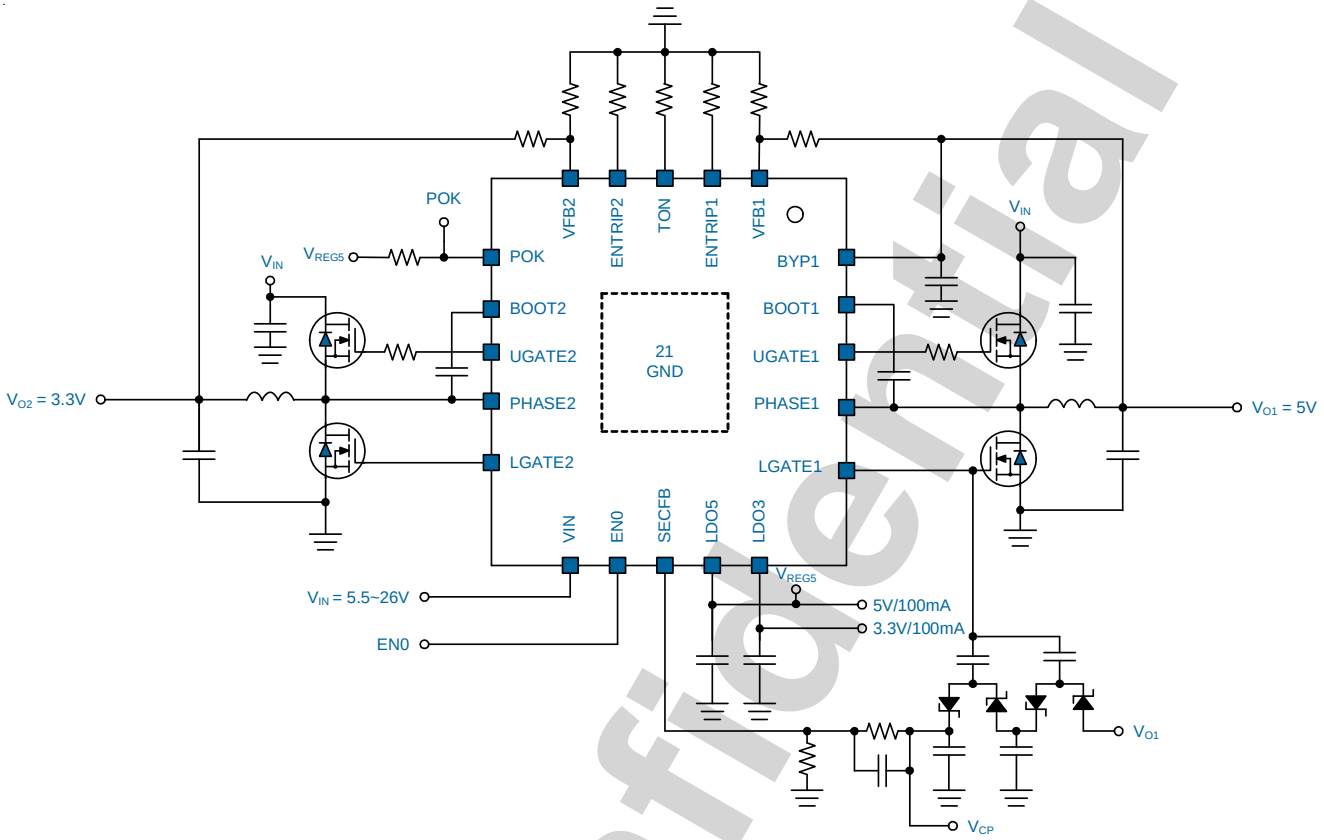
uP1590R

Typical Application Circuit

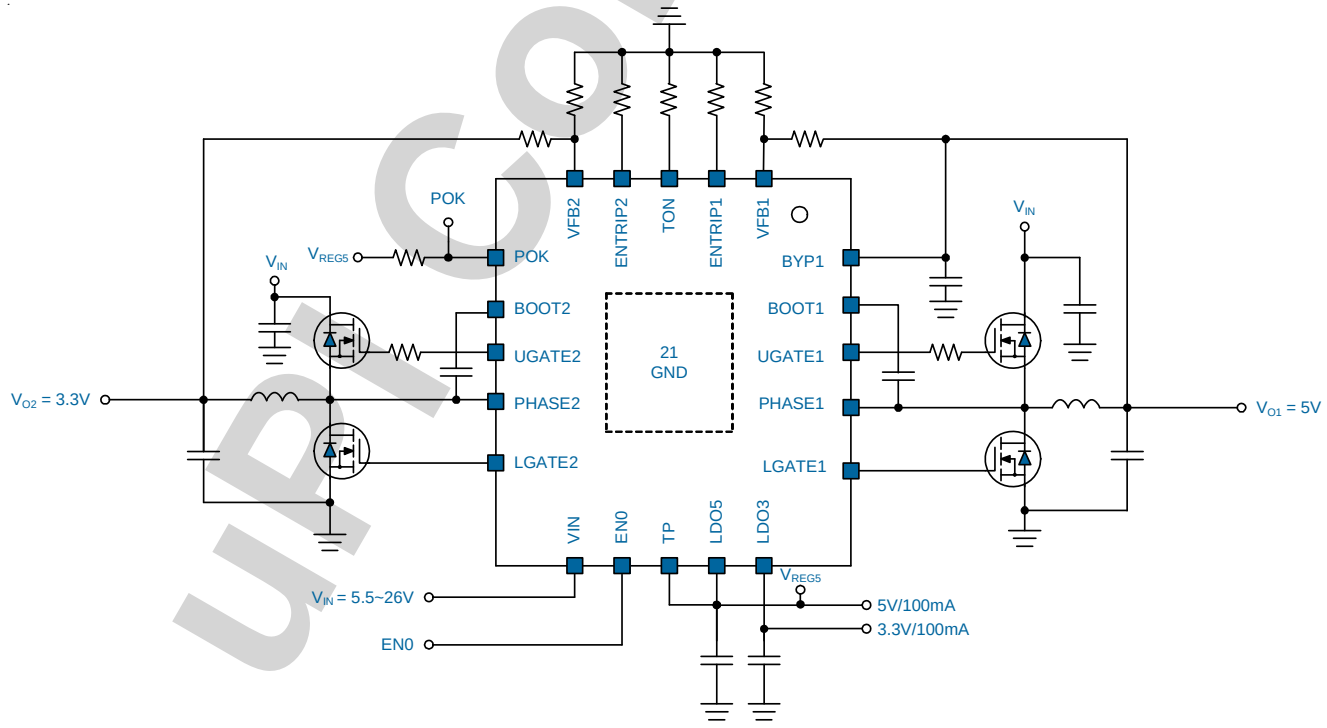


uP1590P

Typical Application Circuit

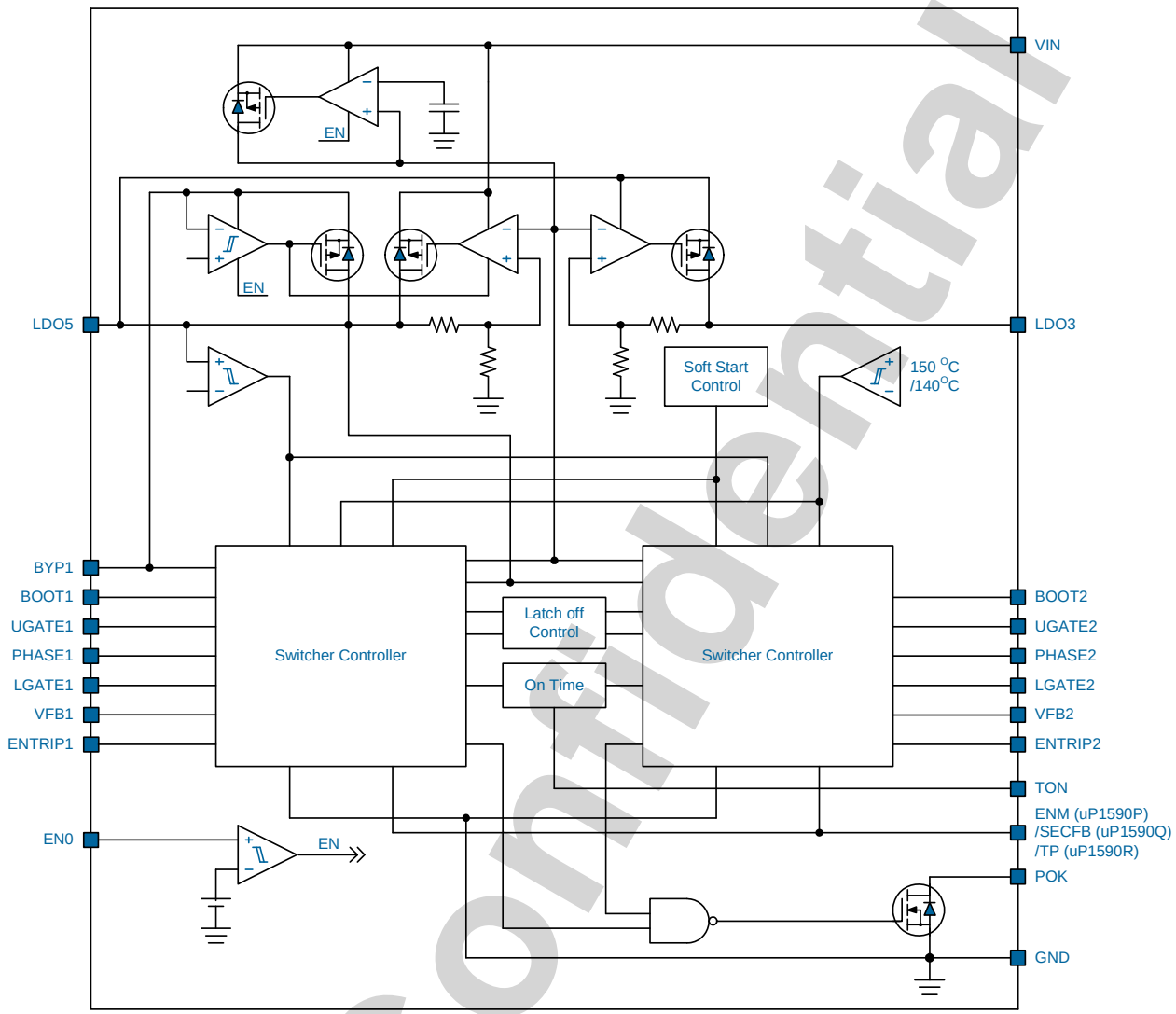


uP1590Q



uP1590R

Functional Block Diagram



Functional Pin Description

No.	Name	Pin Function
1	VFB1	**Buck 1 Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
2	ENTRIP1	**Buck 1 Enable and OCP Setting.** Connect a resistor from this pin to GND to set threshold for synchronous buck 1 $R_{DS(ON)}$ OCP. Leave this pin floating or connect this pin to VCC to shutdown Buck 1.
3	TON	**On-Time Setting Pin.** Connect a resistor from this pin to GND to set the on-time for the upper MOSFETs.
4	ENTRIP2	**Buck 2 Enable and OCP Setting.** Connect a resistor from this pin to GND to set threshold for synchronous buck 2 $R_{DS(ON)}$ OCP. Leave this pin floating or connect this pin to VCC to shutdown Buck 2.
5	VFB2	**Buck 2 Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
6	POK	**Power OK Indication.** POK is the open-drain architecture that indicates the output voltage is ready or not. This pin is set to high impedance when the output voltage is within regulation and the soft-start circuit has terminated. POK is pulled low immediately when either output is in soft-start, standby, shutdown or protection.
7	BOOT2	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver of Buck 2.** The bootstrap capacitor provides the charge to turn on the upper MOSFET. Connect this bootstrap capacitor between BOOT2 pin and the PHASE2 pin to form a bootstrap circuit.
8	UGATE2	**Upper MOSFET Gate Driver Output of Buck 2.** This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the gate of upper MOSFET.
9	PHASE2	**Switch Node of Buck 2.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.
10	LGATE2	**Lower MOSFET Gate Driver Output of Buck 2.** This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. Connect this pin to the gate of lower MOSFET.
11	VIN	**Supply Input.** This pin is the input of the internal 5V and 3.3V LDO regulators. Connect VIN to the battery or AC adapter output.
12	EN0	**LDO Enable.** VIN: enable both LDOs and ready to turn on switcher channels. GND: disable all circuit.
13	ENM (uP1590P)	**Buckx Enable Input and Operation Mode Selection Pin.** Ultrasonic Mode: Connect this pin to LDO5. Diode Emulation Mode: Connect this pin to LDO3. Enable: Pull high this pin above 0.8V.
	SECFB (uP1590Q)	**Change Pump Feedback Pin.** The SECFB is used to monitor the optional external charge pump. Connect a resistive divider from the change pump output to GND to detect the output. If SECFB drops below its feedback threshold, an ultrasonic pulse occurs to refresh the charge pump driven by LGATE1 or LGATE2.
	TP (uP1590R)	**Test Pin.** Must tie this pin to LDO5.
14	LDO5	**Output of Internal 5V LDO.** The LDO5 is capable of sourcing 100mA output current for external loads. Bypass this pin with a minimum 4.7uF.

Functional Pin Description

No.	Name	Pin Function
15	LDO3	**Output of Internal 3.3V LDO.** The LDO3 is capable of sourcing 100mA output current for external loads. Bypass this pin with a minimum 4.7uF.
16	LGATE1	**Lower MOSFET Gate Driver Output of Buck 1.** This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. Connect this pin to the gate of lower MOSFET.
17	PHASE1	**Switch Node of Buck 1.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.
18	UGATE1	**Upper MOSFET Gate Driver Output of Buck 1.** This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the gate of upper MOSFET.
19	BOOT1	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver of Buck 1.** The bootstrap capacitor provides the charge to turn on the upper MOSFET. Connect this bootstrap capacitor between BOOT1 pin and the PHASE1 pin to form a bootstrap circuit.
20	BYP1	**Switch Over Source Voltage Input for LDO5.** Connect to VOUT1 to supply voltage for LDO5 when switch over.
Exposed Pad		**Ground.** The exposed pad dominates heat conduction path and should be well soldered to PCB for optimal thermal performance.

Functional Description

The uP1590 implements an unique RCOT™ control topology for both synchronous Bucks. The uP1590 does not require the external compensator. The RCOT™ supports extremely low ESR output capacitors and makes the design easier and robust.

Enable and Soft Start

EN0 is the control pin of LDO5 and LDO3 regulators. Connect this pin to GND disables two regulators. Connect this pin to 3.3V or 5V will turn the two regulators on to standby mode. Two SMPSs become ready to enable at this standby mode. When ENM (uP1590P) is higher than 0.8V, then both SMPSs begin to start up. Connect this pin to GND disables two SMPSs. Two SMPSs operate in diode emulation mode when ENM pin voltage is set between 2.3V to 3.6V. If V_{ENM} is between 1.2V to 1.8V or between 4.5V to 5V, two SMPSs operate in ultrasonic mode. The uP1590 has an internal 2ms output voltage soft-start for each channel. Connect ENTRIPx pin to VCC or leave it floating disables the SMPSx. For normal operation, connect a resistor from ENTRIPx pin to GND sets over current limit (OCL) threshold. The recommended OCL threshold is from 0.5V to 2.7V. Higher or lower threshold beside this recommended range could active the OCL but accuracy may be affected and not preferred. After POR, the SMPSs automatically start up if the ENTRIPx is valid (released from the disable state).

Table 1. Enable State

EN0	ENM	ENTRIP1	ENTRIP2	LDO3	LDO5	CH1	CH2
GND	X	X	X	Off	Off	Off	Off
VIN	GND	X	X	On	On	Off	Off
VIN	High	Off	Off	On	On	Off	Off
VIN	High	On	Off	On	On	On	Off
VIN	High	Off	On	On	On	Off	On
VIN	High	On	On	On	On	On	On

Table 2. Operation Mode Selection

Recommend ENM Pin Voltage	Operation Mode
GND	Shutdown
1.2V to 1.8V	Ultrasonic Mode
2.3V to 3.6V	Diode Emulation Mode
4.5V to 5V	Ultrasonic Mode

On Time Control and PWM Frequency

The uP1590 runs with pseudo fixed frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is controlled proportional to V_{OUT}/V_{IN} so that the duty ratio will be kept as technically with the same cycle time.

The one-shot timer is programmed by a resister R_{TON} connected from TON pin to GND pin as:

$$T_{ON\_5V} = 4.45\times10^{-2}\times\frac{V_{OUT}}{V_{IN}}\times R_{TON} + 20ns$$

$$T_{ON\_3.3V} = 3.5\times10^{-2}\times\frac{V_{OUT}}{V_{IN}}\times R_{TON} + 10ns$$

The on-time is determined by V_{IN} and V_{OUT} and is kept fairy constant over a wide input and output voltage range at steady state.

Operation Modes (Only for uP1590P)

uP1590P supports two operation modes: Diode Emulation and Ultrasonic mode. The operation mode is selected by ENM pin.

Diode Emulation Mode (ENM = LDO3)

In *Diode Emulation Mode*, the uP1590 automatically switches over to DEM at light load. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The lower MOSFET is turned off if detected the negative inductor current. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next ON cycle. The frequency is reduced smoothly and hence the power losses is reduced at light load.

Functional Description

Ultrasonic Mode (ENM = LDO5)

Ultrasonic mode (USM) is a technique that keeps the switching frequency above audible frequencies while maintaining best of the high conversion efficiency. When the ultrasonic mode is selected, USM control circuit monitors both MOSFETs and forces to change into the ON state if both MOSFETs are off for more than 32us. USM control circuit detects the over voltage condition and begins to modulate the on-time to keep the output voltage regulated.

LDO3/LDO5 Linear Regulators

The uP1590 has two sets of 100mA linear regulators which outputs 5V and 3.3V. The LDO5 provides the main power supply for the circuitry of the device and provides the current for gate drivers.The LDO3 is intended mainly for 3.3V supply for the notebook system during standby mode.

LDO5 Switcher

When VOUT1 finishes soft-start and the voltage higher than its switchover threshold, an internal switch connects BYP1 to LDO5 and shuts down the LDO5 simultaneously. When ENTRIP1 goes low, the LDO5 is activated immediately and then internal switch will be off. It decreases the power dissipation from battery.

Output Discharge Control

When ENTRIPx is high, the uP1590 discharges outputs using internal MOSFET. The current capability of these MOSFETs is limited to discharge slowly.

Power OK Indicator

The uP1590 has one POK output indicator. A pull-up resistor is needed for the open-drain output. The POK is actively held low in soft-start, standby, shutdown and protection. It is released when both VO1 and VO2 voltage above than 90% of their nominal regulation voltage and switchover has finished.

Over Current Protection

The uP1590 has cycle-by-cycle over current limiting control. The inductor current is monitored during the off state and the controller keeps the off state when the inductor current is larger than the over current trip level.

In order to provide both good accuracy and cost effective solution, uP1590 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. ENTRIPx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. ENTRIPx terminal sources I_{TRIP} current, which is 10 uA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as below. Note that the V_{TRIP} is limited up to about 270 mV(Typ.) internally.

$$V_{TRIP}(mV) = \frac{R_{TRIP}(k\Omega) \times I_{TRIP}(uA)}{10} = I_{OCP} \times R_{DS(ON)}$$

$$R_{TRIP}(k\Omega) = \frac{I_{OCP} \times R_{DS(on)} \times 10}{I_{TRIP}(uA)}$$

The voltage between GND pin and PHASEx pin monitors the inductor current so that PHASEx pin should be connected to the drain terminal of the lower MOSFET properly. I_{TRIP} has 4500 ppm/°C temperature slope to compensate the temperature dependency of the lower $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the proper current sensing device, i.e. the source terminal of the lower MOSFET.

When the comparison is done during the off state, V_{TRIP} sets valley level of the inductor current. Therefore, the load current at over current threshold, I_{LIM}, can be calculated as follows:

$$I_{LIM} = \frac{V_{TRIP}}{R_{DSON}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{TRIP}}{R_{DSON}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over current condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it ends up with crossing the under voltage protection threshold and shutdown both channels.

Over/Under Voltage Protection

The uP1590 monitors the feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 112% target voltage, the OVP circuit latches as the upper MOS off and the lower MOS on. When the feedback voltage becomes lower than 58% target voltage, the UVP occurs and after 10us UVP delay, the uP1590 latches off both MOSFETs, and shuts off both drivers of another channel. This function is enabled after 5ms following ENTRIPx has become high.

UVLO Protection

uP1590 has LDO5 under voltage lock out protection (UVLO). When the LDO5 voltage is lower than UVLO threshold voltage, both SMPS are turned off. This is a non-latch protection.

Over Temperature Protection

The uP1590 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP1590 is turned off including LDOs. This is a non-latch protection.

Charge Pump (SECFB)

As shown in the Figure1, the external charge pump is driven by LGATEx. The total charge pump voltage, V_{CP}, is :

$$V_{CP} = VOx + 2 \times V_{LGATEx} - 4 \times V_D$$

where V_{LGATEx} is the peak voltage of the LGATEx driver which is equal to LDO5 and V_D is the forward voltage dropped across the Schottky diode.

The SECFB pin in the uP1590Q is used to monitor the charge pump via a resistive voltage divider to generate DC voltage and the clock driver uses VOx as its power supply. In the event where SECFB drops below its feedback threshold, an ultrasonic pulse will occur to refresh the charge pump driven by LGATEx. If there an overload on the charge pump in which SECFB can not reach more than its feedback threshold, the controller will enter ultrasonic mode. Special care should be taken to ensure that enough normal ripple voltage is present on each cycle to prevent charge pump shutdown.

The robustness of the charge pump can be increased by reducing the charge pump decoupling capacitor and placing a small ceramic capacitor, C_P (47pF to 220pF), in parallel with the upper leg of the SECFB resistor feedback network, R_{CP1}, as shown below in Figure 1

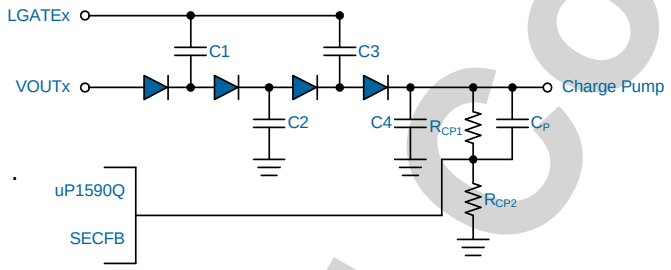


Figure 1.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VIN ---------- -0.3V to +30V
BOOTx to PHASEx ---------- -0.3V to +6V
PHASEx to GND
- DC ---------- -0.3V to +30V
- < 200ns ---------- -5V to +38V

UGATEx to PHASEx
- DC ---------- -0.3V to +6V
- <200ns ---------- -5V to +7V

LGATEx to GND
- DC ---------- -0.3V to +6V
- < 200ns ---------- -2V to +7V

Other Pins to GND ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature Range(Soldering 10sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WQFN3x3 - 20L θ_{JA} ---------- 68°C/W
- WQFN3x3 - 20L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ TA = 25°C
- WQFN3x3 - 20L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, VIN ---------- 5.5V to 26V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN}=12V, V_{EN0}=5V, V_{VFB1}=V_{VFB2}=2V, $V_{ENTRIP1}$=$V_{ENTRIP2}$=1V, V_{BYP1}=5V, I_{LDO5}=I_{LDO3}=0A, T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
VIN Power On Reset	V_{POR}	Rising	--	5.1	5.5	V
		Falling	3.5	--	4.5	
VIN Supply Current	I_{VIN}	No Load, V_{VFB1} = V_{VFB2} = 2.05V	--	0.55	1.10	mA
VIN Standby Current	$I_{VINSTBY}$	No Load, $V_{ENTRIP1}$ = $V_{ENTRIP2}$ = 5V	--	250	350	uA
VIN Shutdown Current	I_{SD}	No Load, V_{EN0} = 0V	--	20	40	uA
Output						
VFB Regulation Voltage	V_{VFBx}	CCM Operation	--	2	--	V
		PSM Operation	1.98	2.006	2.03	
Output Voltage Range			2	--	5.5	V
VOUTx Discharge Current	I_{Dischg}	$V_{ENTRIPx}$ = 5V, V_{OUTx} = 0.5V	--	3	--	mA
SECFB Voltage	V_{SECFB}	uP1590Q only	1.92	2	2.08	V
On Time						
On-Time	T_{ON}	V_{IN} = 20V, R_{TON} = 56kΩ, V_{PHASE1} = 5V	--	640	--	ns
		V_{IN} = 20V, R_{TON} = 56kΩ, V_{PHASE2} = 3V	--	330	--	
Minimum On-Time	T_{ONMIN}		--	80	--	ns
Minimum Off-Time	T_{OFFMIN}		--	--	400	ns
Frequency	F_{SW1}	V_{OUT1} Operation Frequency	200	--	400	kHz
	F_{SW2}	V_{OUT2} Operation Frequency	233	--	466	
USM Frequency	F_{USM}	SMPS operating in USM	25	--	--	kHz
Soft-Start						
Internal SS Time	T_{SS}	Internal soft-start	--	2	--	ms
LDO5 Output						
LDO5 Output Voltage	V_{LDO5}	V_{BYP1} = 0V, I_{LDO5} < 100mA	4.8	5	5.2	V
		V_{BYP1} = 0V, I_{LDO5} < 100mA, 6.5V < VIN < 26V	4.75	5	5.25	
		V_{BYP1} = 0V, I_{LDO5} < 50mA, 5.5V < V_{IN} < 26V	4.75	5	5.25	
LDO5 Output Current	I_{LDO5}	V_{BYP1} = 0V, V_{LDO5} = 4.5V	--	225	--	mA
Switch Over Threshold	V_{TH5VSW}	Turn On	4.53	4.66	4.79	V
		Hysteresis	--	0.25	--	V
5V Switch Over Ron	R_{5VSW}	V_{OUT1} = 5V, I_{LDO5} = 100mA	--	1.5	3	Ω

Electrical Characteristics

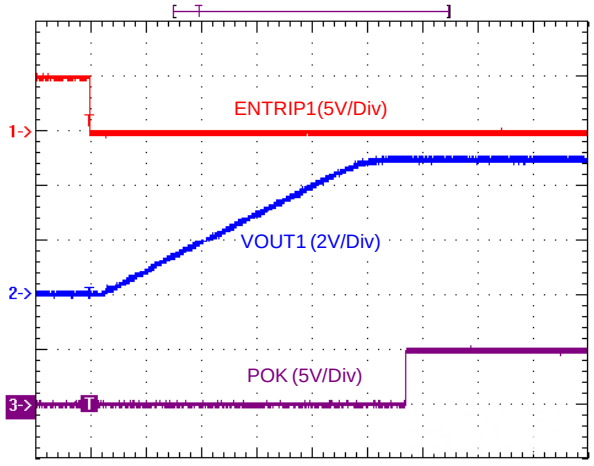
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
LDO3 Output						
LDO3 Output Voltage	V_{LDO3}	V_{BYP1} = 0V, I_{LDO3} < 100mA	3.2	3.3	3.46	V
		V_{BYP1} = 0V, I_{LDO3} < 100mA, 6.5V < V_{IN} < 26V	3.13	3.3	3.5	
		V_{BYP1} = 0V, I_{LDO3} < 50mA, 5.5V < V_{IN} < 26V	3.13	3.3	3.5	
LDO5 Output Current	I_{LDO3}	V_{BYP1} = 0V, V_{LDO3} = 3V	--	150	--	mA
Power OK						
POK Threshold	V_{THPOK}	Rising Threshold	-14	-10	-6	%
		Hysteresis	--	5	--	
POK Propagation Delay	T_{POK}		--	5	--	us
POK Leakage Current	I_{LK_POK}		--	--	1	uA
POK Output Low Voltage	V_{POK_L}		--	--	0.4	V
SECFB POK Threshold	V_{SEC_THPOK}	SECFB with respect to 2V	40	50	60	%
POK Delay	T_{POKDEL}	Delay time from 90% of VFB to POK go high	--	500	--	us
Logic Threshold and Setting Conditions						
EN0 Voltage	V_{EN0}	Rising edge threshold	1.2	1.6	2	V
		Falling edge threshold	0.9	0.95	1	
ENTRIPx Input Voltage	$V_{ENTRIPx}$	OCL Setting Range	0.5	--	2.7	V
		Clear fault high level / SMPSx off level	4.5	--	--	
ENM Threshold Voltage (uP1590P)	V_{ENM}	Shutdown	--	--	0.8	V
		DEM	2.3	--	3.6	
		USM	4.5	--	--	
Protection: Current Sense						
ENTRIPx Source Current	$I_{ENTRIPx}$	$V_{ENTRIPx}$ = 0.9V	9.4	10	10.6	uA
ENTRIPx Current Temp. Coefficient	T_{CIEN}	On the basis of 25°C	--	4500	--	ppm/-°C
OCP Copm. Offset	V_{OCLoff}	$V_{ENTRIPx}$ / 10	- 8	0	8	mV
OCL Threshold	V_{OCL}	$V_{ENTRIPx}$ = 2V	180	200	225	mV
Zero Current Threshold	V_{ZC}	GND - PHASEx, V_{VFBx} = 2.1V	--	3	--	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection: UVP & OVP						
OVP Trip Threshold	V_{OVP}	OVP detect	108	112	116	%
OVP Prop. Delay	T_{OVPDEL}		--	5	--	us
UVP Trip Threshold	V_{UVP}	UVP detect	53	58	63	%
	V_{SEC_UVP}	uP1590Q/R	0.8	--	1.2	V
UVP Prop. Delay	T_{UVPDEL}		--	10	--	us
UVP Enable Delay	T_{UVPEN}	From ENTRIPx enable	--	5	--	ms
UVLO						
LDO5 UVLO Threshold	V_{UVLDO5}	Rising edge	--	4.35	4.5	V
		Falling edge	3.9	4.05	4.2	
LDO3 UVLO Threshold	V_{UVLDO3}		--	2.2	--	V
Thermal Shutdown						
Thermal SDN Threshold	T_{SDN}	Shutdown temperature	--	150	--	°C
		Hysteresis	--	10	--	
Internal Booststrap Switch						
Internal Boost Charging Switch On-Resistor	R_{BOOTx}	LDO5 to BOOTx, I_{BOOTx} = 10mA	--	--	90	Ω
Output Drivers						
UGATE Resistance	R_{UGATEx}	Source, $V_{BOOTx-UGATEx}$ = 100mV	--	5	8	Ω
		Sink, $V_{UGATEx-PHASEx}$ = 100mV	--	2	4	
LGATE Resistance	R_{LGATEx}	Source, $V_{LDO5-LGATEx}$ = 100mV	--	5	8	Ω
		Sink, V_{LGATEx} = 100mV	--	1.5	3	
Dead Time	T_D	UGATEx < 1V to LGATEx > 1V	--	30	--	ns
		LGATEx < 1V to UGATEx > 1V	--	40	--	

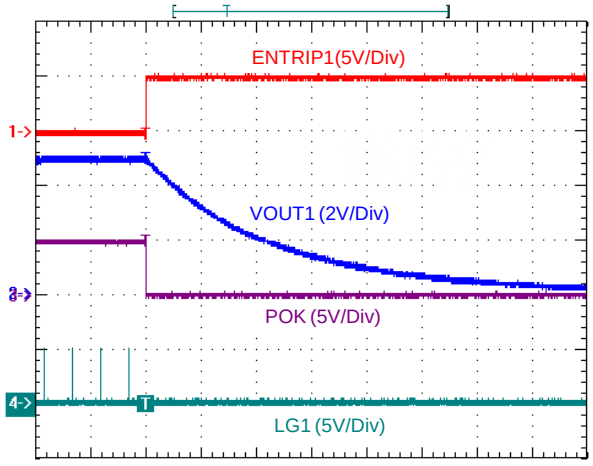
Typical Operation Characteristics

Power On from ENTRIP1



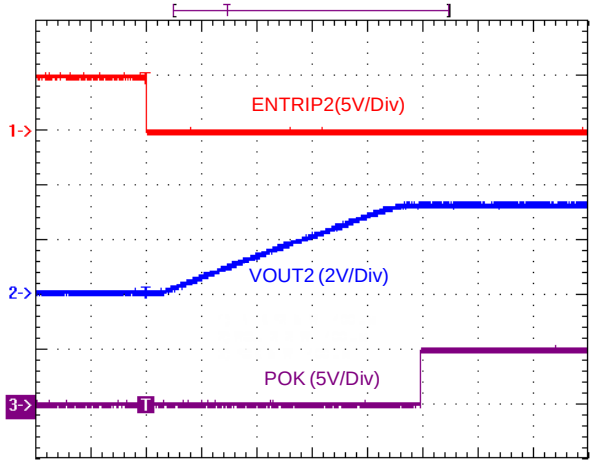
400us/Div
I_{OUT1} = 0A

Power Off from ENTRIP1



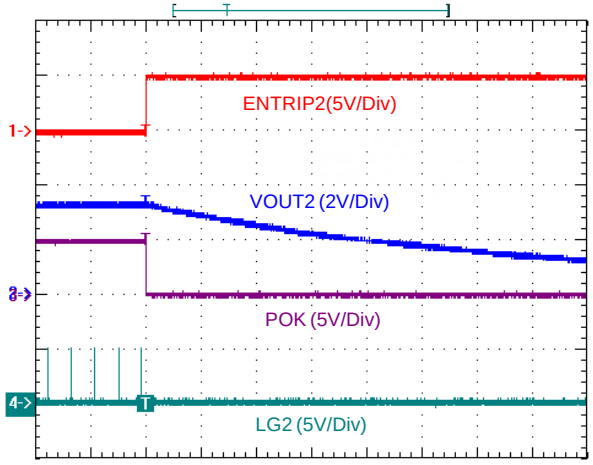
10ms/Div
I_{OUT1} = 0A

Power On from ENTRIP2



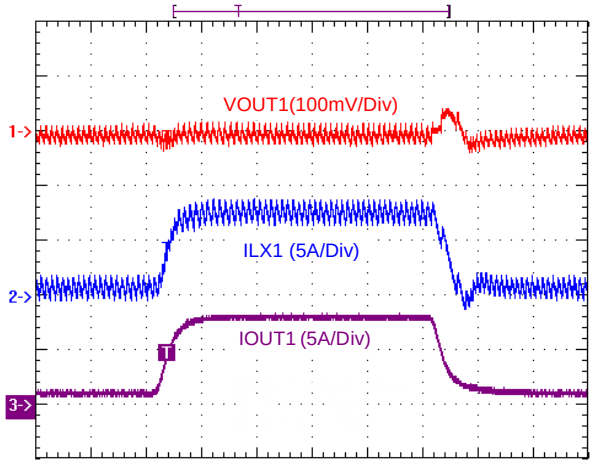
400us/Div
I_{OUT2} = 0A

Power Off from ENTRIP2



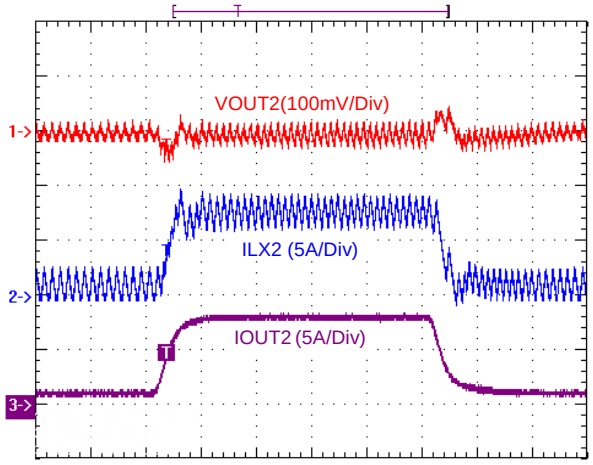
10ms/Div
I_{OUT2} = 0A

VO1 Load Transient Response



20us/Div
V_{IN} = 12V, I_{OUT1} = 1A to 8A

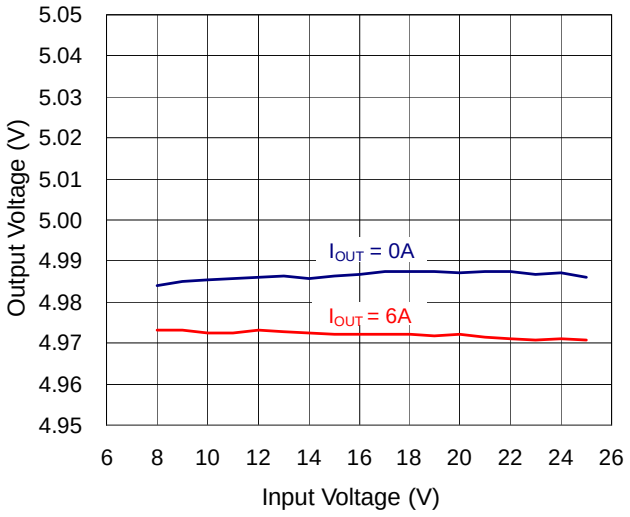
VO2 Load Transient Response



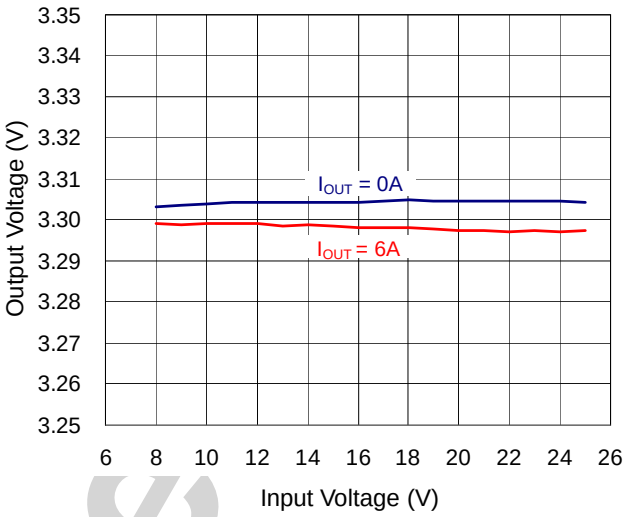
20us/Div
V_{IN} = 12V, I_{OUT2} = 1A to 8A

Typical Operation Characteristics

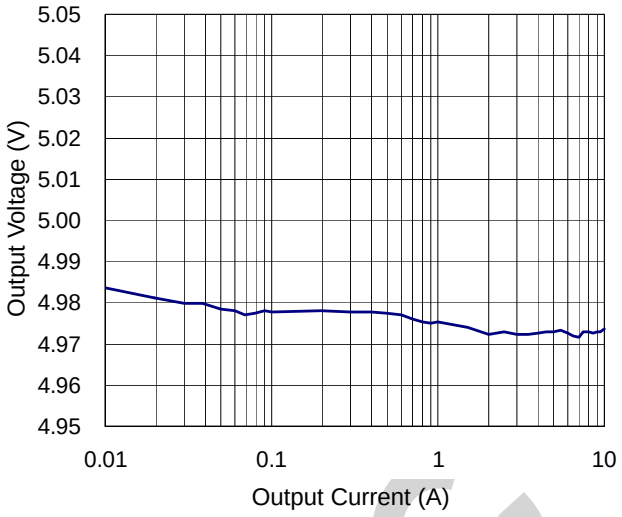
VO1 Line Regulation



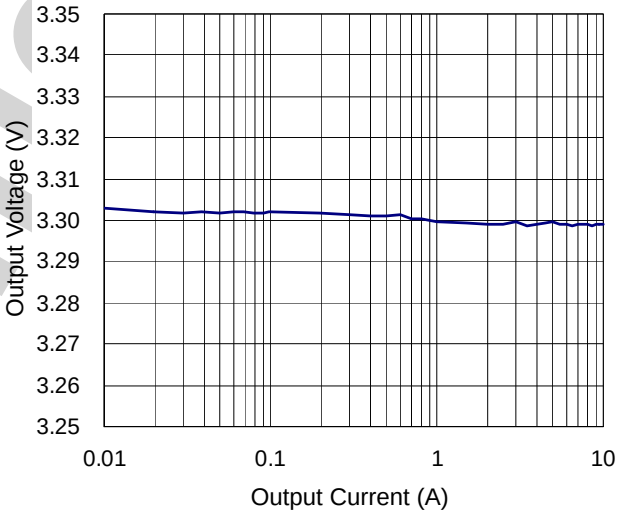
VO2 Line Regulation



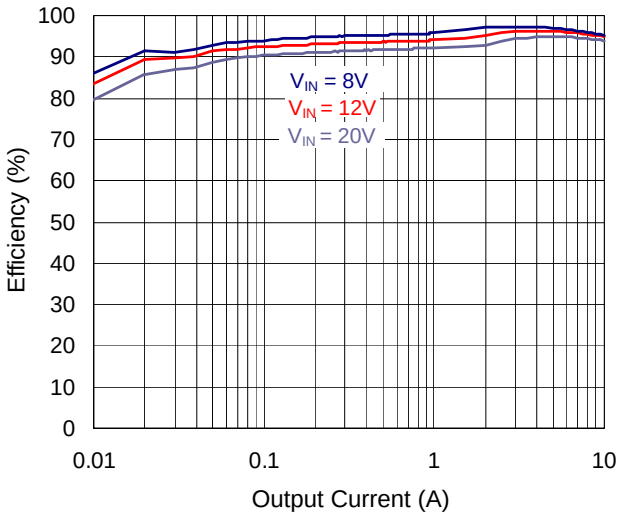
VO1 Load Regulation



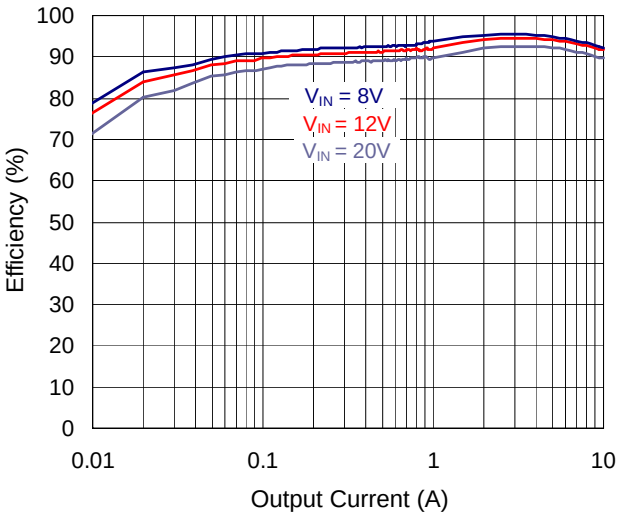
VO2 Load Regulation



VO1 Efficiency



VO2 Efficiency



Application Information

Output Inductor Selection

The inductor plays an important role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the dc resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, the inductor covers a significant proportion of the board space, so its size is also important. Low profile inductors can save board space especially when the height has a limitation. However, low DCR and low profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which translates into the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, the switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown in the following equation:

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUTx})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak to peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice because powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

The calculation above shall serve as a general reference. To further improve the transient response, the output inductance can be reduced even further. This needs to be considered along with the selection of the output capacitor.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from below equations:

$$V_{SOAR} = \frac{\Delta I_{LOAD}{}^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

where V_{SOAR} are the allowable amount of undershoot voltage and overshoot voltage in the load transient, V_{P-P} is the output ripple voltage.

MOSFET Selection

The majority of power loss in the step-down power converter is the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the upper MOSFET is small. Therefore, the switching loss of the upper MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the lower MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter.

To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the MOSFET driver capability and the budget.

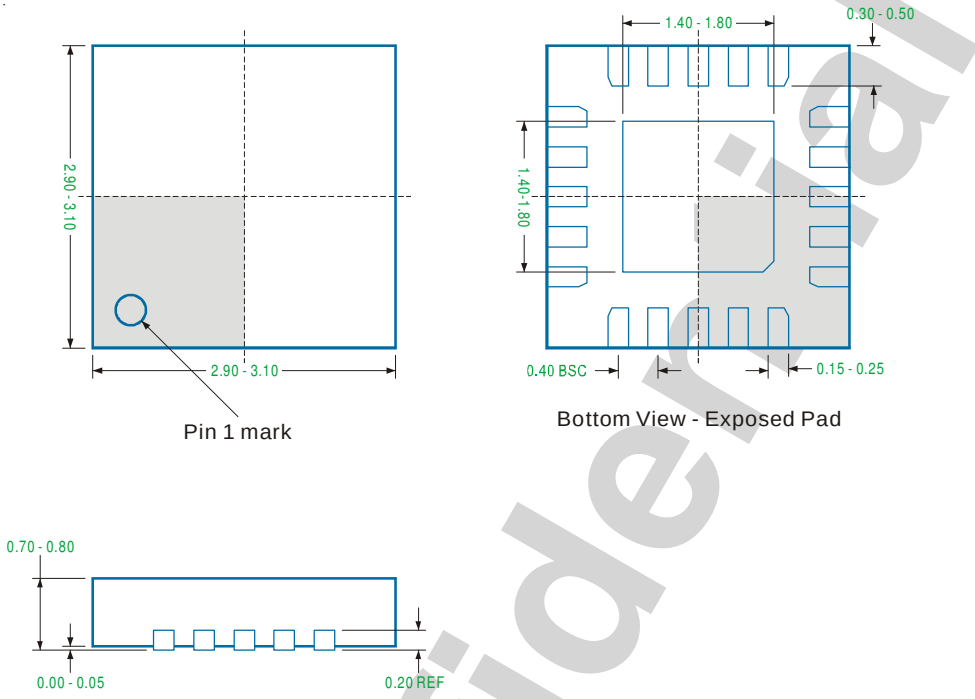
Layout Considerations

Layout is very important in high frequency switching converter designs, the PCB could radiate excessive noise and contribute to the converter instability with improper layout. Certain points must be considered before starting a layout.

- Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the upper or the lower MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VFBx, GND, ENTRIPx and POK should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place the ground terminals of VIN capacitor(s), VOUTx capacitor(s), and source of lower MOSFETs as close as possible. The PCB trace defined as PHASEx node, which connects to source of upper MOSFET, drain of lower MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Package Information

WQFN3x3-20L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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