



RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 63 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1880 MHz.

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQA} = 800$ mA, $V_{GSB} = 0.9$ V, $P_{out} = 63$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

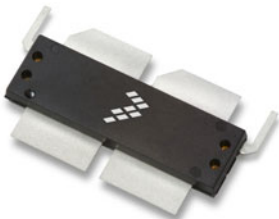
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1805 MHz	17.5	48.7	7.6	-37.5
1840 MHz	17.6	48.3	7.7	-38.9
1880 MHz	17.4	48.2	7.7	-38.5

Features

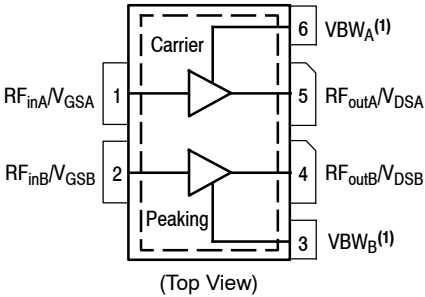
- Advanced high performance in-package Doherty
- High thermal conductivity packaging technology for reduced thermal resistance
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

AFT18H357-24NR6

**1805–1880 MHz, 63 W AVG., 28 V
AIRFAST RF POWER LDMOS
TRANSISTOR**



**OM-1230-4L2L
PLASTIC**



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

- Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 75°C, 63 W Avg., W-CDMA, 28 Vdc, $I_{DQA} = 800$ mA, $V_{GSB} = 0.7$ Vdc, 1840 MHz	$R_{\theta JC}$	0.23	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics (4)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μAdc

On Characteristics - Side A (4)

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 140$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DD} = 28$ Vdc, $I_{DA} = 800$ mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1.4$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

On Characteristics - Side B (4)

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 240$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 2.4$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to [AN1955](#), Thermal Measurement Methodology of RF Power Amplifiers. Go to <http://www.freescale.com/rf> and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 800\text{ mA}$, $V_{GSB} = 0.9\text{ V}$, $P_{out} = 63\text{ W Avg.}$, $f = 1805\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	16.2	17.5	19.2	dB
Drain Efficiency	η_D	42.0	48.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.9	7.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.5	-30.0	dBc

Load Mismatch ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $I_{DQA} = 800\text{ mA}$, $V_{GSB} = 0.9\text{ V}$, $f = 1840\text{ MHz}$, 100 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

VSWR 10:1 at 32 Vdc, 339 W Pulsed CW Output Power (3 dB Input Overdrive from 190 W Pulsed CW Rated Power)	No Device Degradation
---	-----------------------

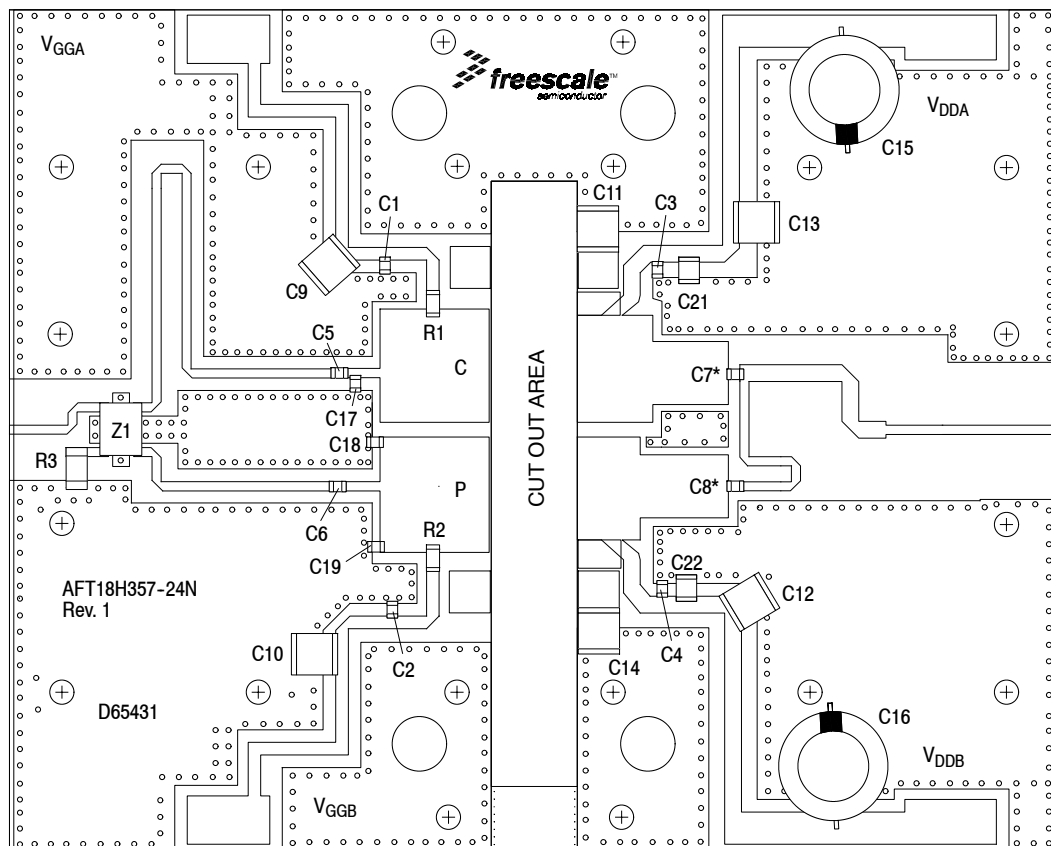
Typical Performance ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 800\text{ mA}$, $V_{GSB} = 0.9\text{ Vdc}$, 1805–1880 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	200	—	W
P_{out} @ 3 dB Compression Point ⁽³⁾	P3dB	—	316	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz bandwidth)	Φ	—	-16	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	60	—	MHz
Gain Flatness in 75 MHz Bandwidth @ $P_{out} = 63\text{ W Avg.}$	G_F	—	0.3	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.004	—	dB/°C
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	$\Delta P1dB$	—	0.008	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
AFT18H357-24NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C7 and C8 are mounted vertically.
Note: C20 component not used.

Figure 2. AFT18H357-24NR6 Test Circuit Component Layout

Table 7. AFT18H357-24NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	20 pF Chip Capacitors	ATC600F200JT250XT	ATC
C5, C6	12 pF Chip Capacitors	ATC600F120JT250XT	ATC
C7	6.2 pF Chip Capacitor	ATC600F6R2JT250XT	ATC
C8	6.8 pF Chip Capacitor	ATC600F6R8JT250XT	ATC
C9, C10, C11, C12, C13, C14	10 μ F Chip Capacitors	C5750X7R1H106M230KB	TDK
C15, C16	220 μ F, 100 V Electrolytic Capacitors	EEV-FK2A221M	Panasonic-ECG
C17	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
C18	1 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
C19	1.2 pF Chip Capacitor	ATC600F1R2BT250XT	ATC
C21, C22	2.2 μ F Chip Capacitors	C3225X7R2A225K230AB	TDK
R1, R2	2.2 Ω , 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω , 4 W Chip Resistor	CW12010T0050GBK	ATC
Z1	1700–2000 MHz Band, 90°, 5 dB Hybrid Coupler	X3C19P1-05S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D65431	MTL

TYPICAL CHARACTERISTICS — 1805–1880 MHz

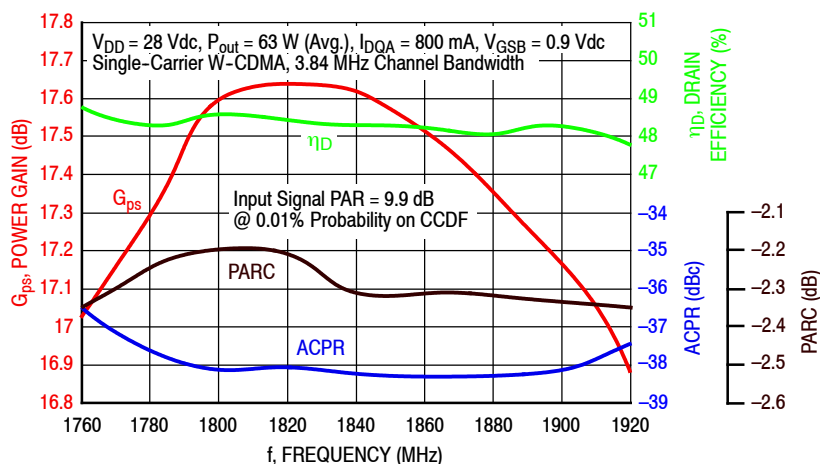


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 63$ Watts Avg.

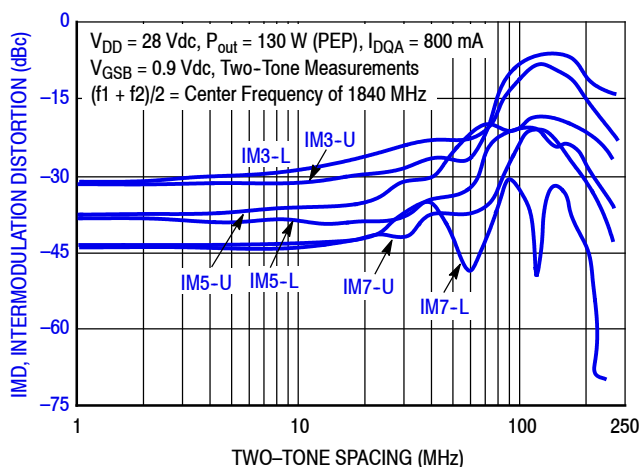


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

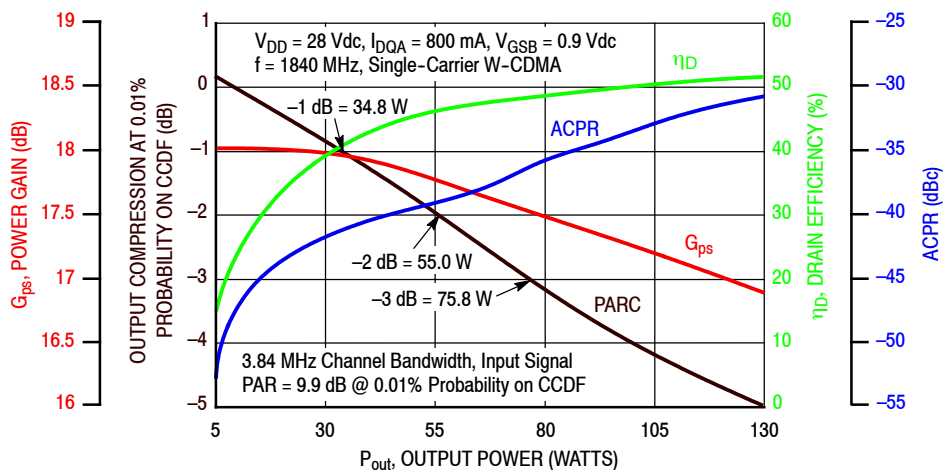


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

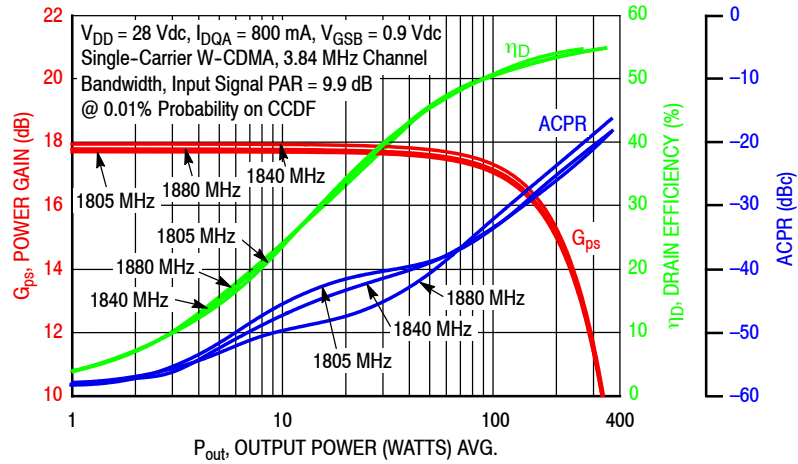


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

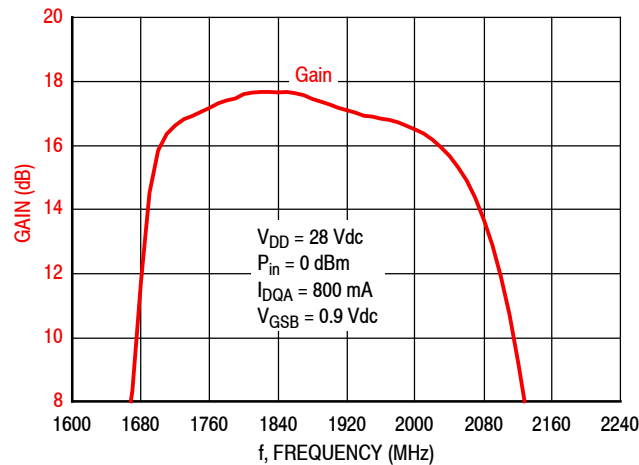


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 818 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.25 – j3.37	1.01 + j3.46	1.37 – j3.14	19.2	51.6	145	56.5	–10
1840	1.53 – j3.73	1.22 + j3.66	1.35 – j3.34	18.9	51.6	146	55.3	–10
1880	1.82 – j4.02	1.55 + j3.98	1.32 – j3.25	19.1	51.5	142	55.4	–11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.25 – j3.37	0.95 + j3.58	1.34 – j3.29	17.0	52.4	173	57.9	–14
1840	1.53 – j3.73	1.13 + j3.82	1.32 – j3.39	16.8	52.4	175	57.1	–15
1880	1.82 – j4.02	1.51 + j4.18	1.35 – j3.58	16.7	52.3	170	55.6	–16

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 818 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.25 – j3.37	1.00 + j3.59	2.78 – j2.07	21.6	49.9	97	69.1	–15
1840	1.53 – j3.73	1.19 + j3.79	2.61 – j1.97	21.6	49.8	96	68.8	–17
1880	1.82 – j4.02	1.56 + j4.13	2.43 – j1.75	21.8	49.4	87	67.3	–19

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.25 – j3.37	0.91 + j3.67	2.69 – j1.94	19.7	50.5	111	70.0	–23
1840	1.53 – j3.73	1.10 + j3.88	2.51 – j2.05	19.5	50.6	115	69.4	–23
1880	1.82 – j4.02	1.44 + j4.27	2.17 – j2.01	19.5	50.5	111	67.7	–25

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

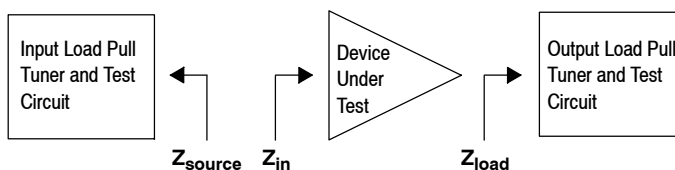
 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $V_{GSB} = 0.8 \text{ Vdc}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	$1.00 - j3.10$	$0.73 + j3.40$	$1.62 - j4.46$	15.0	53.6	230	54.3	-25
1840	$0.92 - j3.29$	$0.81 + j3.51$	$1.73 - j4.64$	15.4	53.6	229	55.1	-30
1880	$1.42 - j3.53$	$1.14 + j3.76$	$1.80 - j4.91$	15.2	53.6	227	54.1	-30

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	$1.00 - j3.10$	$0.73 + j3.48$	$1.73 - j4.60$	13.0	54.2	262	56.4	-32
1840	$0.92 - j3.29$	$0.82 + j3.62$	$1.78 - j4.89$	13.2	54.2	263	55.4	-37
1880	$1.42 - j3.53$	$1.21 + j3.91$	$1.88 - j5.16$	13.1	54.1	259	54.2	-37

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $V_{GSB} = 0.8 \text{ Vdc}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	$1.00 - j3.10$	$0.64 + j3.39$	$3.45 - j2.79$	16.5	52.0	158	67.6	-34
1840	$0.92 - j3.29$	$0.70 + j3.48$	$3.30 - j2.43$	16.8	51.6	145	67.5	-39
1880	$1.42 - j3.53$	$0.95 + j3.69$	$2.79 - j1.51$	16.4	50.4	110	67.9	-44

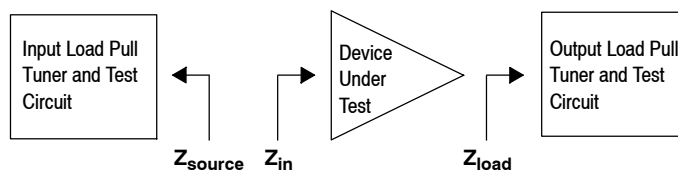
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	$1.00 - j3.10$	$0.68 + j3.48$	$3.74 - j3.07$	14.4	52.5	177	67.7	-43
1840	$0.92 - j3.29$	$0.75 + j3.59$	$3.48 - j2.43$	14.8	52.0	159	67.6	-51
1880	$1.42 - j3.53$	$1.09 + j3.87$	$2.97 - j2.83$	14.6	52.3	172	67.2	-49

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


P1dB - TYPICAL CARRIER LOAD PULL CONTOURS — 1840 MHz

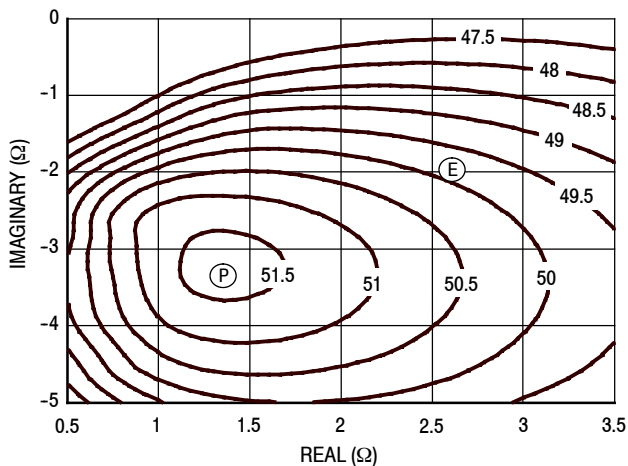


Figure 8. P1dB Load Pull Output Power Contours (dBm)

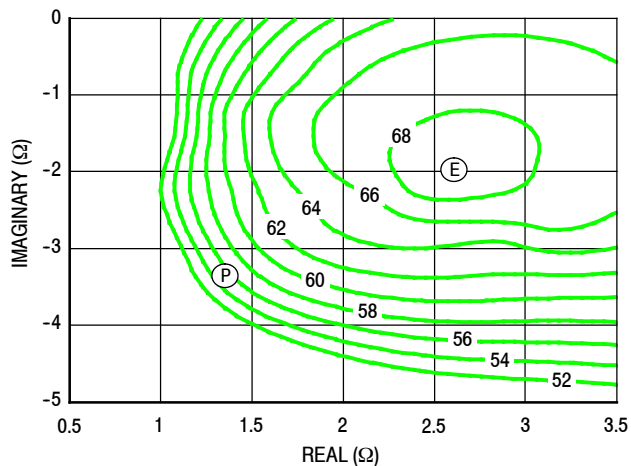


Figure 9. P1dB Load Pull Efficiency Contours (%)

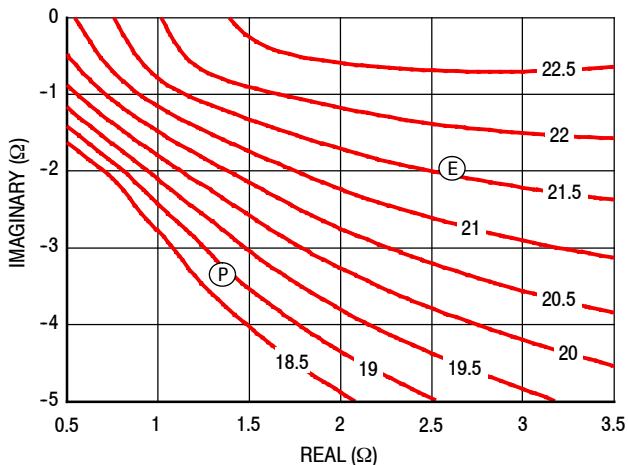


Figure 10. P1dB Load Pull Gain Contours (dB)

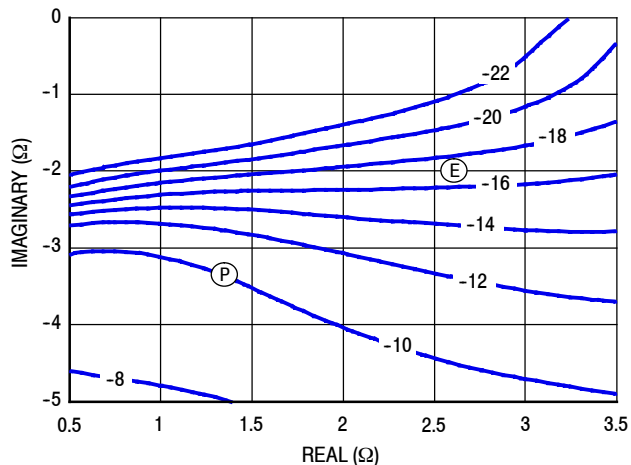


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL CARRIER LOAD PULL CONTOURS — 1840 MHz

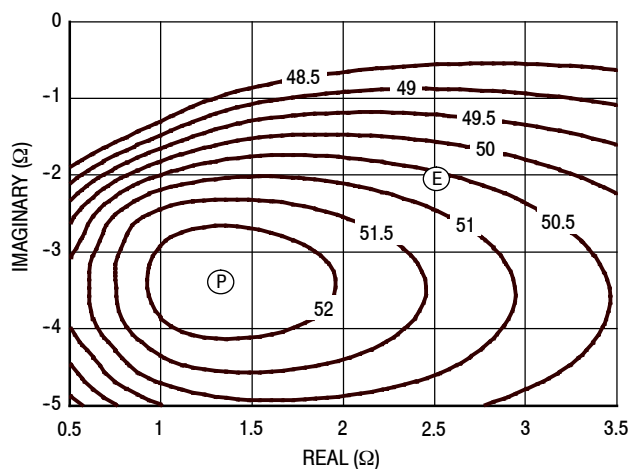


Figure 12. P3dB Load Pull Output Power Contours (dBm)

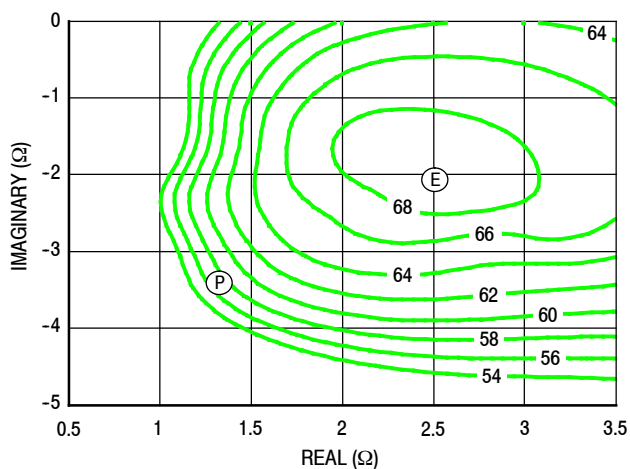


Figure 13. P3dB Load Pull Efficiency Contours (%)

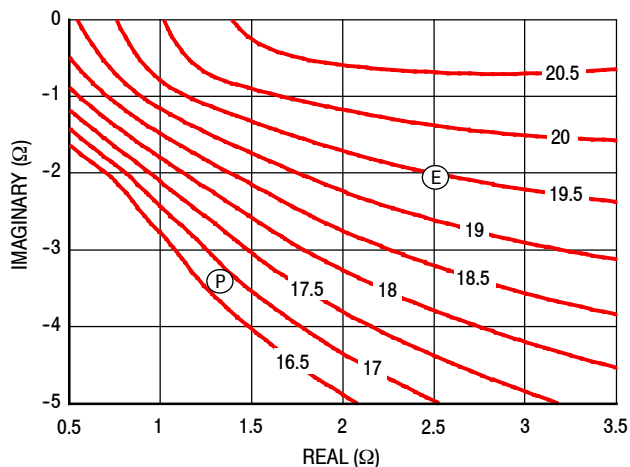


Figure 14. P3dB Load Pull Gain Contours (dB)

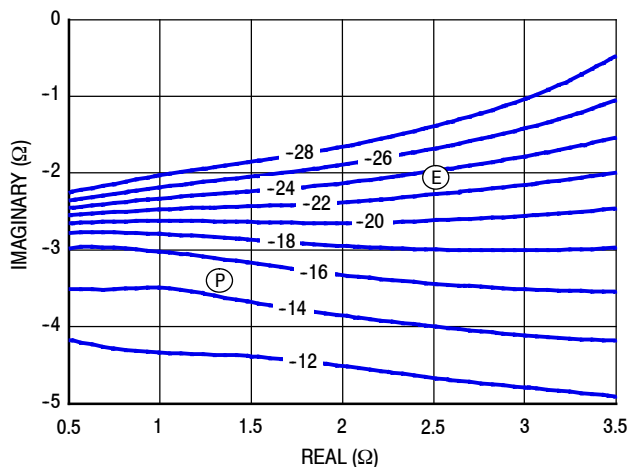


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB - TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz

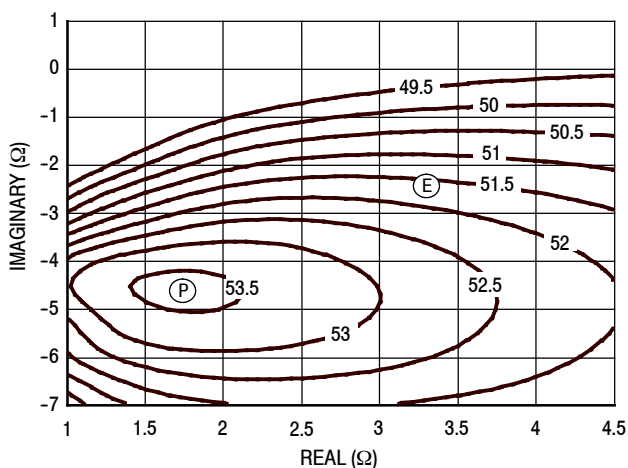


Figure 16. P1dB Load Pull Output Power Contours (dBm)

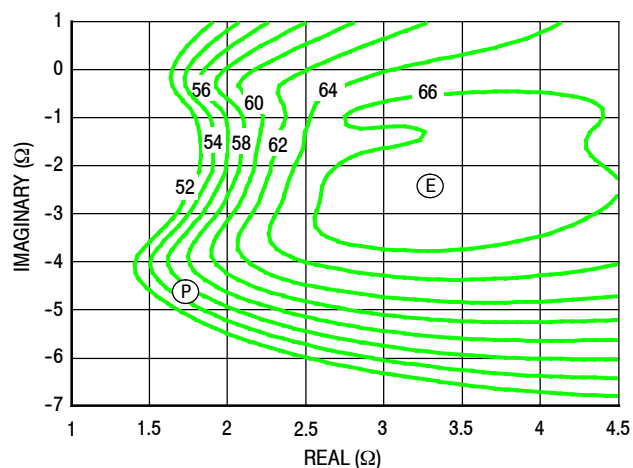


Figure 17. P1dB Load Pull Efficiency Contours (%)

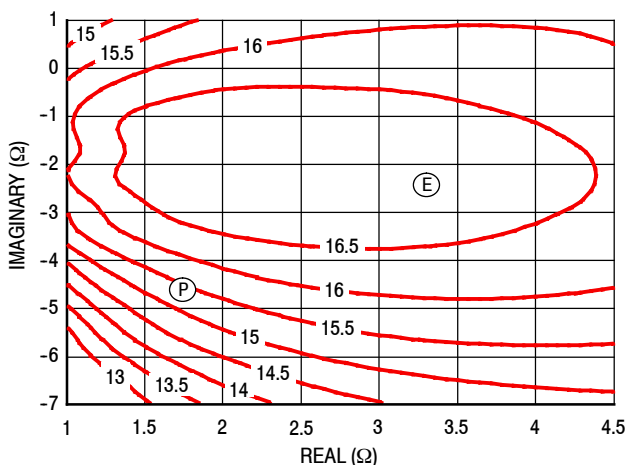


Figure 18. P1dB Load Pull Gain Contours (dB)

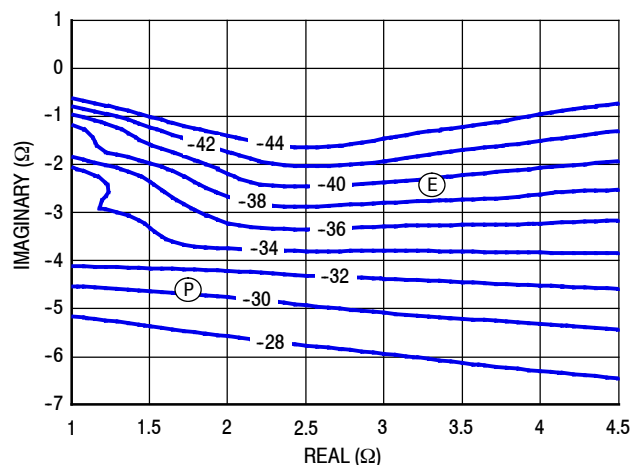


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz

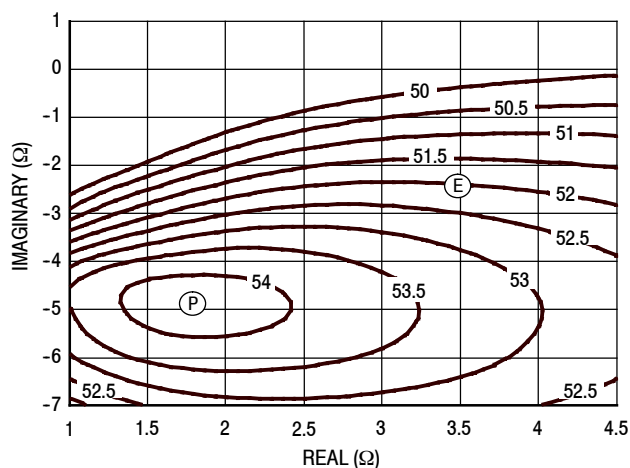


Figure 20. P3dB Load Pull Output Power Contours (dBm)

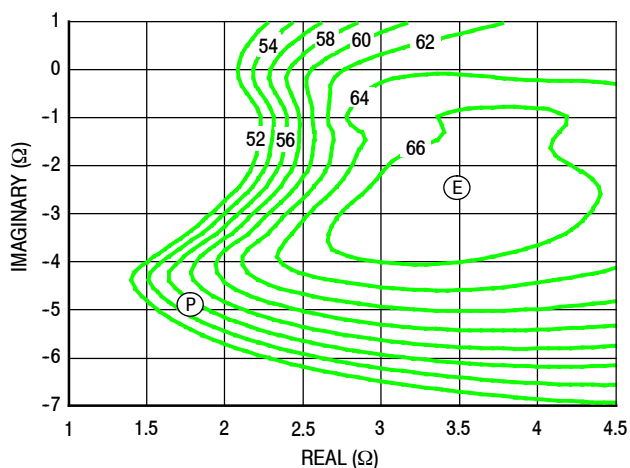


Figure 21. P3dB Load Pull Efficiency Contours (%)

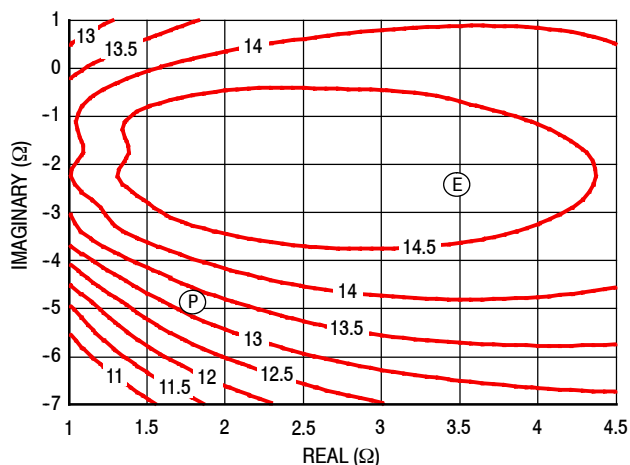


Figure 22. P3dB Load Pull Gain Contours (dB)

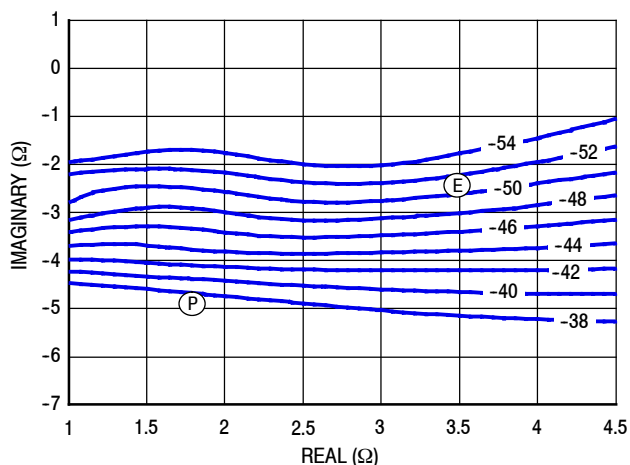
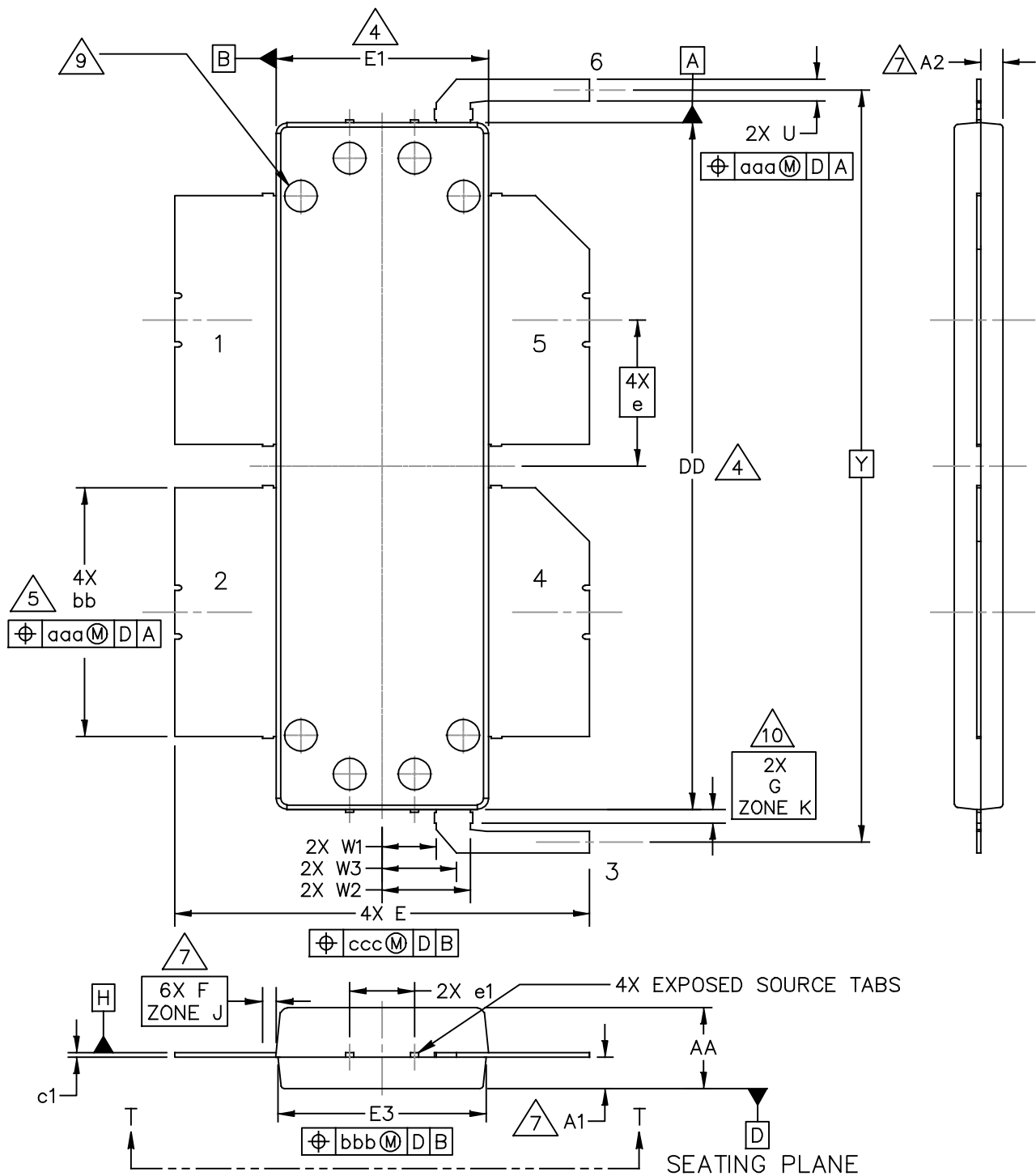


Figure 23. P3dB Load Pull AM/PM Contours (°)

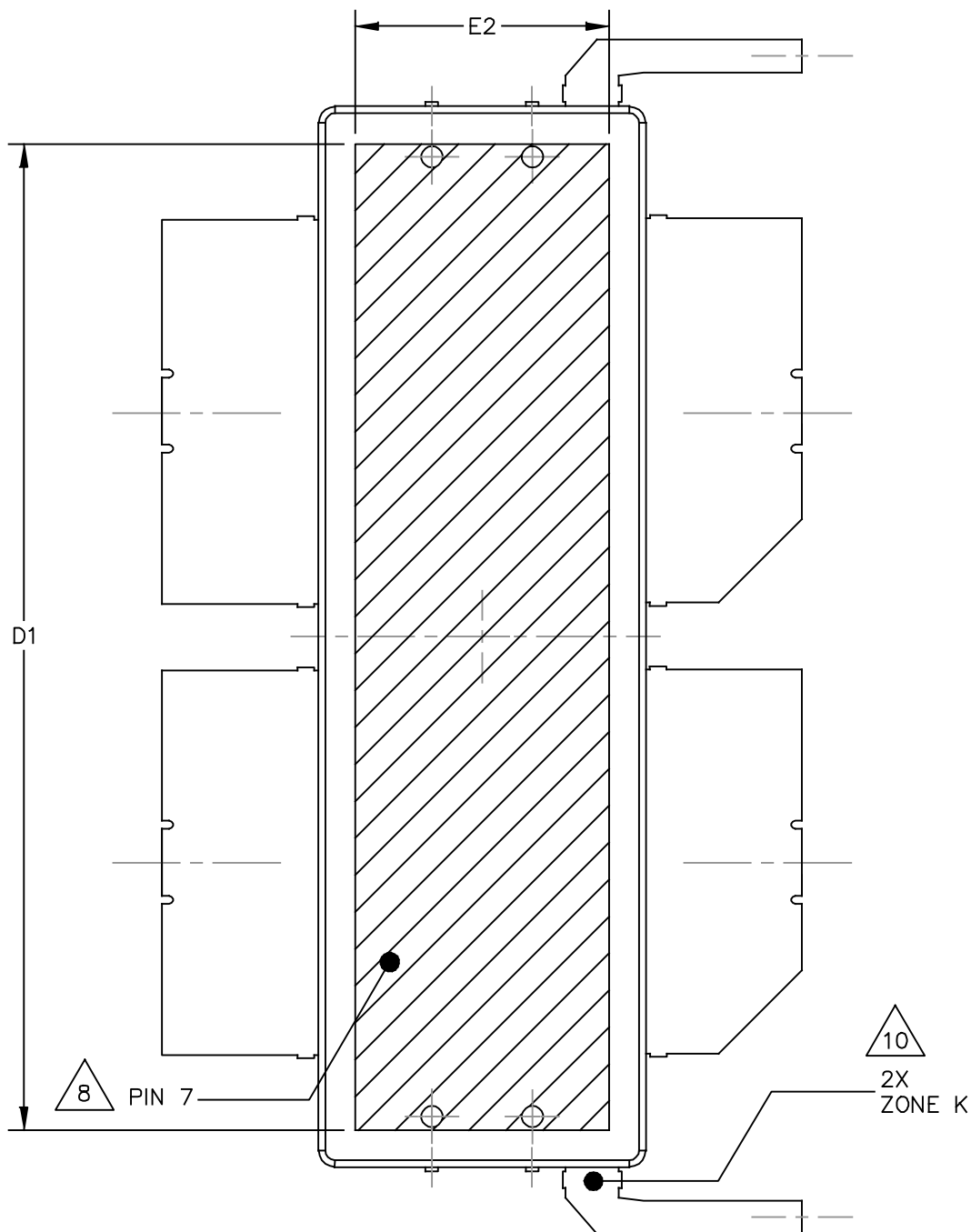
NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM-1230-4L2L	DOCUMENT NO: 98ASA00787D REV: 0	
	STANDARD: NON-JEDEC	
	26 NOV 2014	



BOTTOM VIEW
VIEW T-T

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: OM-1230-4L2L		DOCUMENT NO: 98ASA00787D	REV: 0
		STANDARD: NON-JEDEC	
		26 NOV 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLY WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1, 2, 4 AND 5. A2 APPLIES TO PINS 3 AND 6.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	0.148	.152	3.76	3.86	W1	.095	.105	2.41	2.67
A1	.059	.065	1.50	1.65	W2	.158	.168	4.01	4.27
A2	.056	.068	1.42	1.73	W3	.132	.142	3.35	3.61
DD	1.267	1.273	32.18	32.33	U	.037	.043	0.94	1.09
D1	1.180	----	29.97	----	Y	1.390 BSC		35.31 BSC	
E	.762	.770	19.35	19.56	bb	.457	.463	11.61	11.76
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.270 BSC		6.86 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
					ccc	.010		0.25	
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: OM-1230-4L2L					DOCUMENT NO: 98ASA00787D REV: 0				
					STANDARD: NON-JEDEC				
					26 NOV 2014				

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2015	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© 2015 Freescale Semiconductor, Inc.