TPSM82480 5.5-V Input, 6-A, Step-Down Converter with Integrated Inductor

1 Features

- Ultra Small 7.9 x 3.6 x 1.5 mm Power Module
- Output Current of 6 A
- Input Voltage Range 2.4 to 5.5 V
- Output Voltage Range 0.6 to 5.5 V
- Typical Quiescent Current of 23 µA
- Feedback Voltage Accuracy of ±1% (PWM Mode)
- Output Voltage Select
- Phase Shifted Operation
- Automatic Power Save Modes
- Forced PWM Mode
- Adjustable Soft Start
- Power Good / Thermal Good Outputs
- Undervoltage Lockout
- Over-current and Short-Circuit Protection
- Over-temperature Protection
- -40°C to 125°C Operating Junction Temperature Range

2 Applications

- Low Profile Point-of-Load Supply
- Solid State Drives
- Ultra Portable/Tablet/Embedded PC
- Optical Modules, CMOS Cameras
- Wireless Modules, Network Cards

3 Description

The TPSM82480 is a synchronous step-down DC-DC converter module for low profile point-of-load power supplies. The input voltage range of 2.4 to 5.5 V enables operation from typical 3.3-V or 5-V interface supplies as well as from backup circuits dropping down as low as 2.4 V.

The output current is up to 6 A continuously provided by two phases of 3 A each. These run out-of-phase, reducing pulse current noise significantly.

The TPSM82480 provides automatically entered power save modes to maintain high efficiency down to very light loads. This incorporates an automatic phase adding and shedding feature using both or only one phase according to the actual load. The pulse skip mode for very light loads can be switched off by using the MODE feature.

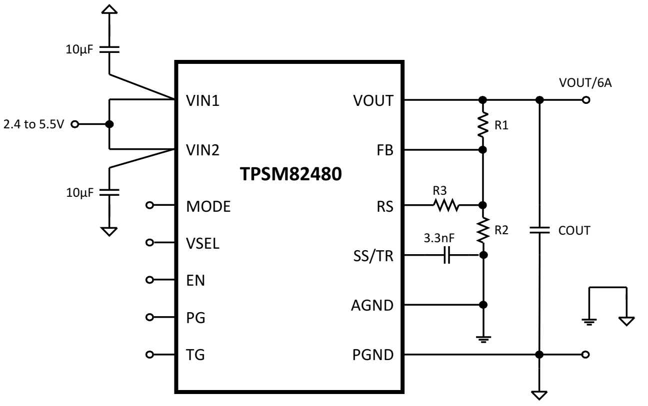
The device features a Power Good signal and an adjustable soft start. Also, the device features a Thermal Good signal to detect excessive internal temperature. The output voltage can be changed to a preselected value by VSEL pin. TPSM82480 is able to operate in 100% duty cycle mode.

Device Information[1]

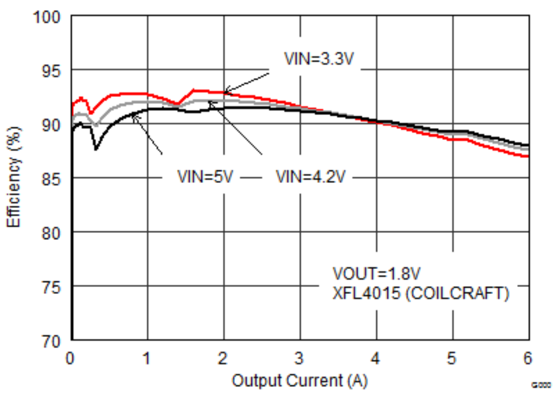
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPSM82480MOP	QFM (24)	7.90 × 3.60 x 1.55 mm

[1] For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current, V_{IN}= 12 V



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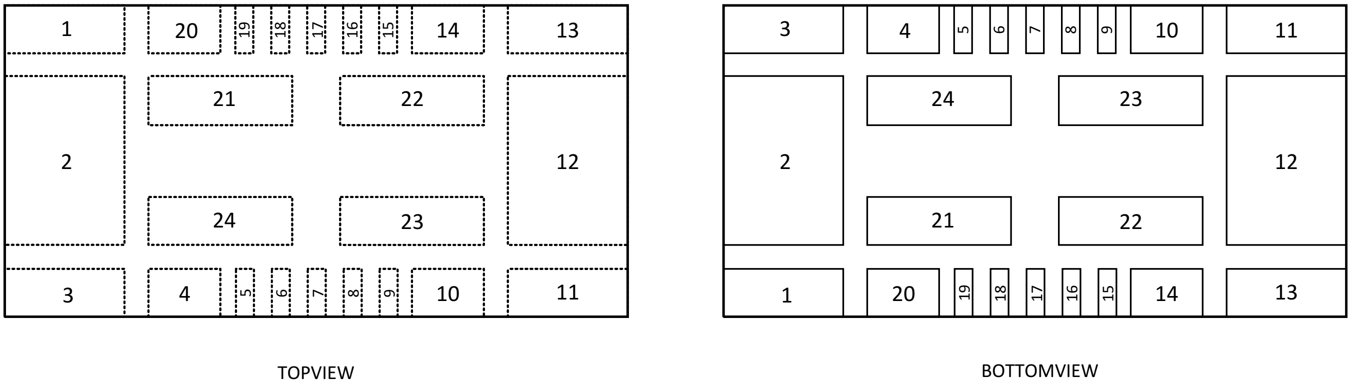
4 Revision History

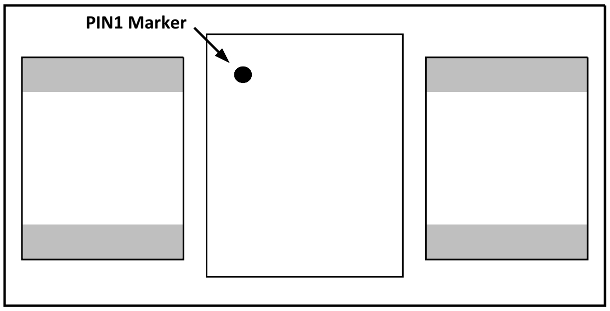
DATE	REVISION	NOTES
July 2017	*	Initial release.

5 Pin Configuration and Functions

**MOP Package
24-Pin QFM**



TOPVIEW BOTTOMVIEW



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT1	1		Output Voltage Node Phase 1 (master), Must be connect with VOUT2
PGND1	2, 3, 20,21		Power Ground Phase 1 (master)
VIN1	4, 24		Supply voltage Phase 1 (master)
EN	5		Enable input (High=Enabled, Low = Disabled)
PG	6		Power Good (open drain, requires pull-up resistor)
VSEL	7		Output Voltage Select (High = VOUT2, Low=VOUT1) , VOUT1 < VOUT2
TG	8		Thermal Good (open drain, requires pull-up resistor)
MODE	9		Operating mode selection (Low=Automatic PWM/PSM, High = Forced PWM)
VIN2	10, 23		Supply voltage Phase 2
PGND2	11,12, 14, 22		Power Ground Phase 2
VOUT2	13		Output Voltage Node Phase 2, Must be connected with VOUT1
SS/TR	15		Soft-Start / Tracking. An external capacitor connected to this pin sets the output voltage rise time.
AGND	16		Analog Ground
FB	17		Output voltage feedback for the adjustable version. Connect resistive voltage divider to this pin.
RS	18		Resistor Select. Connect resistor that sets the level for the second output voltage here (activated by VSEL= High)
VO	19		VOUT detection (connect to VOUT, output discharge is internally connected to this pin)

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Pin Voltage Range(1)	VIN	-0.3	6	V
	EN, VSEL, MODE, SS/TR, PG, TG	-0.3	6	V
	FB, RS	-0.3	3	V
Power Good / Thermal Good Sink Current	PG, TG		10	mA
Operating Junction Temperature Range, T_J		-40	150	°C
Storage Temperature Range, T_{stg}		-65	150	°C

(1) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage Range, V_{IN}	2.4		5.5	V
Output Voltage Range, V_{OUT}	0.6		5.5	V
Maximum Output Current, I_{OUT}	6			A
Operating junction temperature, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPSM82480	UNIT
		MOP 24 PINS	
		JEDEC with thermal vias	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.53	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to 125°C) and V_{IN} = 2.4 V to 5.5 V. Typical values at V_{IN} = 3.6 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input Voltage Range	V_{IN} rising	2.6		5.5	V
		V_{IN} falling	2.4		5.5	
I_Q	Operating Quiescent Current	EN = High, V_{IN} ≥ 3 V, I_{OUT} = 0 mA, device not switching, T_J = -40°C to +85°C		23	38	µA
		100% Mode operation		3.5	6.5	mA
I_{SD}	Shutdown Current	EN = Low (≤ 0.3 V), T_J = -40°C to +85°C		0.5	18.5	µA
V_{UVLO}	Undervoltage Lockout Threshold	Falling Input Voltage	2.2	2.3	2.4	V
		Hysteresis		200		mV
T_{SD}	Thermal Shutdown Temperature	PWM Mode, Rising Junction Temperature		160		°C
	Thermal Shutdown Hysteresis	PWM Mode		10		
CONTROL (EN, VSEL, MODE, SS/TR, PG, TG)						
V_H	Input Threshold Voltage (EN, VSEL, MODE)	to ensure High Level	1.2			V
V_L	Input Threshold Voltage (EN, VSEL, MODE)	to ensure Low Level			0.4	
$I_{LKG(EN)}$	Input Leakage Current (EN)	EN = V_{IN} or GND		10	200	nA
$I_{LKG(MODE)}$	Input Leakage Current (MODE, VSEL)			10	200	nA
$I_{SS/TR}$	SS/TR pin source current		4.7	5.25	5.8	µA
$V_{TH(TG)}$	Thermal Good Threshold Temperature	PWM Mode		120		°C
	Thermal Good Hysteresis	PWM Mode		10		
$V_{TH(PG)}$	Power Good Threshold Voltage	Rising (%V_{OUT})	93%	96%	99%	
		Falling (%V_{OUT})	89%	92%	95%	
$V_{L(PG)}$	Output Low Threshold (PG, TG)	I_{PG} = -2 mA			0.4	V
$I_{LKG(PG)}$	Input Leakage Current (PG)			2	700	nA
$I_{LKG(TG)}$	Input Leakage Current (TG)			2	100	nA
t_{SS}	Internal Soft-Start Time	SS/TR = V_{IN} or floating		80		µs
t_{DELAY}	Time from EN rising until start switching		100	200	400	µs
POWER SWITCH						
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	V_{IN} ≥ 3 V, Phase1		36	98	mΩ
		Phase2				
	Low-Side MOSFET ON-Resistance	Phase1		29	72	mΩ
		Phase2				
I_{LIM}	High-Side MOSFET Current Limit	per phase	4.3	5.0	5.8	A

Electrical Characteristics (continued)

over operating junction temperature range (T_J = –40°C to 125°C) and V_{IN} = 2.4 V to 5.5 V. Typical values at V_{IN} = 3.6 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_{REF}	Internal Reference Voltage				0.6		V
$I_{LKG(FB)}$	Input Leakage Current (FB)	EN = High	V_{FB} = 0.6 V		1	65	nA
$I_{LKG(RS)}$	Input Leakage Current (RS)		VSEL = Low, V_{RS} = 0.6 V		1	65	nA
R_{RS}	Internal resistance (RS to GND)		VSEL = High, I_{RS} = 1 mA		10	50	Ω
V_{OUT}	Output Voltage Range	V_{IN} ≥ V_{OUT}		0.6		5.5	V
V_{OUT}	Feedback Voltage Accuracy	PWM Mode, V_{IN} ≥ V_{OUT} + 1 V	T_J = –20°C to 85°C	-1%		1%	
			T_J = –40°C to 125°C	-1.4%		1.3%	
V_{OUT}	Feedback Voltage Accuracy	Power Save Mode, L = 0.47 µH, C_{OUT} = 4 x 22 µF[1]		-1.4%		2.5%	
	Output Discharge Current[2]	EN = Low, V_{OUT} = 2.5 V			120		mA
	Load Regulation	V_{OUT} = 1.8 V, PWM mode operation			0.02		%/A
	Line Regulation	2.6 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} = 1.8 V, I_{OUT} = 6 A, PWM mode operation			0.02		%/V

(1) The output voltage accuracy in Power Save Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple.

(2) For detailed information on output discharge see *Active Output Discharge*.

6.6 Typical Characteristics

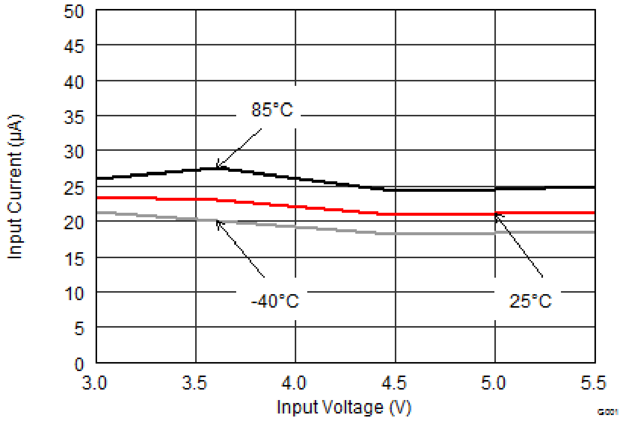


Figure 2. Quiescent Current

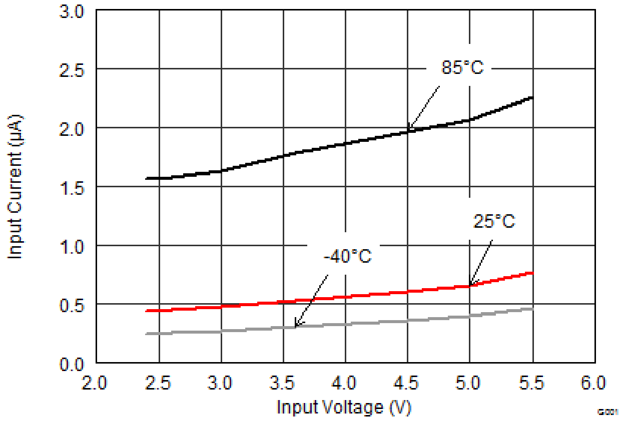


Figure 3. Shutdown Current

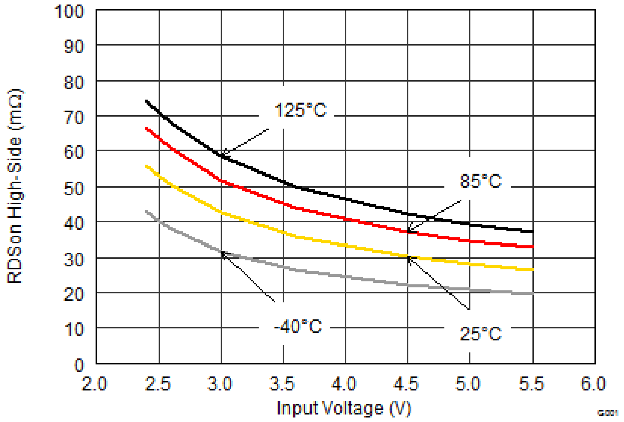


Figure 4. High-Side Switch Resistance

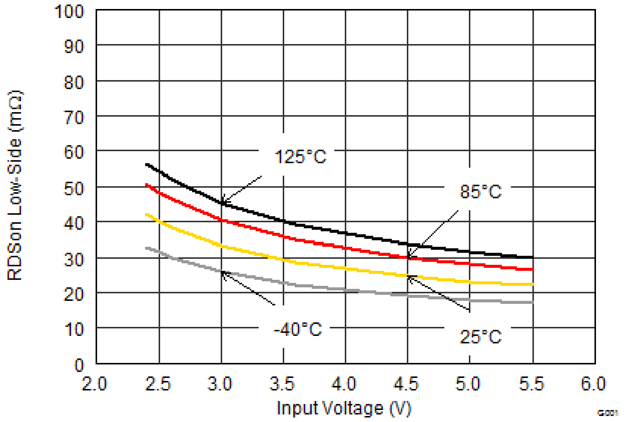


Figure 5. Low-Side Switch Resistance

7 Detailed Description

7.1 Overview

The TPSM82480 is a high efficiency synchronous switched mode step-down converter module based on a 2-phase peak current control topology. It is designed for smallest solution size low-profile applications, converting a 2.4 V to 5.5 V input voltage into a lower 0.6 V to 5.5 V output voltage. While an outer voltage loop sets the regulation threshold for the inner current loop, based on the actual V_{OUT} level, the inner current loop regulates to the actual peak inductor current level for every switching cycle. The regulation network is internally compensated. While the ON-time is determined by duty cycle, inductance and cycle peak current, the switching frequency of typically 2.2 MHz is set by a predicted OFF-time. The device features a Power Save Mode (PSM) to keep the conversion efficiency high over the whole load current range.

The TPSM82480 is a 2-phase converter, sharing the load among the phases. Identical in construction, the second phase control is connected with an adaptive delay to the first phase. Both the phases use the same regulation threshold and cycle-by-cycle peak current setpoint. This ensures a phase-shifted as well as current-balanced operation. Using the advantages of the 2-phase topology, a 6-A continuous output current is provided with high performance and as small as possible solution size.

7.2 Functional Block Diagram

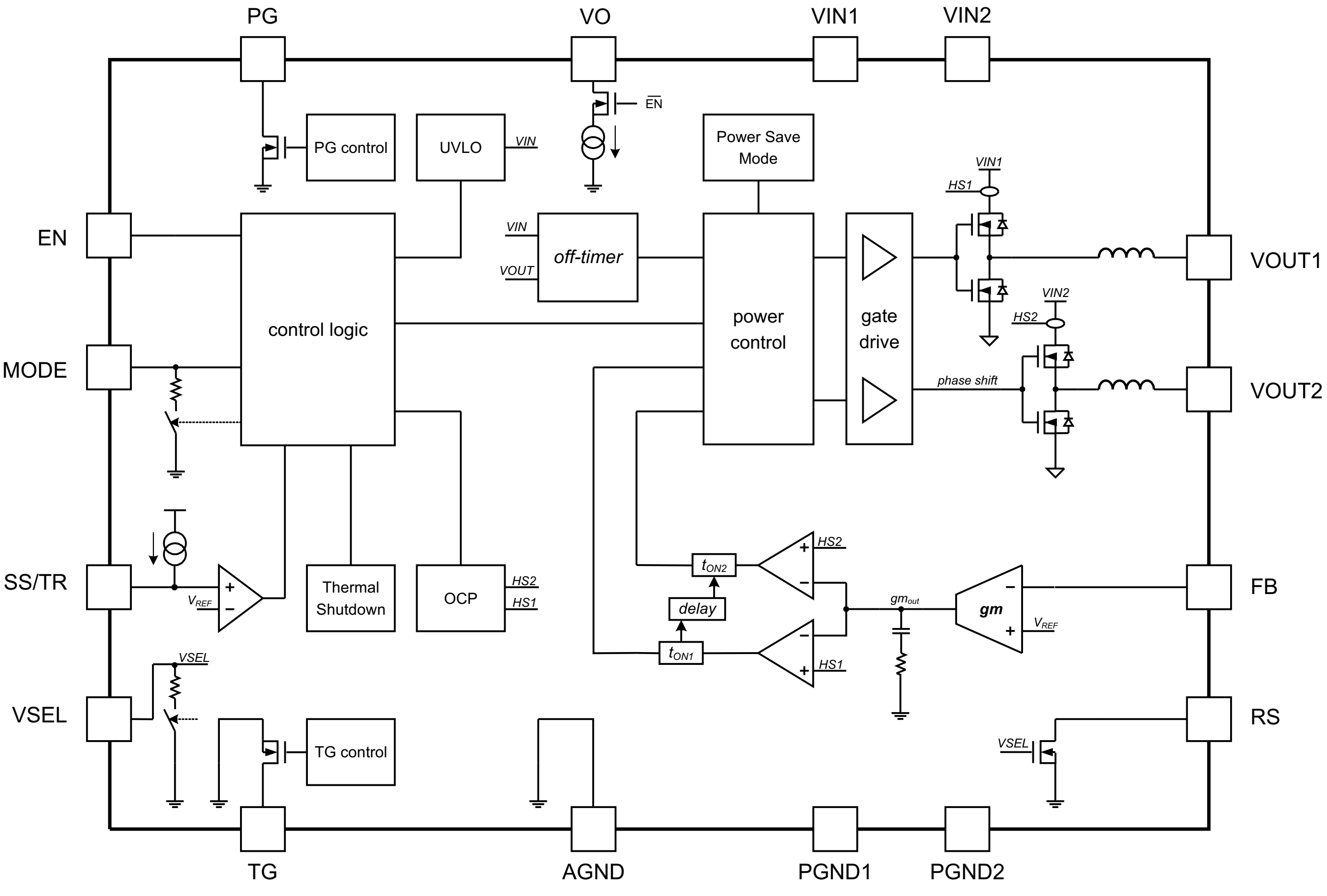


Figure 6. TPSM82480

7.3 Feature Description

7.3.1 Enable / Shutdown (EN)

The device starts operation, when VIN is present and enable (EN) is set High. Since the boundary EN thresholds are specified with 1.2 V for rising and 0.4 V for falling voltages, the typical vales are 0.85 V (rising) and 0.65 V (falling). The device is disabled by pulling EN Low. Leaving the EN pin floating is not recommended.

7.3.2 Soft Start (SS), Pre-biased Output

The internal soft start circuit controls the output voltage slope during startup. This avoids excessive inrush current and provides an adjustable controlled output-voltage rise time. The soft start also prevents unwanted voltage drop from high impedance power sources or batteries.

When EN is set to start device operation, the device starts switching after a delay of typically 200 µs and VOUT rises with a slope, controlled by the external capacitor which is connected to the SS/TR pin (soft start). Leaving the SS/TR pin floating or connecting to VIN provides internally set fastest startup with a soft start slope of about 80us. See *Application Curves* for typical startup operation.

The device can start into a pre-biased output. In this case, the device starts switching, only when the internal set point for VOUT increases above the pre-biased voltage level.

7.3.3 Tracking (TR)

The device tracks an external voltage applied to the SS/TR pin. The FB voltage tracks the external voltage as long as it is below about 0.6V. Above 0.6V the device goes to normal operation. If the voltage at the SS/TR pin decreases below about 0.6V, the FB voltage tracks again this voltage. See *Tracking* for further details.

7.3.4 Output Voltage Select (VSEL)

A resistive divider (VOUT to FB to AGND) sets the output voltage of the TPSM82480. Providing a logic High level at the VSEL pin, another resistor, connected between FB and RS pins is connected in parallel to the lower resistor of the divider. This sets a different higher output voltage and can be used for dynamic voltage scaling (see *Setting* V_{OUT2} *Using the VSEL Feature*).

If the VSEL pin is set Low, the device connects an internal pull down resistor to keep the internal logic level Low, even if the pin is floating afterwards. The device disconnects the resistor, if the pin is set to High.

7.3.5 Forced PWM (MODE)

To avoid *Power Save Mode (PSM) Operation*, the device can be forced to PWM mode operation by pulling the MODE pin High. In this case the device operates continuously with it's nominal switching frequency and the minimum peak current can go as low as -500 mA.

If the MODE pin is set Low, the device connects an internal pull down resistor to keep the internal logic level Low, even if the pin is floating afterwards. The device disconnects the resistor, if the pin is set to High.

7.3.6 Power Good (PG)

The TPSM82480 has a built in power good function. The PG pin goes High, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or thermal shutdown, PG is Low. The PG pin is an open drain output that requires a pull-up resistor and can sink typically 2mA. If not used, the PG pin can be left floating or grounded.

7.3.7 Thermal Good (TG)

As long as the junction temperature of the TPSM82480 is below the thermal good temperature of typically 120°C, the logic level at the TG pin is High. If the junction temperature exceeds that temperature, the TG pin goes Low. This can be used for the system to take action preventing excessive heating or even thermal shutdown. The TG pin is an open drain output that requires a pull-up resistor and can sink typically 2mA. If not used, the TG pin can be left floating or grounded.

ADVANCE INFORMATION

Feature Description (continued)

7.3.8 Active Output Discharge

The VO pin, connected to the output voltage, provides an active discharge path when the device is switched off by setting EN Low or UVLO event. In case of being activated, this discharge circuit sinks typically 120mA for output voltages of typically 1 V and above. If V_{OUT} is lower, the active current sink enters linear operation mode and the discharge current decreases.

7.3.9 Undervoltage Lockout (UVLO)

The undervoltage lockout prevents misoperation of the device, if the input voltage drops below the UVLO threshold which is set to typically 2.3 V. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

7.3.10 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typical), the device goes in thermal shutdown with a hysteresis of about 10°C. Both the power FETs are turned off and the PG pin goes Low. Once T_J has decreased enough, the device resumes normal operation with Soft Start.

7.4 Device Functional Modes

7.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82480 is based on a predictive OFF-time peak current control topology, operating with PWM in continuous conduction mode for heavier loads. The switching frequency is typically 2.2MHz. Both the master and follower phase regulate to the same VOUT level, each with a separate current loop, using the same peak current set point, cycle by cycle. This provides excellent peak current balancing, independent of inductor dc resistance matching. Since the follower phase operates with an adaptive delay to the master phase, phase shifted operation is always obtained. If the load current decreases, the device runs with the master phase only (see *Phase Add/Shed and Current Balancing*).

PWM only mode can be forced by pulling MODE pin High. If MODE is set Low, the device features an automatic transition into Power Save Mode, entered at light loads, running in discontinuous conduction mode (DCM).

7.4.2 Power Save Mode (PSM) Operation

As the load current decreases to half the ripple current, the converter enters Power Save Mode operation. During PSM, the converter operates with reduced switching frequency maintaining high conversion efficiency. Power Save Mode is based on an adaptive peak current target, to keep output voltage ripple low. Since each pulse shifts V_{OUT} up, a pause time happens until V_{OUT} trips the internal V_{OUT_Low} threshold again and the next pulse takes place.

The switching frequency in PSM (one phase operation) calculates as:

$$f_{SW(PSM)} = \frac{2 \cdot I_{OUT} \cdot V_{OUT}\left(V_{IN} - V_{OUT}\right)}{L \cdot I_{PEAK}^{2} \cdot V_{IN}} \tag{1}$$

7.4.3 Minimum Duty Cycle and 100% Mode Operation

The minimum on-time, which is typically 70ns, normally determines a limit on the minimum operating duty cycle. The calculation is:

$$DC_{min} = 70\text{ns} \cdot 100\% \cdot f_{SW}\,[\text{Hz}] \tag{2}$$

However, a frequency foldback lowers the switching frequency depending on the duty cycle and ensures proper regulation for every duty cycle.

Device Functional Modes (continued)

There is no limit towards maximum duty cycle. When the input voltage becomes close to the output voltage, the device enters automatically 100% duty cycle mode and both high-side FETs switch on as long as VOUT remains below the regulation setpoint. In this case, the voltage drop across the high-side FETs and the inductors determines the output voltage level. An estimate for the minimum input voltage to maintain output voltage regulation is:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left[\frac{R_{DS(ON)}}{2} + 13.5\text{m}\Omega\right] \tag{3}$$

Where the maximum DCR of the inductors is 27mΩ.

In 100% duty cycle mode, the low-side FETs are switched off. The typical quiescent current in 100% mode is 3.5 mA.

7.4.4 Phase Shifted Operation

Using an inherent benefit of the two-phase conversion, the two phases of TPSM82480 run out of phase. For every switching cycle, the second phase is not allowed to turn on its high-side FET until the master phase has reached its peak current value. This limits the input RMS current and corresponding switching noise.

7.4.5 Phase Add/Shed and Current Balancing

When the load current is below the internal threshold, only the master phase operates. The second phase activates, if the load current exceeds the threshold of typically 1.7 A. The second phase powers off with a hysteresis of about 0.5 A, when the load current decreases.

7.4.6 Current Limit and Short Circuit Protection

Each phase has a separate integrated peak current limit. The dc values are specified in the *Electrical Characteristics*. While its minimum value limits the output current of the phase, the maximum number gives the current that must be considered to flow in some operating case. At the peak current limit, the device provides its maximum output current.

However, if the current limit situation remains for 512 consecutive switching cycles, the peak current folds back to about 1/3 of the regular limit. This limits the output power for over current and short circuit events. The foldback current limit is released to the normal one only if the load current has decreased as far as needed to undercut the (foldback) peak current limit.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM82480 is a switched mode step-down converter module, able to convert a 2.4-V to 5.5-V input voltage into a lower 0.6-V to 5.5-V output voltage, providing up to 6 A continuous output current. It needs a minimum amount of external components. Apart from the output and input capacitors, additional resistors or capacitors are only needed to enable features like soft start, adjustable and selectable output voltage as well as Power Good and/or Thermal Good.

8.2 Typical Application

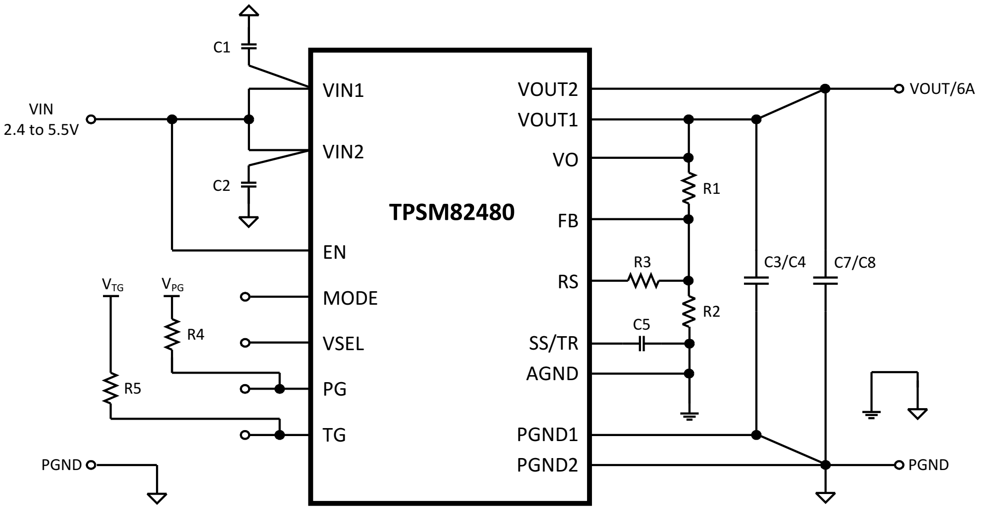


Figure 7. Typical Application using TPSM82480 for a 6A Point-Of-Load Power Supply

8.2.1 Design Requirements

The following design guideline provides a range for the component selection to operate within the recommended operating conditions. Table 1 shows the components selection that was used for the measurements shown in the *Application Curves*.

Typical Application (continued)

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
Power Module	5.5-V, 6-A step-down module with integrated inductor	TPSM82480MOP, Texas Instruments
C1, C2	2x22-µF, 10-V, ceramic, 0603, X5R	GRM188R61A226ME15#, muRata
C3, C4, C7, C8	4x22-µF, 25-V, ceramic, 0805, X5R	GRM21BR61E226ME44L, muRata
C5	3300-pF, 10-V, ceramic, 0402	Standard
R1, R2, R3	Depending on Vout1 and Vout2, chip, 0402, 0.1%	Standard
R4, R5	470-kΩ, chip, 0603, 1/16-W, 1%	Standard

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Adjustable Output Voltage

While the device regulates the FB voltage to 0.6V, the output voltage is specified from 0.6 to 5.5 V. A resistive divider (from VOUT to FB to AGND) sets the actual output voltage of the TPSM82480. Equation 4 and Equation 5 are calculating the values of the resistors. First, determining the current through the resistive divider leads to the total resistance (R_1 + R_2). A minimum divider current of about 5 µA is recommended and can be higher if needed.

$$R_1 + R_2 = \frac{V_{OUT}}{I_{FB}} \tag{4}$$

$$R_2 = \frac{V_{REF}}{V_{OUT}}(R_1 + R_2) \tag{5}$$

8.2.2.2 Setting V_{OUT2} Using the VSEL Feature

A V_{OUT} level, different as set with R_1 and R_2 (see *Setting the Adjustable Output Voltage*), can be forced by connecting R_3 between FB and RS pins and pulling VSEL High. R_3 is calculated using Equation 6.

$$R_3 = \frac{V_1 \cdot R_1 \cdot R_2^2}{(V_2 - V_1) \cdot (R_1 \cdot R_2 + R_2^2)} \quad \text{for} \quad (V_2 > V_1) \tag{6}$$

where:

V_1 is the lower level output voltage and

V_2 the higher level output voltage.

8.2.2.3 Output Capacitor Selection

The recommended minimum output capacitance is 4 x 22 µF, that can be ceramic capacitors exclusively. A larger value of C_{OUT} might be needed for V_{OUT} ≤ 1.8V, to improve transient response performance, as well as for V_{OUT} > 3.3 V to compensate for voltage bias effects of the ceramic capacitors. The other way round, using of an additional feed forward capacitor can help reducing amount of output capacitance that is needed to achieve a certain transient response target (see Table 3).

The TPSM82480 provides a wide output voltage range of 0.6 V to 5.5 V. While stability is a critical criteria for the output filter selection, the output capacitor value also determines transient response behavior, ripple and accuracy of V_{OUT}. The internal compensation is designed for an output capacitance range from about 50 µF to 150 µF effectively. Since ceramic capacitors are used preferably, this translates into nominal values of 4 x 22 µF to 4 x 47 µF and mainly depends on the output voltage. The following values are recommended:

Table 2. Recommended Output Capacitor Values (nominal)

	$V_{OUT} \leq 1.0V$	$1.0V \leq V_{OUT} \leq 3.3V$	$V_{OUT} \geq 3.3V$
2x22µF			
4x22µF		√	
4x47µF	√	√	√
6x47µF			

Beyond the recommendations in Table 2, other values can be chosen and might be suitable depending on VOUT and actual effective capacitance. In such case, stability needs to be checked within the actual environment.

Even if the output capacitance is sufficient for stability, a different value might be desirable to improve the transient response behavior. Table 3 can be used to determine capacitor values for specific transient response targets:

Table 3. Recommended Output Capacitor Values (nominal)

Output Voltage [V]	Load Step [A]	Output Capacitor Value[1]	Feedforward Capacitor[1]	Typical Transient Response Accuracy	
				±mV	±%
1.0	0 - 3	4 x 47µF	-	50	5
	3 - 6			50	5
1.8	0 - 3	4 x 22µF	36pF	50	3
	3 - 6			50	3
2.5	0 - 3	4 x 22µF	36pF	62	2.5
	3 - 6			50	2
3.3	0 - 3	4 x 47µF	36pF	100	3
	3 - 6			80	2.5

(1) The values in the table are nominal values. The effective capacitance can differ significantly, depending on package size, voltage rating and dielectric material.

The architecture of the TPSM82480 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X5R or X7R dielectrics. Using even higher values than demanded for stability and transient response has further advantages like smaller voltage ripple and tighter dc output accuracy in Power Save Mode.

8.2.2.4 Input Capacitor Selection

The input current of a buck converter is pulsating. Therefore, a low ESR input capacitor is required to prevent large voltage transients at the source but to provide peak currents to the device. The recommended value for most applications is 2 x 10 µF, split between the VIN1 and VIN2 inputs and placed as close as possible to these pins and PGND pins. If additional capacitance is needed, it can be added as bulk capacitance. To ensure proper operation, the effective capacitance at the VIN pins must not fall below 2 x 5 µF.

Low ESR multilayer ceramic capacitors are recommended for best filtering. Increasing with input voltage, the dc bias effect reduces the nominal capacitance value significantly. To decrease input ripple current further, larger values of input capacitors can be used.

8.2.2.5 Soft Start Capacitor Selection

The soft start ramp time can be set externally connecting a capacitor between the SS/TR and AGND pins. The capacitor value C_{SS} that is needed to get a specific rising time Δt_{SS} calculates as:

$$C_{SS} = \Delta t_{SS} \cdot \frac{5.25\mu A}{0.6V} \qquad (7)$$

Since the device has an internal delay time Δt_{DELAY} from EN=High to start switching, the overall startup time is longer as shown in Figure 8.

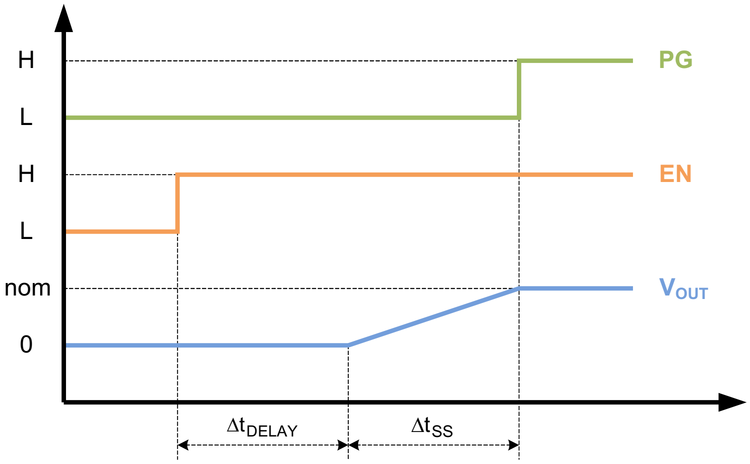


Figure 8. Soft Start Δt_{SS}

If very large output capacitances are used (e.g. >4x47µF), the use of a soft start capacitor is mandatory to secure complete startup.

8.2.2.6 Tracking

For values up to 0.6V, an external voltage, connected to the SS/TR pin, drives the voltage level at the FB pin. In doing so, the voltage at the FB pin is directly proportional to the voltage at the SS/TR pin.

When choosing the resistive divider proportion according to Equation 8, V_{OUT} tracks V_{TR} simultaneously.

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \tag{8}$$

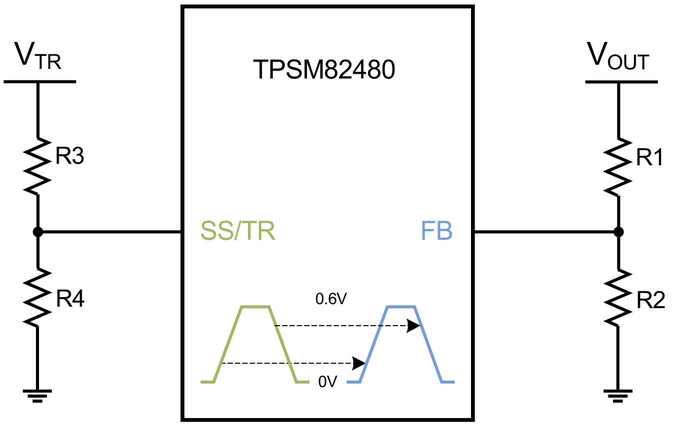


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Figure 9. Voltage Tracking

Following the example of *Setting the Adjustable Output Voltage* with V_{OUT} = 1.8 V, R_1 = 240 kΩ and R_2 = 120 kΩ, *Equation 9* and Equation 10 calculate R3 and R4, connected to the SS/TR pin. Different to the resistive divider at the FB pin, a larger current must be chosen, to avoid a tracking offset caused by the 5.25 µA current that flows out of the SS/TR pin. Assuming a 250 µA current, R_4 calculates as follows:

$$R_4 = \frac{0.6V}{250\mu A} = 2.4k\Omega \tag{9}$$

R_3 calculates now rearranging Equation 8:

$$R_3 = R_4 \cdot \frac{R_1}{R_2} = 2.4k\Omega \cdot \frac{240k\Omega}{120k\Omega} = 4.8k\Omega \tag{10}$$

However, the following limitations can influence the tracking accuracy:

- The upper limit of the SS/TR voltage that can be tracked is about 0.6V. Since it is detected internally by a comparator, process variation and ramp speed can cause up to ±30 mV different threshold.
- In case that the voltage at SS/TR ramps up immediately when VIN is supplied or EN is set High, the internal startup delay, Δt_{DELAY}, delays the ramp of V_{OUT}. The internal ramp starts after Δt_{DELAY} at the voltage level, which is actually present at the SS/TR pin.
- The tracking down speed is limited by the RC time constant of the internal output discharge (always connected when tracking down) and the actual load with the output capacitance. Note: The device tracks down with the same behavior for MODE High (Forced PWM) or Low (Auto PSM).

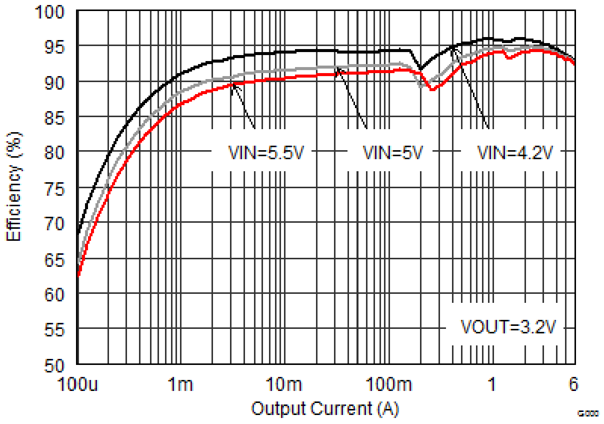
8.2.2.7 Thermal Good

The Thermal Good pin provides an open drain output. The logic level is given by the pull up source which can be VOUT. In this case, TG goes or stays Low, when the device switches off due to EN, UVLO or Thermal Shutdown.

When using an independent source for the pull up logic, the logic behavior at shutdown differs, because the TG pin internally goes high impedance. As before, TG goes Low when TG threshold is reached, but goes back High in the event of being switched off (e.g. Thermal Shutdown).

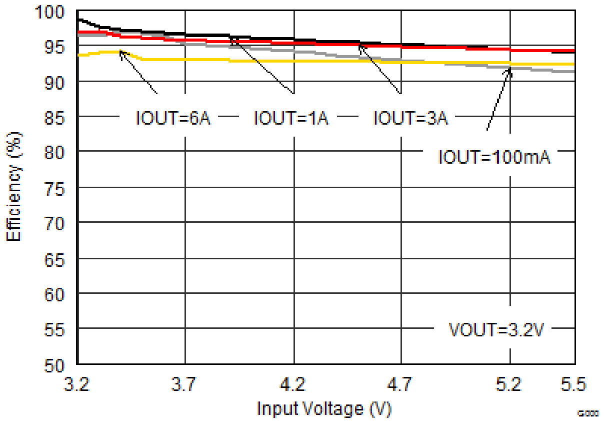
8.2.3 Application Curves

V_{IN}= 3.6 V, V_{OUT} = 1.8V (R1 / R2 = 240 kΩ / 120 kΩ), T_A = 25°C, (unless otherwise noted)



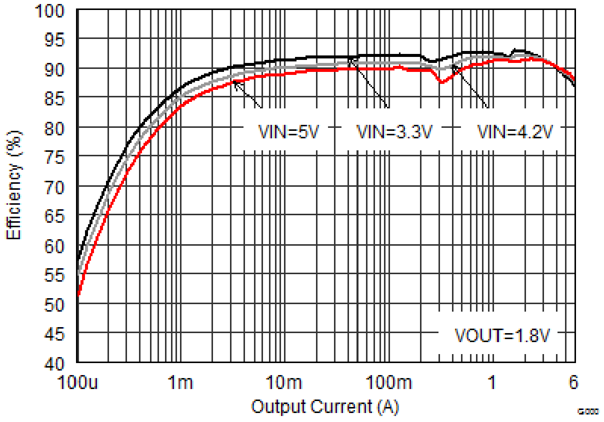
V_{OUT} = 3.2 V

Figure 10. Efficiency vs Output Current



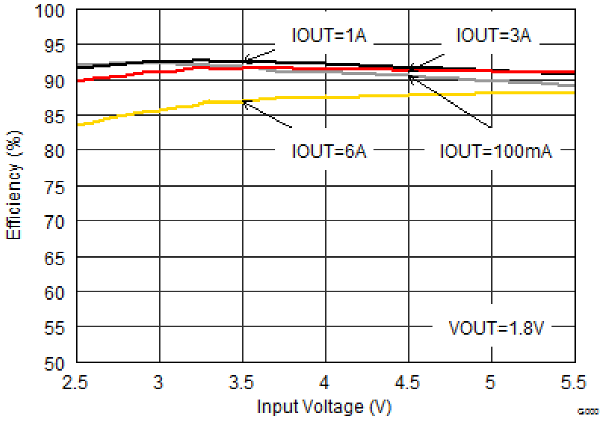
V_{OUT} = 3.2 V

Figure 11. Efficiency vs Input Voltage



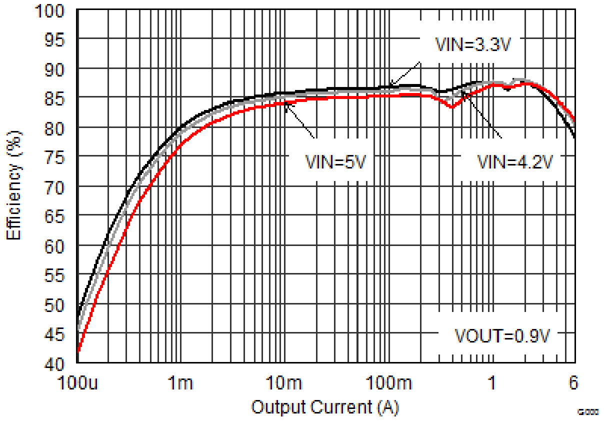
V_{OUT} = 1.8 V

Figure 12. Efficiency vs Output Current



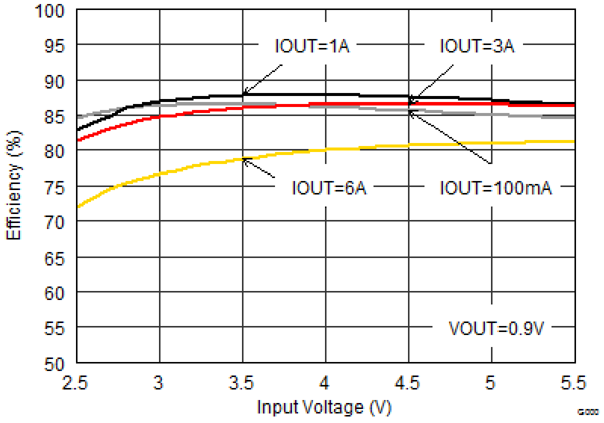
V_{OUT} = 1.8 V

Figure 13. Efficiency vs Output Voltage



V_{OUT} = 0.9 V

Figure 14. Efficiency vs Output Current



V_{OUT} = 0.9 V

Figure 15. Efficiency vs Input Voltage

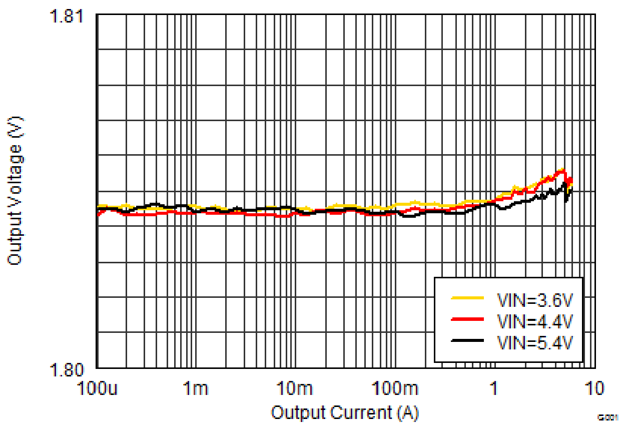


Figure 16. Output Voltage vs Output Current (Load Regulation)

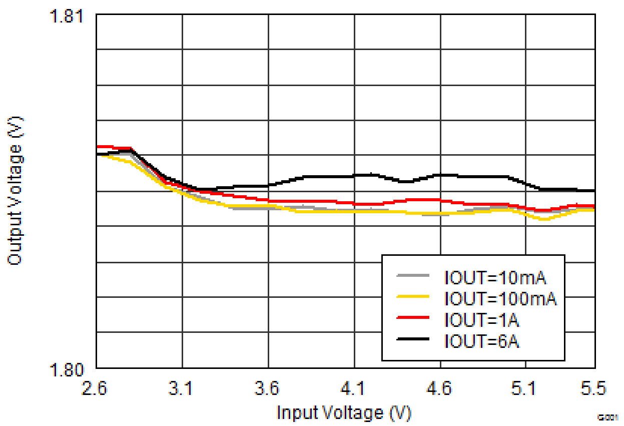
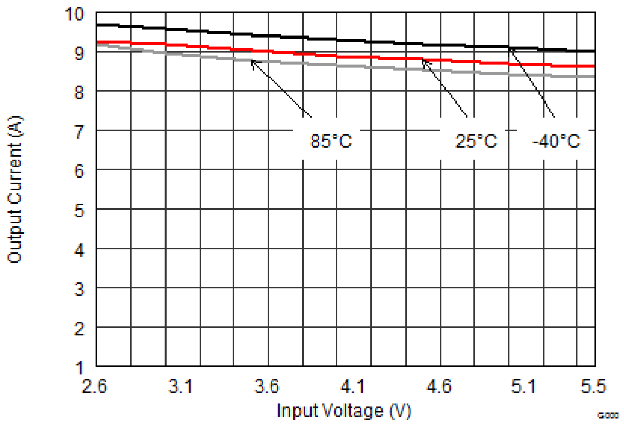
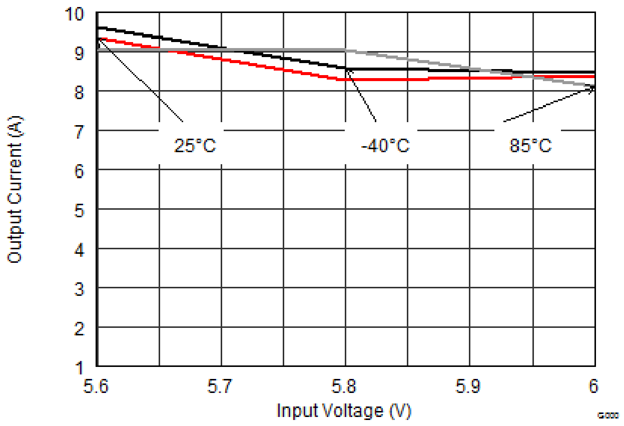


Figure 17. Output Voltage vs Input Voltage (Line Regulation)



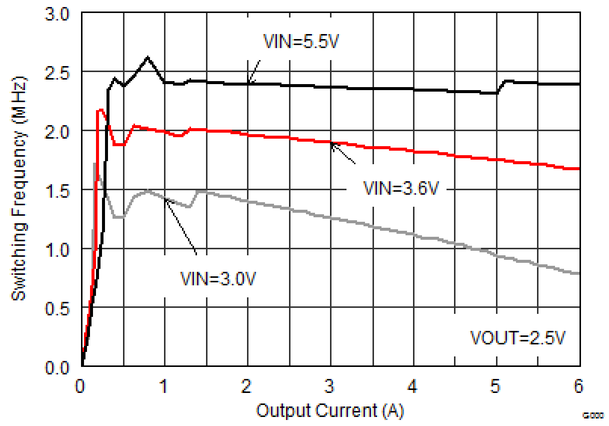
V_{OUT} = 0.6 V

Figure 18. Maximum Output Current



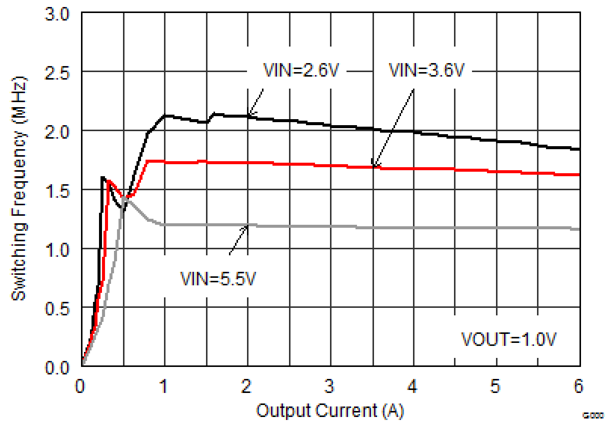
V_{OUT} = 5.5 V

Figure 19. Maximum Output Current



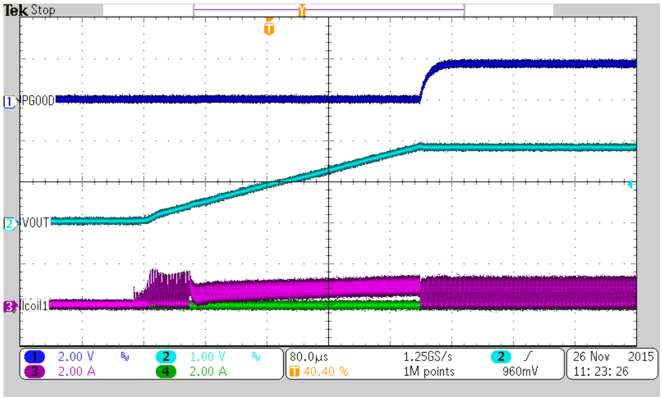
V_{OUT} = 2.5 V

Figure 20. Switching Frequency vs Output Current



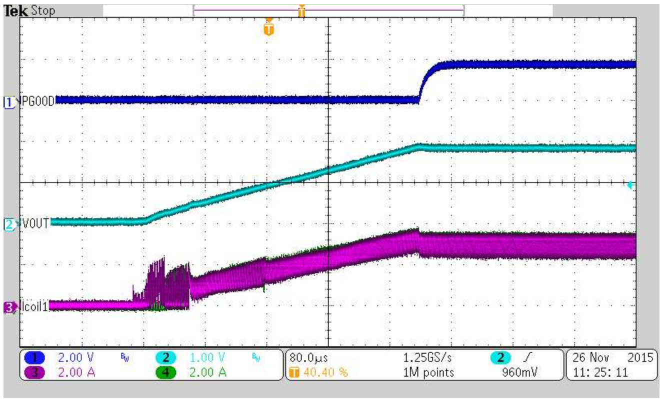
V_{OUT} = 1 V

Figure 21. Switching Frequency vs Output Current



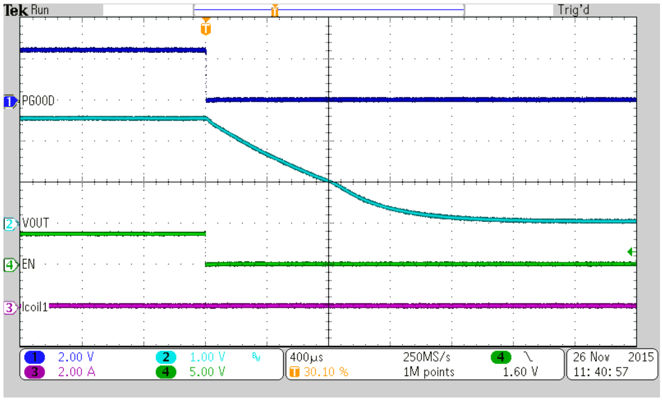
V_{OUT} = 1.8 V

Figure 22. Startup into 3.3 Ω



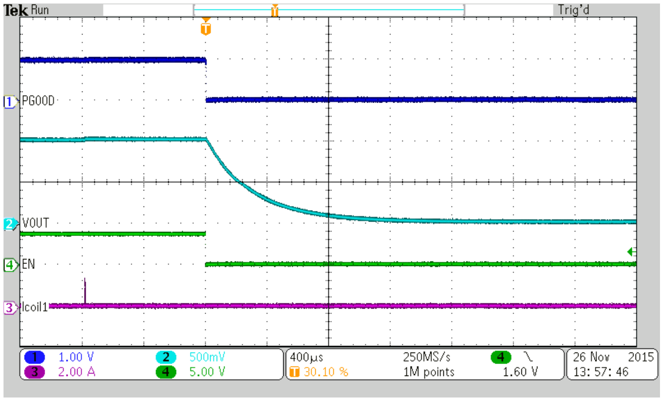
V_{OUT} = 1.8 V

Figure 23. Startup into 0.3 Ω



V_{OUT} = 2.5 V

Figure 24. Output Discharge



V_{OUT} = 1 V

Figure 25. Output Discharge

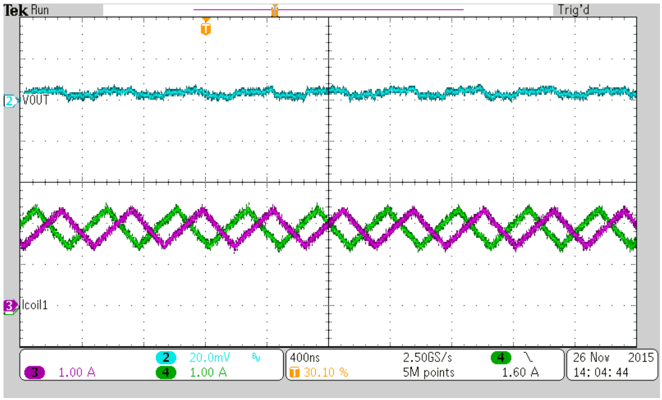
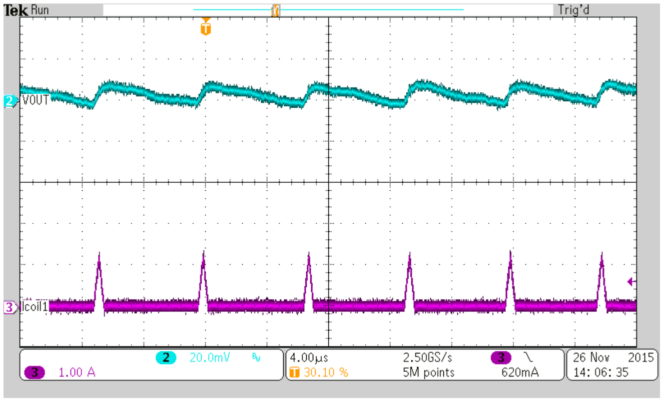


Figure 26. Typical Operation PWM



I_{OUT} = 50 mA

Figure 27. Typical Operation PSM

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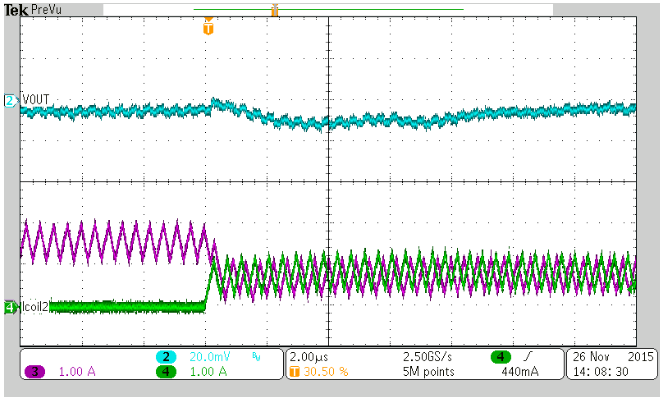


Figure 28. Adding 2nd Phase

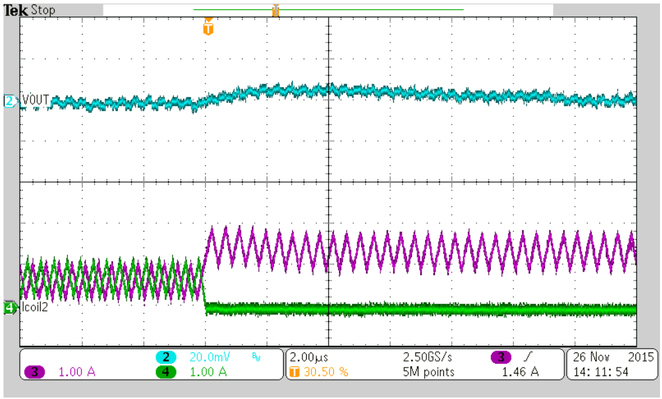


Figure 29. Shedding 2nd Phase

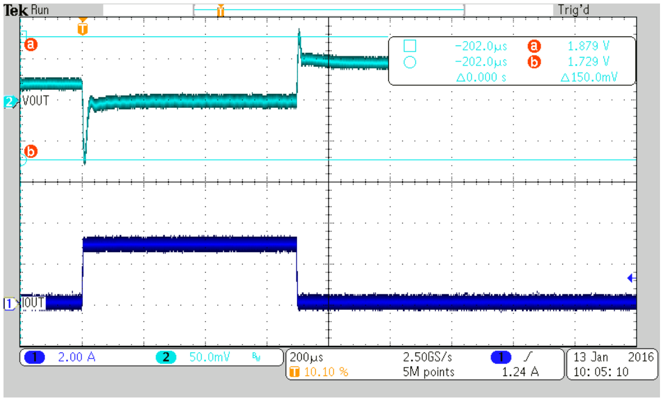
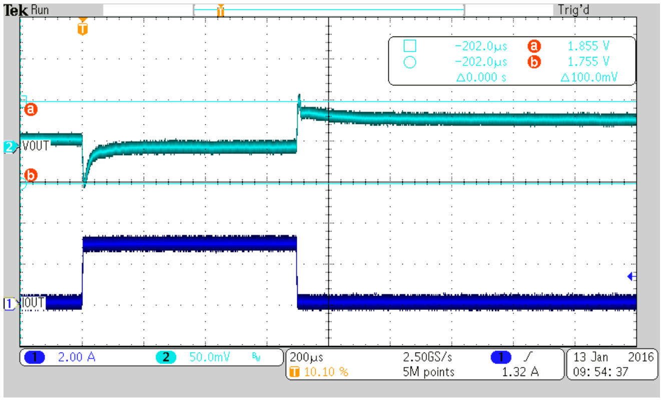


Figure 30. Load Transient Response (PSM-PWM), Load Step 0 to 3 A



C_{ff} = 36 pF (nom)

Figure 31. Load Transient Response (PSM-PWM), Load Step 0 to 3 A

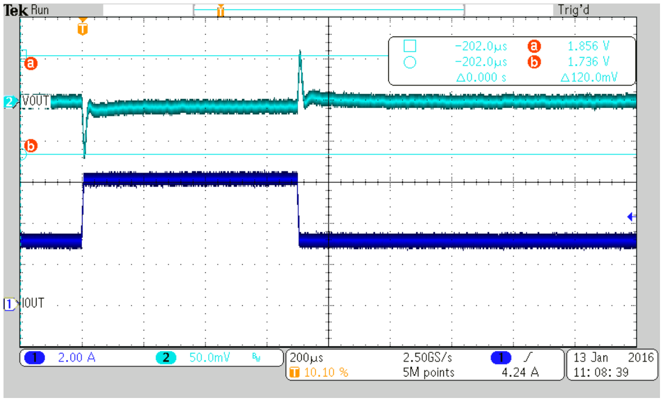
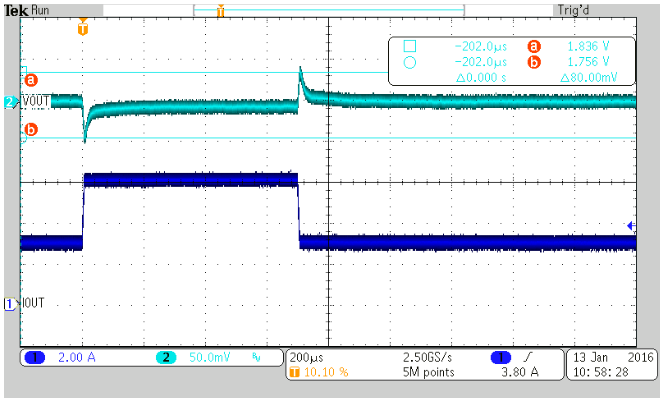
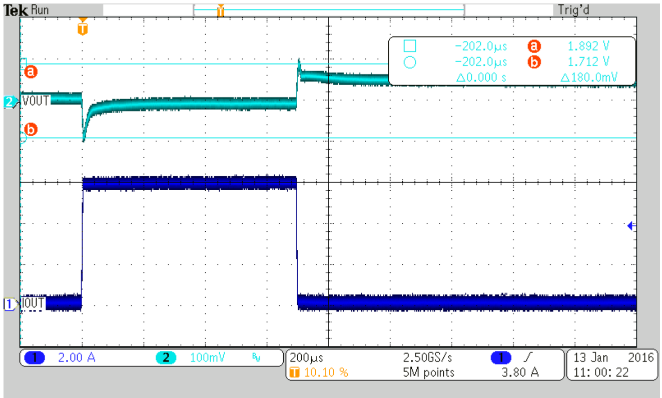


Figure 32. Load Transient Response (PWM-PWM), Load Step 3 to 6 A



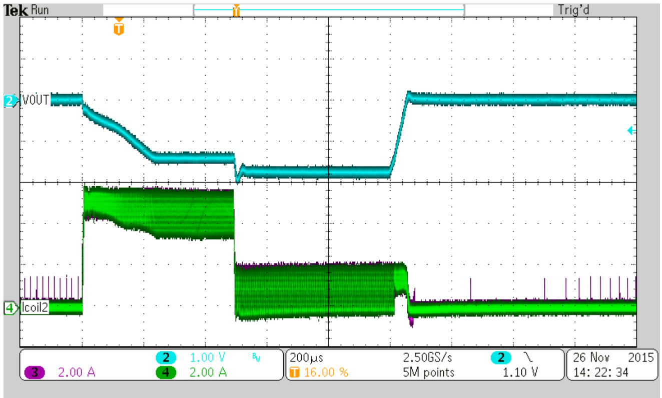
C_{ff} = 36 pF (nom)

Figure 33. Load Transient Response (PWM-PWM), Load Step 3 to 6 A



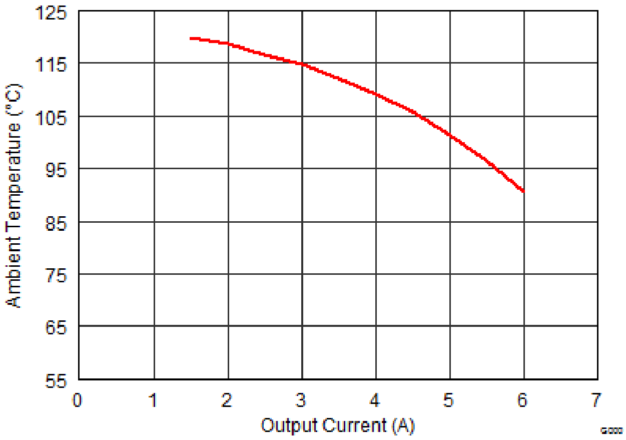
C_{ff} = 36 pF (nom)

Figure 34. Load Transient Response (PWM-PWM), Load Step 0 to 6 A



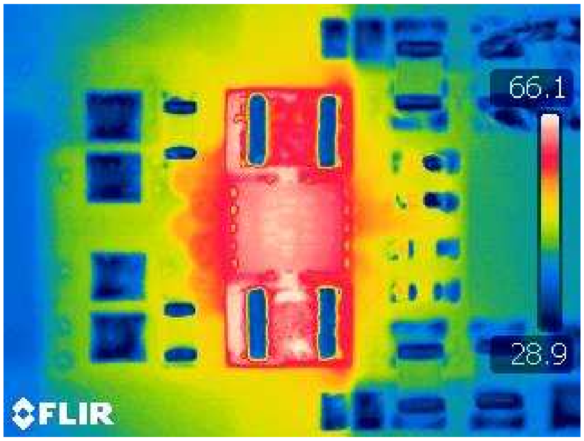
I_{OUT} = 10 A

Figure 35. Current Limit Fold-Back at Overload



V_{IN} = 5 V V_{OUT} = 3.3 V

Figure 36. Maximum Ambient Temperature (TPSM82480 EVM)



V_{IN} = 5 V V_{OUT} = 3.3 V I_{OUT} = 6 A

Figure 37. Device Temperature (TPSM82480 EVM)

ADVANCE INFORMATION

8.3 System Examples

This section provides typical schematics for commonly used output voltage values.

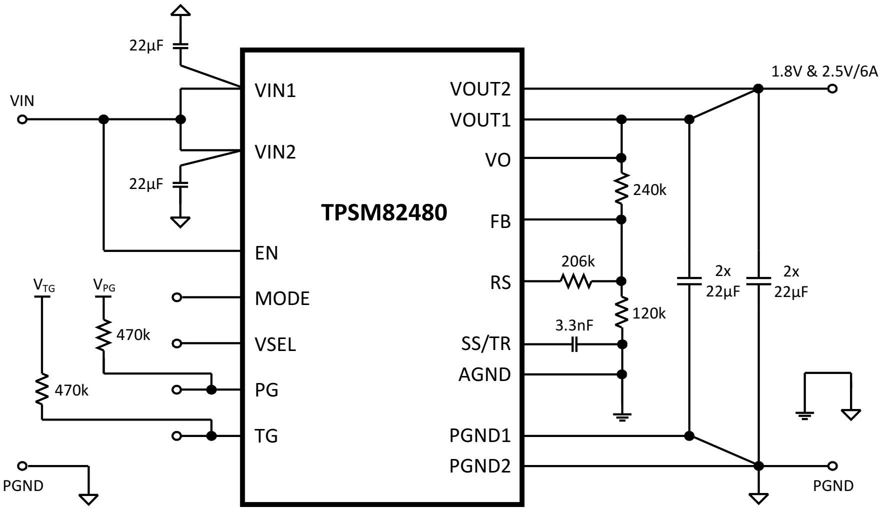


Figure 38. A typical 1.8 V & 2.5 V, 6 A Power Supply

Table 4. Resistive Divider Values for different Combinations of V_{OUT}

OUTPUT VOLTAGE	R1	R2	R3
2.5V and 3.3V	380kΩ	120kΩ	285kΩ
1.2V and 1.8V	120kΩ	120kΩ	120kΩ
0.9V and 1.0V	60kΩ	120kΩ	360kΩ

9 Power Supply Recommendations

The TPSM82480 is designed to operate from a 2.4-V to 5.5-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

10 Layout

10.1 Layout Guidelines

A recommended PCB layout for the TPSM82480 dual phase solution is shown below. It ensures best electrical and optimized thermal performance considering the following important topics:

- Both V_{OUT1} and V_{OUT2} must be connected to build a common VOUT structure.

- The input capacitors must be placed as close as possible to the appropriate pins of the device. This provides low resistive and inductive paths for the high di/dt input current. The input capacitance is split, as is the V_{IN} connection, to avoid interference between the input lines.

- The V_{OUT} regulation loop is closed with C_{OUT} and its ground connection. To avoid PGND noise crosstalk, PGND is kept split for the regulation loop. If a ground layer or plane is used, a direct connection by vias, as shown, is recommended. Otherwise the connection of C_{OUT} to GND must be short for good load regulation.

- The FB node is sensitive to dv/dt signals. Therefore the resistive divider should be placed close to the FB (and RS pin in case of using R_3) pin, avoiding long trace distance.

For more detailed information about the actual EVM solution, see SLVUAI6.

10.2 Layout Example

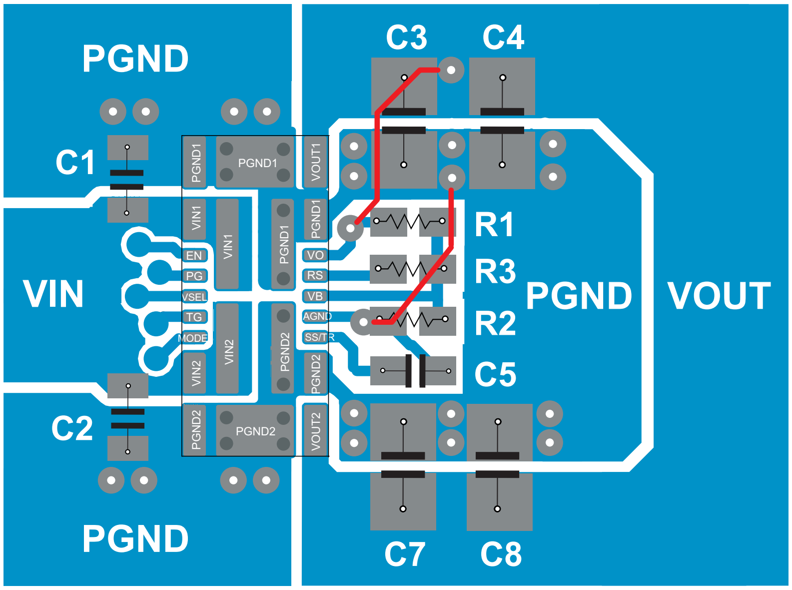


Figure 39. TPSM82480 Board Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *TPSM82480EVM-BSR002 Evaluation Module User's Guide*, SLVUB57

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5)(6)
TPSM82480MOPR	PREVIEW	QFM	MOP	24	3000	TBD	CU NIPDAU	Level-1-260C-UNLIM	–40 to 125	TBD
TPSM82480MOPT	PREVIEW	QFM	MOP	24	250	TBD	CU NIPDAU	Level-1-260C-UNLIM	–40 to 125	TBD

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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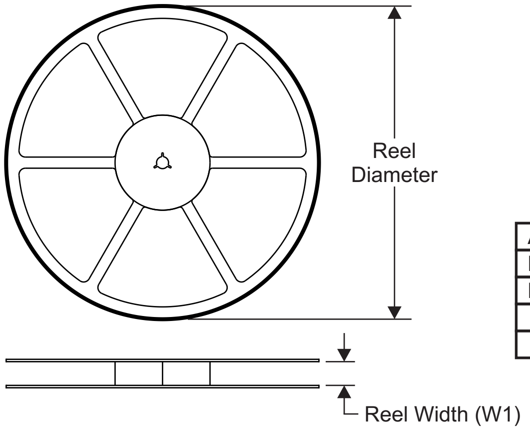
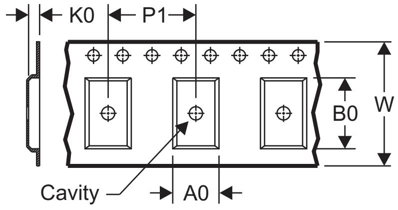
12.1.2 Tape and Reel Information

REEL DIMENSIONS

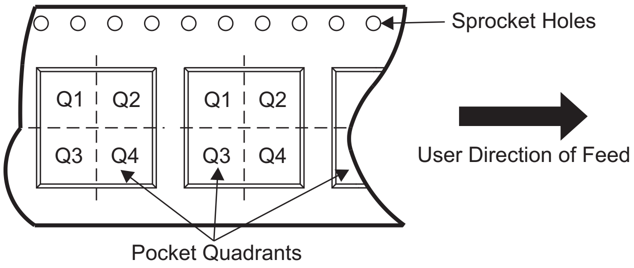


TAPE DIMENSIONS



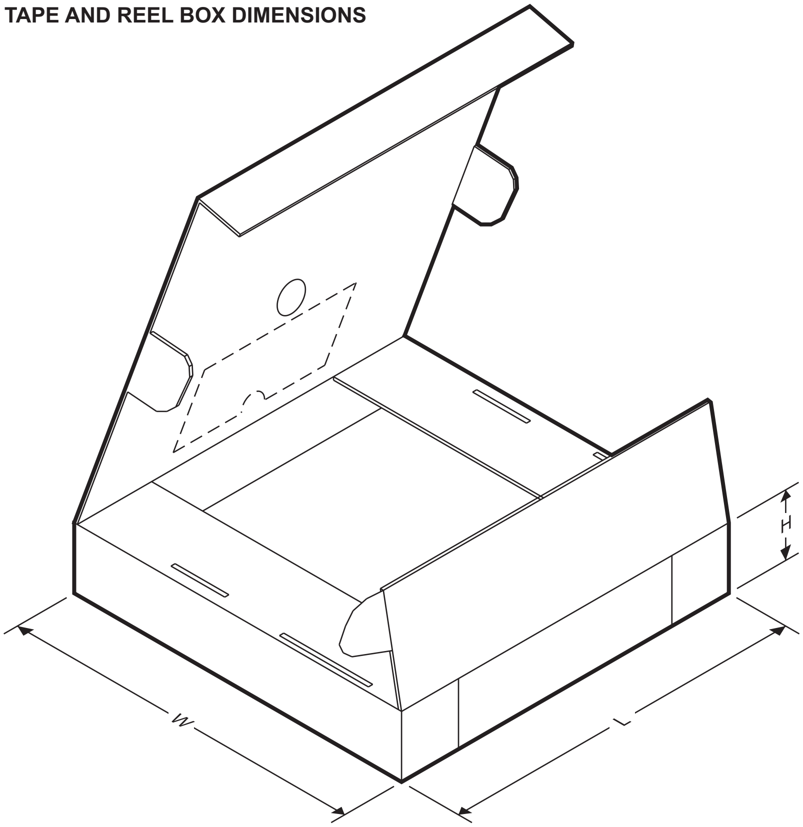
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



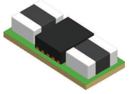
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM82480MOPR	QFM	MOP	24	3000								
TPSM82480MOPT	QFM	MOP	24	250								

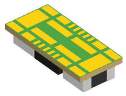
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM82480MOPR	QFM	MOP	24	3000			
TPSM82480MOPT	QFM	MOP	24	250			

ADVANCE INFORMATION



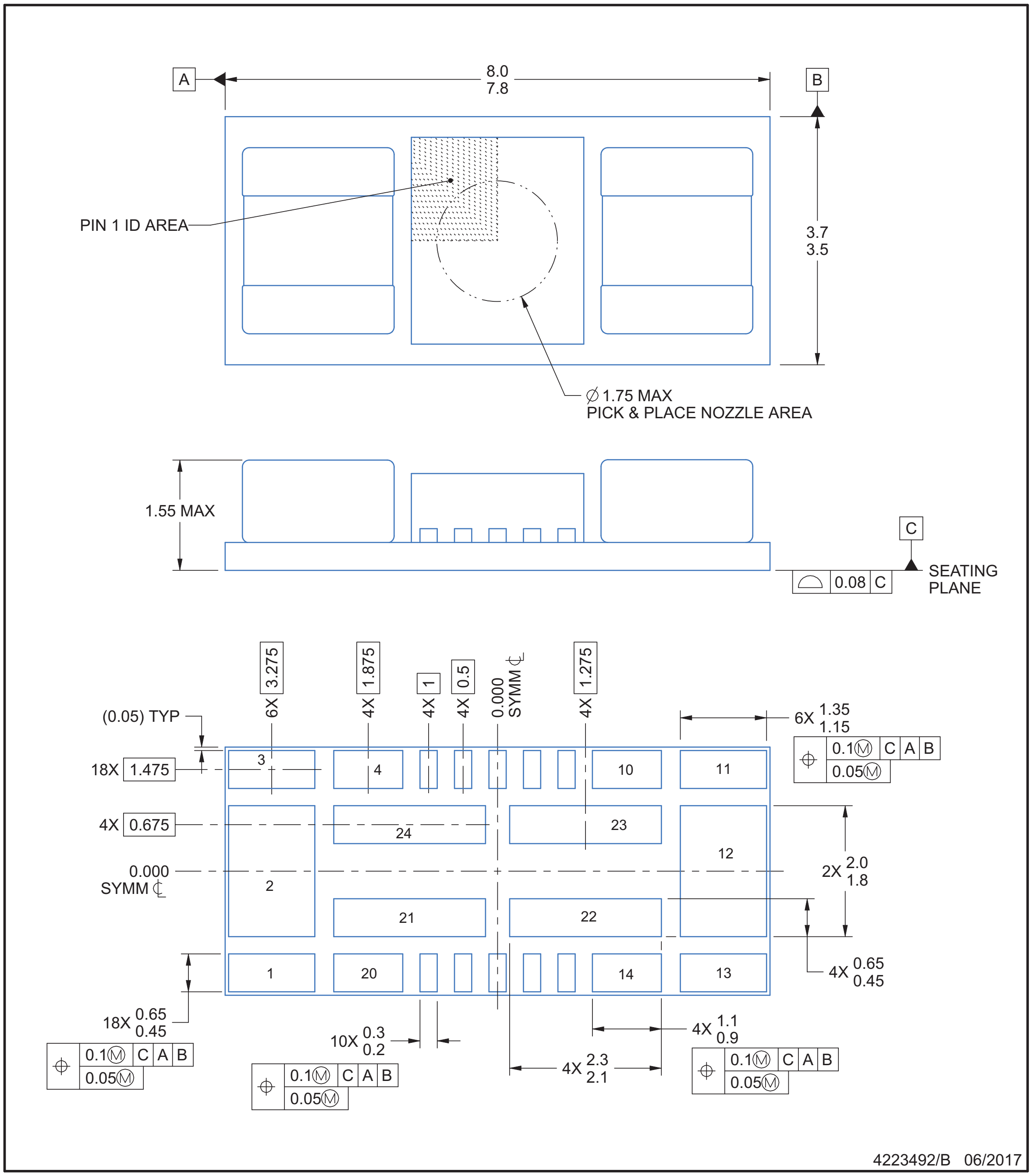


PACKAGE OUTLINE

MOP0024A

QFM - 1.55 mm max height

QUAD FLAT MODULE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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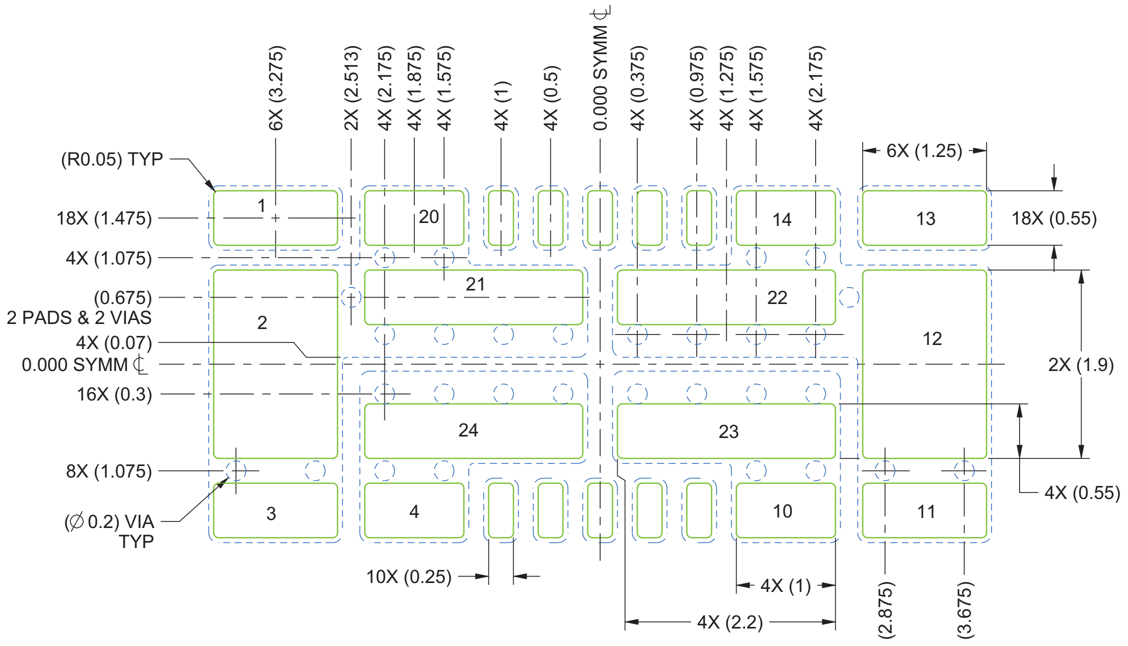
EXAMPLE BOARD LAYOUT

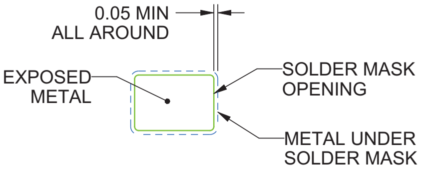
MOP0024A

QFM - 1.55 mm max height

QUAD FLAT MODULE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X



PAD DETAIL
TYPICAL

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NOTES: (continued)

3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.

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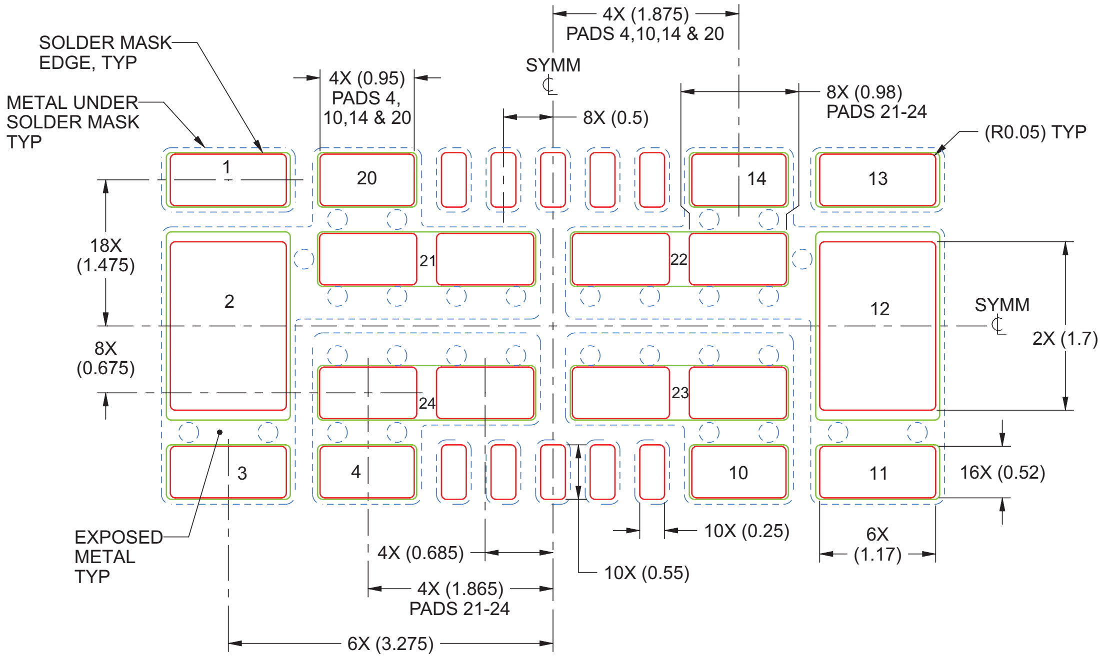
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

MOP0024A **QFM - 1.55 mm max height**

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 3, 11 & 13: 88%
PADS 4, 10, 14 & 20: 90%
PADS 2, 12 & 21-24: 84%
SCALE:15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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