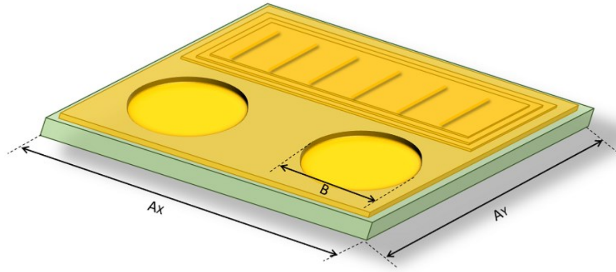
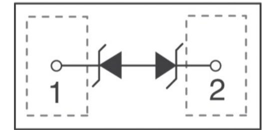
FESD5VC2M1L

Low Clamping Chip Bi-directional TVS diode

New Design for CSP





Mechanical Data	Notes
Dice size	AX:450um,AY:330um,BX:85um,BY:85um
Wafer size	4"(Gross Die:82,000pcs/good die>76,260pcs)
Chip Thickness	138um±12um
Scribe line width	60um
Top metal	Al-for wire bonding
Back side metal	Ti-Ni-Ag for soldering

Parameter	Symbol	Conditions	Value	Unit
Reverse stand-off voltage	V_{RWM}		5	V
Peak pulse power	P_{PP}	Tp=8/20us	150	W
Peak pulse current	I_{PP}	Tp=8/20us	4	A
Electrostatic discharge	V_{ESD}	IEC61000-4-2 Level 4	± 8(Contact)	KV
Max.junction temp.	Tj		+150	℃

Characteristics TA=25℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Breakdown Voltage	V_{BR}	I_T=1mA	6.4		9.0	V
Reverse leakage current	I_R	V_R=5V			0.9	uA
Clamping voltage	V_C	I_{PP}=1A I_{PP}=4A			15.0 25.0	V
Diode capacitancd pin1 to 2	Cj	V_R=0V f=1MHz		0.35	0.4	pf

Notes:
(1)sampling testing:no bad dice inking/guaranteed good die >93%
(2)Testing follow customer
(3)Tj=Ta+Rth(j-a)*(pf+pr),where Rth(j-a)-thermal resistance,Pf-forward power dissipation,
Pr-revers power dissipation
(4)**For device testing

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